ELECTRICAL & COMPUTER ENGINEERING
UNIVERSITY OF MICHIGAN

Electrical and Computer Engineering

ECE Final PhD Defense

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Building Blocks for Sampling and Digitization in High-speed Communication Systems

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Chair: Michael Flynn

Abstract:

High-speed communication systems enable global interaction between people from different nations and from different places on earth. Advances in communication technology and semiconductor fabrication technology have led to exponential growth in the speed and capacity of communication systems. At the same time, many of today's applications such as remote video meeting and on-line streaming have pushed the needs for bandwidth.

The performance of high speed communication systems crucially depends on the quality and precision of sampling and digitization. Low phase noise oscillators are essential in high data rate communication to ensure data accuracy. The ring VCO is gaining importance in ultra-scaled CMOS technologies because of its efficiency in silicon area. High-speed analog-to-digital converters are used as analog frontends of DSP-based receivers. Power efficient ADCs are required to reduce the energy cost per bit for GHz-rate communication systems.

This thesis first presents an N-path filter enhanced ring-VCO (NPFRVCO) with a novel self-filtering scheme to break the typical tradeoff between noise and power, enabling a ring oscillator to approach the phase noise performance of an LC-VCO. The new scheme only incurs a small extra cost in power consumption and does not require any extra reference or control circuitry. A new traveling wave pipeline ADC is also proposed that simultaneously achieves the maximum sampling rate and high efficiency. The scheme exploits the delay of on-chip transmission lines to implement a pipeline and thereby avoids the use of power hungry track-and-hold or MDAC stages. High sampling rates are achieved without using time interleaving, thus no interleaving calibration is needed, making the system design far easier.