A 100 MS/s, 10.5 Bit, 2.46 mW Comparator-Less Pipeline ADC Using Self-Biased Ring Amplifiers

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***Abstract*—The ring amplifier is an energy efficient and high output swing alternative to an OTA for switched-capacitor circuits. However, the conventional ring amplifier requires external biases, which makes the ring amplifier less practical when we consider process, supply voltage, and temperature (PVT) variation. This paper presents a self-biased ring amplifier scheme that makes the ring amplifier more practical and power efficient while maintaining the benefits of efficient slew-based charging and an almost rail-to-rail output swing. We introduce an improved auto-zero scheme that eliminates the gain error caused by the parasitic capacitance across the auto-zero switch. Furthermore, a comparator-less pipeline ADC structure takes advantage of the characteristics of the ring-amplifier to replace the sub-ADC in each pipeline stage. The prototype ADC has measured SNDR, SNR and SFDR of 56.6 dB (9.11 b), 57.5 dB and 64.7 dB, respectively, for a Nyquist frequency input sampled at 100 MS/s, and consumes 2.46 mW.**

***Index Terms*—A/D, ADC, analog to digital converter, auto-zero, comparator-less ADC, energy efficient, low power, ring amplifier, self-biased ring amplifier, switched capacitor.**

I. Introduction

ONE of the key requirements in the design of a pipeline ADC is accurate inter-stage amplification. In conventional switched-capacitor (SC) based ADCs, an operational transconductance amplifier (OTA) performs this amplification; however, these OTAs are one of the largest power consumers in the ADC. Additionally, cascoding is generally needed to meet the inter-stage gain requirement, but this reduces the output dynamic range. It has also become more difficult to design low-voltage OTAs in modern, scaled CMOS technologies due to the reduction in both supply voltage and intrinsic device gains. The reduced supply voltage means multi-stage amplifiers are often used instead of cascoding, which further increases power, and also possibly requires complex compensation schemes.

Several alternative approaches have been proposed to overcome the problems of conventional OTA-based SC circuits, including inverter-based SC circuits [1], [2], and zero-crossing based circuits [3]–[7]. Inverter based SC circuits have limited accuracy due to the limited gain of a single inverter. Zero-crossing circuits replace the OTA with a comparator (or zero-crossing detector) and current sources, and have the benefit of slew-based charging. Although, the concept of zero-crossing [3] is simple, the non-idealities of the building blocks and the open loop nature of its operation limit gain accuracy. Various techniques tackle these limitations [4]–[7], but these techniques make the zero-crossing more complex and limit efficiency.

Another attractive alternative is the ring amplifier [8]–[12]. The ring amplifier, essentially a stabilized offset-canceled three-stage inverter, has the benefit of slew-based charging. In addition, ring amplifiers have a near rail-to-rail output swing because the output stage is a simple inverter that operates in sub-threshold in steady state. Ring amplifier based SC circuits use feedback just as conventional OTA based SC circuits do, and therefore the accuracy depends on the gain of the ring amplifier. The required gain can be relatively easily achieved from three gain stages. Although, the simple structure of the ring amplifier is attractive, the requirement for external bias voltages limits the practicality when we consider PVT variation.

This paper presents a new self-biased ring amplifier that makes the ring amplifier simpler and more robust to PVT variation while maintaining the benefits of the ring amplifier. We also introduce an improved auto-zeroing scheme that eliminates the inaccuracy caused by switch parasitic capacitance. Furthermore, a comparator-less sub-ADC is presented that utilizes the fast internal response of the ring amplifier as a quantizer. A 10.5 b 100 MS/s prototype pipeline ADC demonstrates the effectiveness of these new techniques [13].

The paper is organized as follows. In Section II, we review the conventional ring amplifier and analyze its limitations. Section III introduces the self-bias ring amplifier and explains its benefits, Section IV describes the improved auto-zero scheme, and Section V presents the comparator-less sub-ADC technique. Finally, in Section VI, we present measurements of the prototype ADC, and conclude the paper in Section VII.

II. Review of the Ring Amplifier and its Limitations

The ring amplifier is an energy efficient and high output swing alternative to an OTA for use in SC amplifiers [8]–[12]. The ring amplifier is based on an offset-canceled three-inverter stage amplifier as shown in Fig. 1. A capacitor, C_1 stores the voltage difference between a desired common mode voltage V_{CM} and the trip point voltage of the first inverter. This voltage on C_1 is refreshed during a reset phase. Although a cascade of three inverter stages can achieve high gain, a three-stage inverter amplifier is not stable in a feedback network, such as the SC am-

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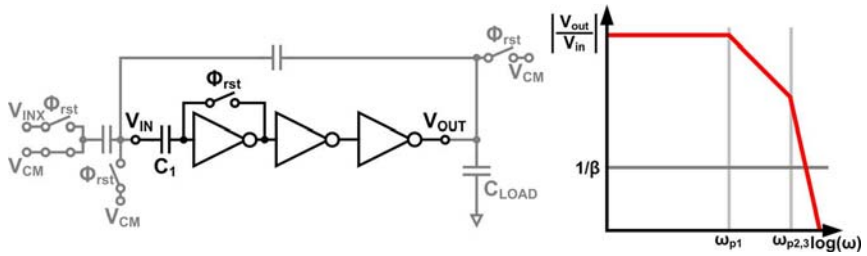

Fig. 1. An offset canceled three-stage inverter in a SC feedback amplifier configuration and its frequency response.

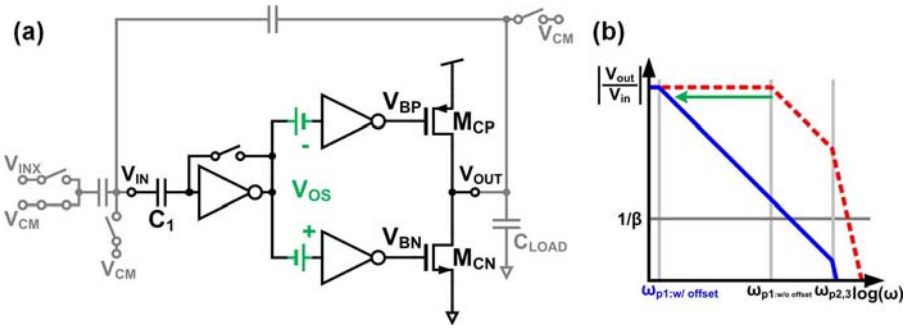

Fig. 2. Conceptual ring amplifier in a SC feedback amplifier configuration and its frequency response.

plifier shown in Fig. 1. This is because this amplifier has three poles close in frequency resulting a negative phase margin.

In order to stabilize the three inverter stage amplifier, [8]–[12] split the second stage of the amplifier in Fig. 1 into two separate inverter gain paths, and apply an offset voltage, V_{OS}, at the inputs of these two second stage inverters[1] as shown in the conceptual ring amplifier of Fig. 2(a). One second-stage inverter drives the gate of the PMOS transistor of the third stage (V_{BP}) while the other drives the gate of the NMOS transistor (V_{BN}). The offset voltages of the two second stage inverters are tuned to bias the third stage transistors, M_{CP} and M_{CN}, in sub-threshold as V_{IN} approaches V_{CM}:

$$V_{BP} > V_{DD} - |V_{th:P}|, \quad V_{BN} < V_{th:N}. \tag{1}$$

In this way, as V_{IN} approaches V_{CM}, the output resistance of the third stage dramatically increases, forming a dominant pole that stabilizes the overall amplifier [Fig. 2(b)]. While settling, this ring amplifier has a high output slewing current. However, when it is settled the current from the output stage, operating in sub-threshold, is negligible. Fig. 3 shows the conventional, practical implementation of a ring amplifier [8]–[12]. The capacitors, C_2 and C_3, act as the floating bias offset voltage sources in Fig. 2. An external bias voltage, V_{OS}, sets these capacitor voltages during a reset period.

A positive small-signal phase margin is a necessary but insufficient condition for stability of the ring amplifier. In fact, a ring amplifier can become unstable due to large signal effects even if there is a positive phase margin. This is because the current of the last stage transistors changes dramatically around the target

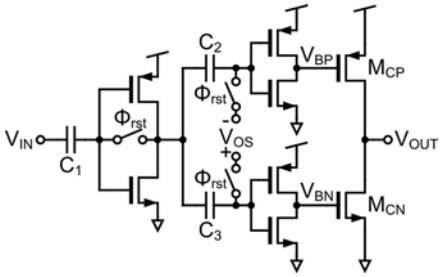

Fig. 3. Conventional ring amplifier [8]–[12].

settling point, making the large signal behavior of the ring amplifier highly nonlinear. As an example, Fig. 4 shows the simulated large signal behavior of the ring amplifier in the SC amplifier configuration,[2] shown in Fig. 2. In this example, the ring amplifier has phase margin of 73° when V_{IN} is at V_{CM}, but is still unstable.

The simulation shown in Fig. 4 begins as the amplifier emerges from the reset phase. If the overall SC amplifier input, V_{INX}, is higher than V_{CM}, the ring amplifier input, V_{IN}, initially falls at the beginning of the amplification phase and the gain of the first and the second inverter stages causes the gate voltages, V_{BP} and V_{BN}, of the last stage PMOS and NMOS transistors to hit ground. In this condition, the PMOS transistor of the last stage strongly conducts so that the output of the ring amplifier, V_{OUT}, slews towards V_{DD} (i.e., 1.2 V in this example). Ideally, this slewing should stop as V_{IN} reaches V_{CM} (i.e., 0.6 V), but here slewing continues and V_{IN} overshoots V_{CM} because the inverters and the feedback path have a finite response time. This V_{IN} overshoot causes V_{BN} and V_{BP} to reach V_{DD}, strongly turning on the NMOS of the last stage and causing V_{OUT} to start slewing down towards ground. If this falling slew rate is similar to the previous rising slew rate, then

[1][11] introduces a fine ring amplifier which applies an offset voltage at the output of the second stage inverter, without splitting the second stage inverter, to more precisely control the output stage overdrive voltage. This fine ring amplifier offers a higher gain but a reduced slew rate. The reduced slew rate is overcome by using the ring amplifier in [8]–[10] in parallel with the fine ring amplifier.

[2]Ideal switches without charge injection or clock feed-through are used in this simulation for clarity.

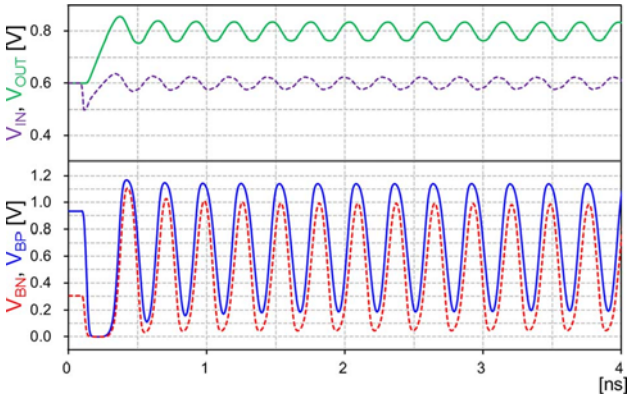

Fig. 4. Simulated transient response of the ring amplifier of Fig. 2. The ring amplifier oscillates even with 73° of positive phase margin.

slewing and overshoot repeat in alternate directions, leading to sustained oscillation.

As seen in this example, the ring amplifier can still oscillate even if there is a substantial positive phase margin. In order to prevent this sustained oscillation, we must configure the circuit so that the overshoot decreases each successive oscillation. The overshoot is proportional to the gain of the three stages, the slew rate, the feedback factor, and the response time. Therefore, reducing the gain of the three stages, or reducing the slew rate, or reducing the feedback factor can reduce overshoot. Reducing the response time by increasing the bandwidth of the first and the second inverters also reduces the overshoot.[3] The gain and the feedback factor are usually determined by the target application, so this tuning is best done by reducing the slew rate and increasing the first and second inverter bandwidths. Tuning is a tradeoff between the speed needed for the application and the power consumption.

The ring amplifier delivers high gain from its three gain stages without the need for complicated gain enhancement techniques. Furthermore, the ring amplifier can slew very efficiently because the third stage inverter acts as a pair of digital switches during slewing. However, the conventional ring amplifier circuit has drawbacks because it depends on the external offset voltage, V_{OS}. The quiescent voltages of V_{BP} and $V_{BN,}$ when $V_{IN} = V_{CM}$, must be set within narrow voltage windows as illustrated in Fig. 5. If the quiescent overdrive voltages of the last stage are set too high then the ring amplifier can oscillate because the output resistance of the third inverter stage is never sufficiently large to create a sufficient phase margin. On the other hand, if the quiescent overdrive voltage is too low, the bandwidth of the last stage is reduced and the ring amplifier might not settle fully within the given settling time. With a low quiescent overdrive voltage, even if the ring amplifier settles in the given settling time, the second stage inverters operate in the triode region resulting in a low overall three-stage gain.[4] Setting

[3]These observations agree well the [10, (8)].

[4]This low second stage gain can be avoided by applying the offset voltage at the output of the second stage inverter without using two second-stage inverters [11]. However this reduces the offset voltage setting accuracy since the sampled offset leaks through parasitic diodes of the switches because the voltages of offset sampling capacitors exceed the rails during slewing – the amount of leakage depends on slewing time.

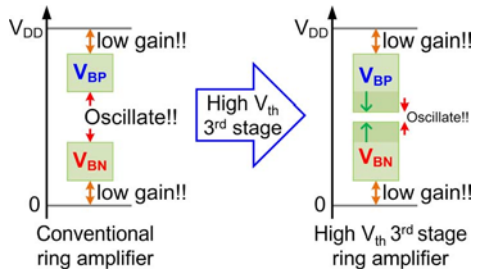

Fig. 5. Ring amplifier third stage quiescent offset voltage range.

V_{OS} for these narrow V_{BP} and V_{BN} voltage windows is difficult when we consider PVT variation of the second and third stage inverters. Furthermore, the common mode of V_{OS} also determines the output common mode voltage of the ring amplifier. The common mode of V_{OS} is amplified by gains of the second and third stages to set the output common mode voltage. This is also affected by PVT variation making it difficult to set the output common mode within a certain range. Some of the PVT variation issue can be solved by using on-chip biases that track PVT variation [12]. However, we still need to consider the device to device variation which can cause large output common mode variation. The device to device variation is particularly problematic since the ring amplifier uses almost minimum sized transistors [9].

III. Self-Biased Ring Amplifier

In this section, we introduce the new self-biased ring amplifier and explain its benefits. We adopt high threshold devices for the last stage inverter to extend the stable offset (V_{OS}) range. We also eliminate the external biases and the split second stage inverter. We dynamically apply an offset using a resistor in the second stage to make the ring amplifier more practical and power efficient.

A. Introducing High Threshold Device for the Last Stage

We introduce high threshold devices in the third stage of the ring amplifier to take advantage of their higher output resistance. Because we can get orders of magnitude higher output resistance from the high threshold voltage device inverter,[5] we can extend the V_{OS} range (or the range quiescent overdrive voltages V_{BP} and V_{BN}) as illustrated in Fig. 5. This extended V_{OS} range increases the robustness of the ring amplifier to PVT variation.

B. Ring Amplifier Without Offset Biasing

Adopting high threshold devices for the last stage allows us to stabilize a three-inverter stage amplifier without the split second stage and offsets, as shown in Fig. 6. When the sum of threshold voltages of transistors in the third stage inverter is higher than the power supply voltage (i.e., $V_{TH:N} + |V_{TH:P}| > V_{DD}$), then third stage operates in the sub-threshold region. The three-stage inverter is stabilized since the third stage forms a dominant

[5]This also reduces the slewing current of the ring amplifier. However, for same sized last stage transistors, the output resistance in steady state is two to three orders of magnitude higher while the slewing current is reduced by a half to a quarter. Therefore, the use of high threshold voltage devices for the last stage is beneficial although we need to increase the size of the last stage to make the slewing current the same.

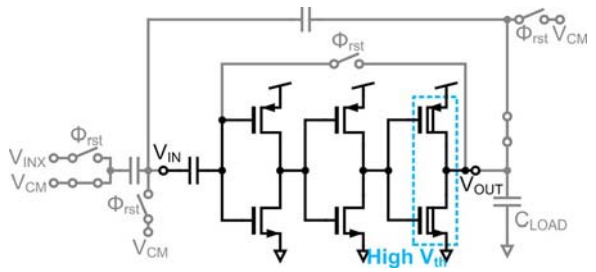

Fig. 6. Offset-less ring amplifier. This can be stabilized when the sum of the last stage inverter transistors threshold voltage is higher than the power supply voltage ($V_{TH:N} + |V_{TH:P}| > V_{DD}$).

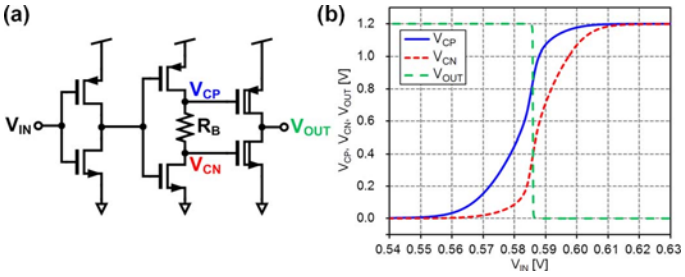

Fig. 7. Ring amplifier with dynamically applied offset using a resistor R_B in the second stage inverter.

pole due to the significantly higher output resistance from the sub-threshold operation. This simple three-stage ring amplifier has two advantages compared to the conventional ring amplifier. Firstly, the reduced number of second stage inverters, together with the removal of the offset capacitors and the switches, reduces the loading on the first stage, allowing us to reduce the power consumption of the first inverter while maintaining the same first stage bandwidth. Secondly, we can auto-zero the entire three inverter stages as in Fig. 6 and this gives us a more stable output common mode even with PVT variation, and the device to device variation. However, this simplified offset-less ring amplifier is not practical because the power supply voltage condition ($V_{TH:N} + |V_{TH:P}| > V_{DD}$) is not always true.

C. Dynamic Offset Using Resistor in the Second Stage Inverter

In order to avoid these constraints on the power supply voltage, while keeping the advantages of a single inverter-based second stage without external biases, we embed a polysilicon resistor, R_B, between the drains of the NMOS and PMOS transistors of the second-stage inverter, as shown in Fig. 7(a). R_B dynamically applies an offset to gate voltages, V_{CP} and V_{CN}, of the third stage inverter transistor thanks to the IR drop due to the inverter short circuit current. There is now a voltage offset between the gates of the last stage PMOS and NMOS transistors when V_{in} is close to the virtual ground. As we can see in Fig. 7(b), the second inverter still drives the last stage rail-to-rail when the ring amplifier input, V_{in}, is away from the virtual ground. The offset voltage variation caused by the R_B resistance variation and the second inverter short circuit current variation is acceptable as long as it is within the stable V_{OS} range. As explained in Section III-A, the acceptable V_{OS} range is extended by using high threshold device in the last stage. This increases the design margin for offset voltage variation.

This resistor based dynamic offset ring amplifier has another benefit. Since the offset depends on the short circuit current of the second stage inverter, this offset tracks the power supply voltage. This means the ring amplifier with dynamic offset biasing can operate over a wider V_{DD} range. The short circuit current of the second-stage inverter can be calculated from the NMOS saturation region square law equation:

$$I_D = \frac{1}{2}\mu_n C_{ox}\frac{W_n}{L_n}\left(\frac{V_{DD}}{2} - V_{TH:N}\right)^2. \quad (2)$$

This assumes that the second inverter is balanced so that the trip point of the second inverter is $V_{DD}/2$. As shown in (2), the inverter current increases quadratically as V_{DD} increases and therefore the voltage across R_B also increases quadratically. Ideally, the offset voltage should linearly track[6] V_{DD} to maintain the same overdrive voltage on the last stage transistors regardless of V_{DD}. Nevertheless, the increase in IR drop with V_{DD} along with the extended offset range facilitated by the high threshold voltages of the last stage ensures a wide V_{DD} operating range.

D. Noise and Power Optimization

We optimize the noise and the power consumption of the first stage inverter. The first stage inverter is the dominant noise source of the dynamic offset ring amplifier in Fig. 7. Although flicker noise is mostly removed by the auto-zeroing [14], thermal noise cannot be cancelled. Since the thermal noise of an inverter is inversely proportional to the g_m of the inverter, we must increase g_m to reduce the thermal noise. For a given length and for a fixed gain, the only way to increase the g_m of an inverter is to increase the width of the inverter. However, increasing the width also increases the power consumption.

If we also adjust the power supply voltage of the first inverter then we do not have to significantly increase power consumption to reduce the thermal noise. In fact, we can get a higher g_m for a given quiescent current, I_D, from an inverter when we reduce the power supply voltage. Since the g_m of a MOS transistor is $2I_D/(V_{GS} - V_{TH})$ when we assume strong inversion operation, then assuming the trip point of the inverter is $V_{DD}/2$, we get g_m/I_D of an inverter as:

$$\frac{g_m}{I_D} = \frac{2}{\left(\frac{V_{DD}}{2} - V_{TH:N}\right)} + \frac{2}{\left(\frac{V_{DD}}{2} - |V_{TH:P}|\right)}. \quad (3)$$

Equation (3) shows that g_m/I_D of an inverter increases as we decrease V_{DD}. Fig. 8 shows the simulated g_m and bandwidth of the first stage inverter at the trip point versus the first stage inverter V_{DD} ($V_{DD:inv1}$). The short circuit current of the first stage inverter is fixed in this simulation by changing the width of the inverter. We can get a close to maximum bandwidth with about 2.8 times higher g_m compared with the default power supply (1.2 V) when $V_{DD:inv1}$ is around 0.85 V. As we see from the simulation, we can get optimum g_m and bandwidth with a lower $V_{DD:inv1}$ which allows us to reduce the thermal

[6]This can be achieved by using triode mode N/PMOS resistors instead of a poly resistor. However the use of triode mode transistors also increases the loading capacitance of the second stage and therefore also the power consumption of the ring amplifier.

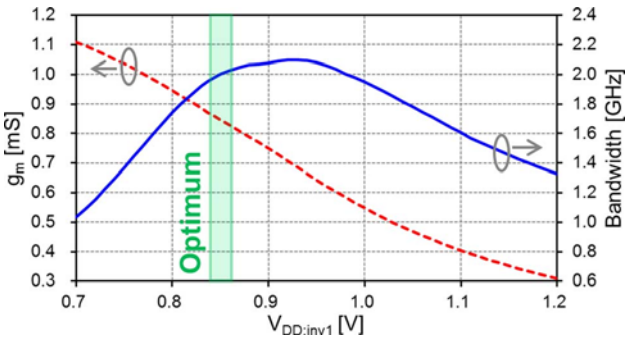

Fig. 8. Simulated first stage bandwidth and transconductance versus first stage power supply voltage ($V_{DD:inv1}$) with fixed stage current.

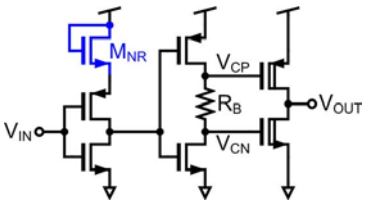

Fig. 9. Self-biased ring amplifier. Here M_{NR} is used as an internal power regulator of the first stage inverter.

noise of the first stage inverter without significantly increasing power consumption.

Instead of using an external voltage, we lower $V_{DD:inv1}$ using a diode-connected NMOS (M_{NR}) as shown in Fig. 9. The diode connected M_{NR} works as an internal regulator and effectively lowers the power supply voltage of the first stage inverter without additional power consumption. The size of M_{NR} needs to be large to reduce the regulated voltage variation. Fig. 9 shows the final structure of the self-biased ring amplifier.

IV. Ring Amplifier Auto-Zero

As discussed in the previous section, unlike the conventional ring amplifier, which only cancels the offset of the first stage, we auto-zero the entire input offset of the self-biased ring amplifier. The auto-zeroing is required to cancel the difference between V_{CM} and the input common voltage of the ring amplifier. This also removes the output offset of the ring amplifier, unlike the conventional ring amplifiers [8]–[12], and this helps maximize the usable dynamic range of the output swing. In this section, we explain the problems of auto-zeroing the ring amplifier in a flip-around 1.5 b MDAC gain stage (Fig. 10), and introduce a new scheme that overcomes these problems.

A. Stability During Auto-Zero

We first consider stability during the auto-zero. When Φ_1 is high (i.e., the sampling/auto-zeroing phase) the MDAC stage in Fig. 10 samples the input, V_{in}, onto the sampling capacitors C_1 and C_2, and at the same time samples the offset of the ring amplifier on the offset sampling capacitor, C_C. Then, when Φ_2 is high (the amplification phase), the MDAC stage amplifies the sampled voltage by transferring the sampled input charge to C_1 capacitor. During the amplification phase, the ring amplifier sees the sampling capacitors of the next pipeline stage as the load capacitance. In addition, the feedback factor during the amplification phase is about a half. However, during the sampling/auto-zeroing phase, the offset sampling capacitor, C_C, is the only load, and also the feedback factor increases to about one. The increased feedback factor and the reduced load capacitance (i.e., assuming $C_C < C_1+C_2$) during the auto-zero phase make the ring amplifier hard to stabilize because these reduce the phase margin, and increase the slew rate. It is possible to design a ring amplifier that is stable during auto-zeroing with this condition, but this requires higher power consumption than that required for the amplification phase. If C_C is equal to C_1 and C_2, then to stabilize the ring amplifier during the auto-zero phase, the second and third poles of the ring amplifier need to be four times higher than that required to stabilize it during the amplification phase. This requires at least four times higher power for the first and second inverters.

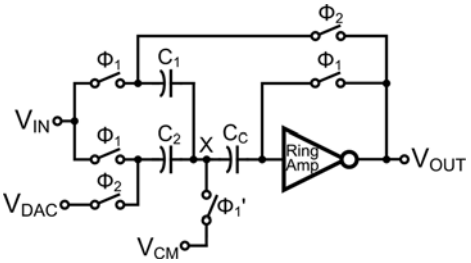

Fig. 10. Auto-zeroed flip-around 1.5 b MDAC gain stage using a ring amplifier. This configuration has potential stability problems during auto-zero.

One approach to improving stability during the sampling/auto-zeroing phase without using more power is to increase the C_C capacitance, but this is not desirable for moderate resolution ADCs where the auto-zero related noise is not dominant. In order to stabilize the ring amplifier during auto-zero, and considering the twice larger feedback factor, C_C needs to be at least twice as large as sampling capacitance of the next stage ($C_C > 2(C_1 + C_2)$). However, that would require a large area since C_C should be a floating capacitor and floating capacitors such as MIM or MOM have a relatively low per unit area capacitance. A high density MOS capacitor can be used for C_C, but a MOS capacitor has a relative large bottom plate parasitic capacitance. The large bottom plate parasitic capacitance of C_C on the virtual ground node X increases the gain error during the amplification [15] because the bottom plate capacitance of C_C steals some of the sampled signal charge due to the imperfect virtual ground.

Instead of using a large C_C, we periodically add a loading capacitor C_{LA}, as shown in Fig. 11. C_{LA} is connected to the output of the ring amplifier during the auto-zero phase, but not during the amplification phase. The sum of C_C and C_{LA} needs to be at least twice as large as the next stage sampling capacitors (i.e., $C_C + C_{LA} > 2(C_1 + C_2)$). However, the use of a large C_{LA} does not require much area because we can use a high per unit area capacitance MOS capacitor, since one terminal of C_{LA} is always connected to ground. In addition, the addition of C_{LA} does not increase power consumption since the sampled offset voltage on C_{LA} stays constant in every cycle.

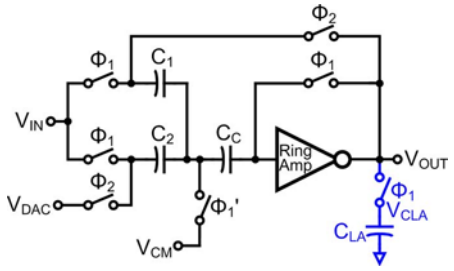

Fig. 11. Auto-zeroed flip-around 1.5 b MDAC gain stage using a ring amplifier with stabilization loading capacitor C_{LA}.

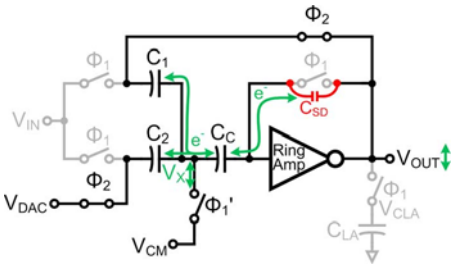

Fig. 12. Gain error mechanism due to the parasitic capacitance of the auto-zero switch.

B. Improved Auto-Zero Switch to Eliminate Gain Error

Another important consideration is the gain error due to the parasitic capacitance across the auto-zero switch. As shown in Fig. 12, the source-drain parasitic capacitance, C_{SD}, of a conventional auto-zero switch scheme causes a gain error during the amplification phase. As the ring amplifier output voltage, V_{OUT}, moves during the amplification phase, C_{SD} steals (or injects) charge from (or to) the C_C capacitor and this also changes the sampled input charge in the sampling capacitors, C_1 and C_2. In addition, the change in charge on C_C also moves the virtual ground voltage, V_X, from V_{CM}, which also causes a gain error. The gain of the MDAC gain stage in Fig. 12 including the gain error caused by C_{SD} can be calculated as:

$$\frac{V_{OUT}}{V_{IN}} = \frac{2}{1+\left(\frac{1}{C}+\frac{2}{C_C}\right)C_{SD}} \tag{4}$$

where C_1 and C_2 have the same value C, V_{DAC} is equal to V_{CM}, and we assume the ring amplifier has infinite gain and zero offset for simplicity. As we can see from the equation, C_{SD} is problematic for gain accuracy.

One way to reduce this gain error is to minimize C_{SD} using layout techniques. For example, we can minimize C_{SD} by extending the distance between the source and drain of the auto-zero switch, or by adding a shield in between. However, we cannot completely eliminate this gain error because C_{SD} still exists due to the electrical field in the substrate and we cannot completely shield over the gate poly.

We introduce an improved auto-zero switch, as shown in Fig. 13, to eliminate the C_{SD} related gain error. This improved auto-zero scheme makes use of the sampled ring amplifier offset voltage, V_{CLA}, stored on C_{LA}, which we already use to stabilize the ring amplifier during the auto-zero phase. During the auto-zero phase, the scheme works in the same way as a conventional auto-zero by turning on the switches S_{AZ1} and S_{AZ2}, and turning off the switch S_{AZ3}. During the amplification phase, S_{AZ1} and S_{AZ2} are turned off and S_{AZ3} connects the intermediate auto-zero switch voltage, V_{AZ}, to the sampled offset voltage, V_{CLA}, which effectively grounds C_{SD} to V_{CLA}. In this way, C_{SD} no longer affects the charge on the other capacitors, even as V_{OUT} moves.

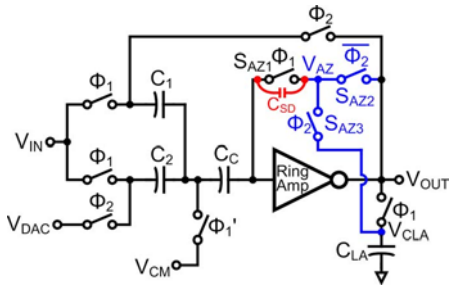

Fig. 13. An improved auto-zero switch that is free from C_{SD} related gain error.

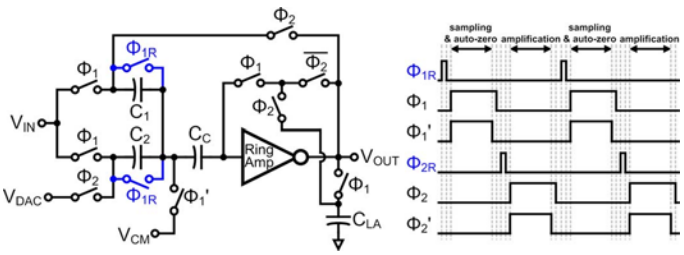

Fig. 14. Modification of the ring amplifier MDAC to use the amplification direction information. The sampling capacitors C_1 and C_2 are reset right before the sampling phase to ensure the amplification of the previous stage always starts from V_{CM}.

V. Comparator-Less Sub-ADC Using Ring Amplifier

We introduce a comparator-less MDAC stage that uses the self-biased ring amplifiers as comparators by exploiting a unique characteristic of the ring amplifier. As discussed in Section II, during the amplification phase, the second stage outputs reach ground when the ring amplifier output slews up, and the second stage outputs reach V_{DD} when the ring amplifier output slews down. In other words, the second stage output voltage indicates the amplification direction during ring amplifier output slewing. In fact, the first two stages of the ring amplifier work as an offset canceled continuous time comparator at the beginning of the amplification as a byproduct of the slow response of the last stage. We can use this amplification direction information as the next stage MDAC sub-ADC decision. This allows us to further reduce the power consumption of a ring amplifier based pipeline ADC by eliminating dedicated clocked comparators for the sub-ADCs.

In order to properly use this direction information from the ring amplifier, we first ensure the amplification always starts from V_{CM}. To ensure this, we reset the sampling capacitors C_1 and C_2 using a short pulse Φ_{1R} before the sampling phase, as shown in Fig. 14. This resetting operation also reduces the maximum slew requirement by half, which allows us to further reduce the ring amplifier power consumption for the same operating speed.

We can sample the amplification direction from the second stage output V_{CP} of the self-biased ring amplifier (Fig. 9) by using a minimum sized NOR gate and a set-reset (SR) latch as

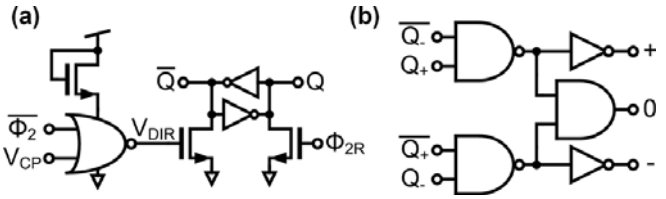

Fig. 15. (a) Amplification direction sampling circuit. (b) Amplification direction information to 1.5 b sub-ADC result decode logic. Q_+ and Q_- are from each side of the pseudo-differential ring amplifier MDAC gain stages.

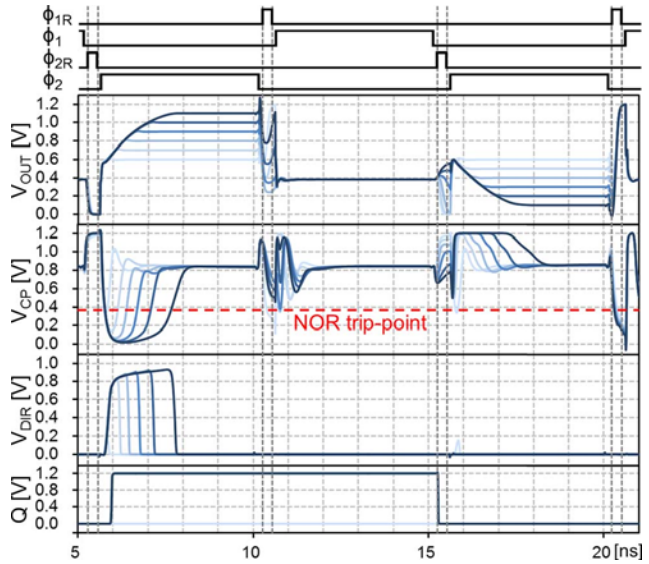

Fig. 16. Simulation of the MDAC gain stage in Fig. 14 with the amplification direction sampling circuit in Fig. 15 for various input voltages.

in Fig. 15(a). The latch consists of weak back-to-back inverters, and pull-down set-reset NMOS transistors. The latch can be set or reset by turning on only one of the pull down transistors. Fig. 16 shows a simulation of the MDAC gain stage (Fig. 14) with the direction sampling circuit for various input voltages. The NOR gate inverts V_{CP} during the amplification phase and outputs 0 during the sampling phase. The supply voltage of the NOR gate is reduced by a diode connected NMOS transistor in order to reduce the logic threshold voltage of the gate. This helps to get the correct NOR trip-point for the direction sampling and prevents unwanted short circuit current after the ring amplifier slewing due to the lower than V_{DD} quiescent voltage of V_{CP}. The SR latch is reset right before the amplification phase and samples the amplified direction information from the NOR gate output V_{DIR}. We can use the latch output, Q, as the next MDAC stage sub-ADC result. A similar circuit samples the opposite direction information from the opposite side of the MDAC pseudo-differential stage. The simple decoding circuit in Fig. 15(b) decodes the two direction information bits ($Q+$ and $Q-$) to provide the 1.5 b sub-ADC result for the next stage.

The auto-zero ensures the correct amplification direction even with PVT variation, while the NOR trip-point and the ring amplifier slew rate define the threshold of the direction sampling. The direction sampling threshold voltage tends to be close to V_{CM} because V_{CP} drops near ground for even slightly positive V_{OUT} slewing and the slew is tuned to be slow (about half of amplification period for maximum swing) for better power efficiency. Therefore, even with some PVT variation, the thresholds are well within the redundancy ($\pm 1/2V_{ref}$) of the 1.5 b/stage pipeline ADC.

VI. ADC Implementation and Measured Results

A 100 MS/s, 1.5 b/stage 10.5 b pipeline ADC [13] is implemented as a proof of the concept prototype to demonstrate the effectiveness of the self-biased ring amplifier. As shown in Fig. 17, the ADC is composed of a flip-around sample and hold amplifier (SHA) [16] with the bootstrapping input switches [17], nine 1.5 b flip-around MDAC stages, and dummy loading for the last stage. Figs. 18 and 19 show the pseudo-differential ring amplifier based flip-around SHA and MDAC gain stage used in the ADC. The pseudo-differential CMFB in [8] is implemented for all stages. The SHA also works as the first MDAC 1.5 b sub-ADC.[7] To further optimize the power efficiency, the seven last MDAC stages are scaled down by half compared to the first two MDAC stages. Identical self-biased ring amplifiers are used for the SHA and for the first two MDACs. The SHA uses a sampling capacitance (C_S) of 400 fF and the first two MDAC stages use sampling capacitors (C_1, C_2) of 200 fF. The SHA and the first two MDAC stages use 200 fF offset storage capacitors (C_C). The ring amplifiers used in the seven last MDAC stages use half width transistors and a doubled resistance R_B when compared with the ring amplifier of the first two MDAC stages. R_B is doubled to generate the same bias voltages, V_{CP} and V_{CN}, as the first two stages with half the inverter short-circuit current.

The prototype ADC is fabricated in a single poly nine metal (1P9M) 1.2 V 65 nm CMOS process. The ADC core fits within a small area of 0.097 mm^2, as shown in the die microphotograph in Fig. 20. A summary of performance is shown in Table I.[8] The top and bottom references are set at 1.1 V and 0.1 V thanks to the wide swing of the ring amplifier which results a full-scale differential input signal of 2 $V_{pk\text{-}pk}$. Linearity plots (Fig. 21) measured at 10 b and at a full conversion rate of 100 MS/s, show that the measured DNL and INL are within ± 0.22 LSB and $-0.62/+0.54$ LSB, respectively. As shown in the measured spectrums (Fig. 22), at a 100 MHz sampling rate the ADC achieves 57.9 dB SNDR, 58.2 dB SNR, and 71.9 dB SFDR with a 10.08 MHz input, and 56.6 dB SNDR, 57.5 dB SNR, and 64.7 dB SFDR with a Nyquist frequency input. Fig. 23 summarizes the measured SFDR, SNR, and SNDR versus input frequency. The ADC has a quite flat SNR response while SFDR (also SNDR affected by SFDR) is degraded at higher input frequency due to imperfect bootstrapping sampling switch design. The ADC has linear SNDR response up to the full-scale (Fig. 24). For a 2 $V_{pk\text{-}pk}$ input swing, the SNDR

[7]We implement the SHA in this ADC to demonstrate a completely comparator-less pipeline ADC. We can eliminate SHA as in [9] if we use a conventional flash ADC for the first stage sub-ADC. The elimination of SHA also improves SNR and power efficiency of the ADC since the SHA adds noise to the sampled input signal without providing amplification. From a power consumption point of view, it is better to use this ring amplifier based comparator-less MDAC for all stages except the first stage sub-ADC for better performance.

[8]The ADC measurements have been updated since those reported in [13]. The measurements in [13] were degraded by digital output I/O related supply noise. The ADC and the test board were revised to achieve better isolation between the ADC core and the digital output I/O.

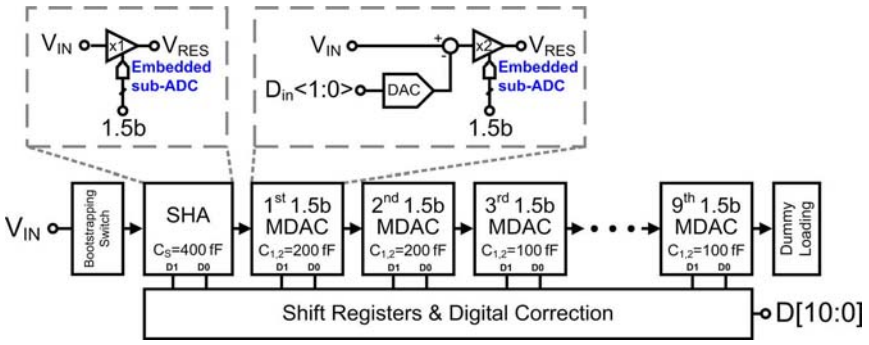

Fig. 17. Prototype ADC structure.

TABLE I
ADC PERFORMANCE SUMMARY

Resolution	10.5 bit	
Supply	1.2 V (Analog, Clock), 0.75 V (Digital)	
Sampling Rate	100 MS/s	
Technology	65 nm 1P9M CMOS	
Active Area	0.097 mm^2	
Input Range	2.0 $V_{pk\text{-}pk}$ differential	
DNL (10 bit)	-0.22/+0.22 LSB	
INL (10 bit)	-0.54/+0.62 LSB	
Power Consumption	2.46 mW Total: 2.33 mW (Analog + CLK), 61.6 µW (Ref.), 65.4 µW (Digital)	
	F_{in}=10.08 MHz	**F_{in}=49.97 MHz**
SNDR	57.9 dB	56.6 dB
SNR	58.2 dB	57.5 dB
SFDR	71.9 dB	64.7 dB
ENOB	9.33 bit	9.11 bit
FoM [P/($f_s \cdot 2^{ENOB}$)]	38.4 fJ/conv-step	44.5 fJ/conv-step

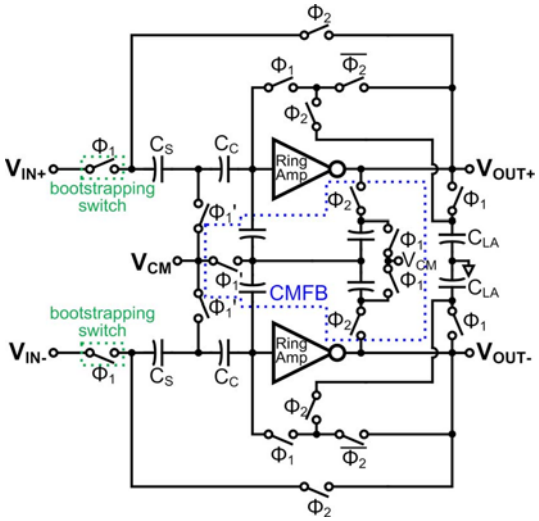

Fig. 18. Pseudo-differential ring amplified based flip-around sample and hold amplifier.

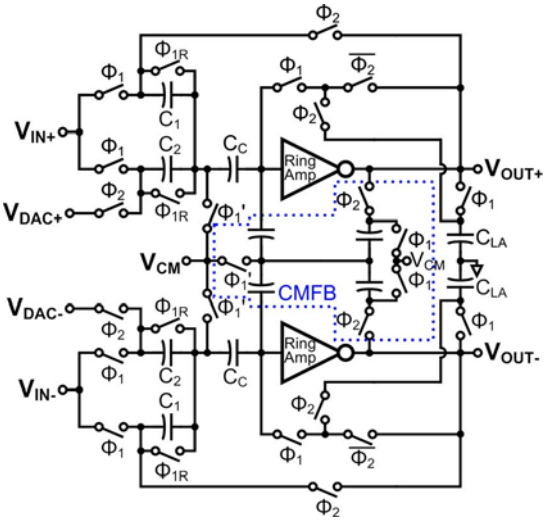

Fig. 19. Pseudo-differential ring amplified based MDAC gain stage.

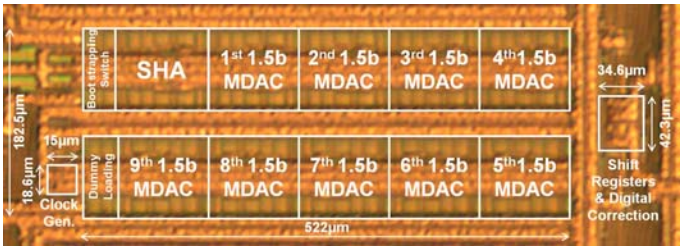

Fig. 20. Die microphotograph of prototype ADC.

with a Nyquist input frequency remains higher than 56 dB over an analog power supply voltage range from 1.2 V to 1.28 V (Fig. 25). This proves that the dynamic bias using a resistor, R_B, effectively tracks the power supply voltage variation. The SNDR increases as the supply voltage increases up to 1.26 V because the g_m of the first stage inverter increases as the supply voltage increases, and the increased g_m reduces thermal noise of the ring amplifiers. However, the SNDR drops when the supply voltage is higher than 1.26 V because the quiescent offset voltage across R_B increases faster than the supply voltage, and this causes the second stage to operate in the triode region resulting a lower overall three-stage gain. This reduced overall gain gives us a lower SFDR and thus also a reduced SNDR.

The ADC consumes a total power (excluding I/O) of 2.46 mW at the full conversion speed of 100 MS/s, with a Nyquist frequency input. This results in a figure-of-merit (FoM) of 38.4 fJ/conversion-step for a 10.08 MHz input, and 44.5 fJ/conversion-step for a Nyquist frequency input. This power consumption is comprised of the 1 mW ring amplifier static power dissipation, 62 μW for the reference, and 65 μW for the shift register and digital correction. The remaining

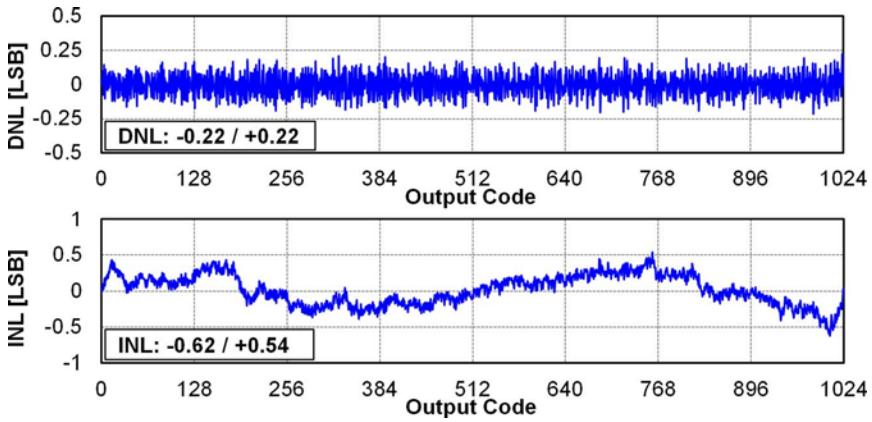

Fig. 21. Measured DNL and INL at 10 b level, 100 MSPS.

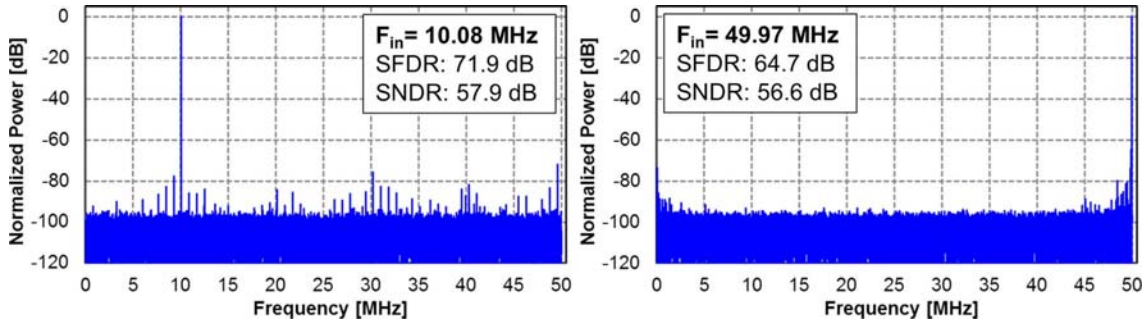

Fig. 22. Measured spectrums for 10.08 MHz and 49.97 MHz inputs sampled at 100 MS/s (65,536 point FFT).

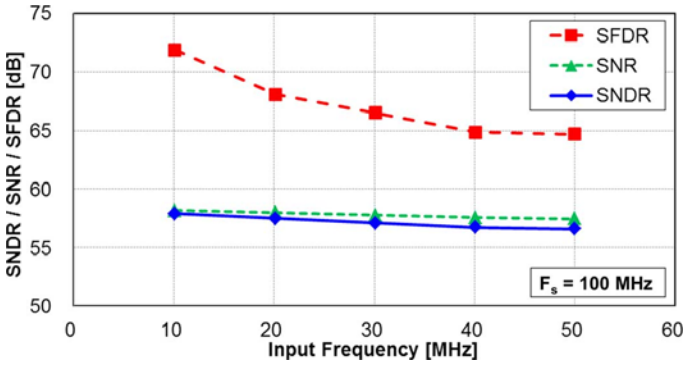

Fig. 23. Measured SFDR, SNR, and SNDR versus input frequency.

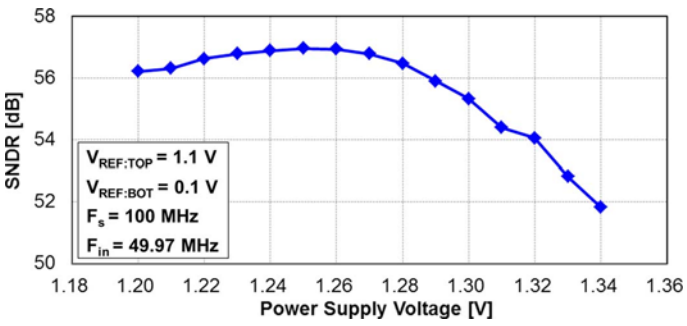

Fig. 25. Measured SNDR versus analog power supply.

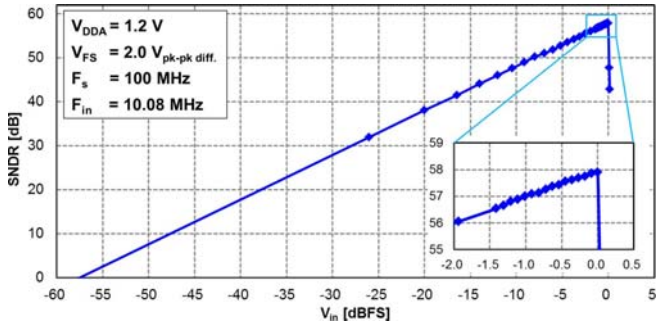

Fig. 24. Measured SNDR versus input amplitude.

1.33 mW is consumed by the clock generator and the ring amplifier dynamic power consumption.

Table II compares the performance of the prototype ADC with conventional ring amplifier based ADCs. This work achieves a three times better FoM (with Nyquist frequency input) than [9] which uses the same 1.5 b/stage ADC structure. In addition, the FoM of the prototype ADC is better than or comparable to more energy effective structured ADCs [8], [11]. These results show the effectiveness of the self-bias ring amplifier.

Fig. 26 compares the FOM with pipeline ADCs presented at ISSCC (1997–2015) and the VLSI Symposium (1997–2014) [18]. The FOMs of [8] and [9] are updated with the Nyquist frequency input values for a fair comparison. Excluding the SAR-assisted pipeline ADCs which have a more efficient hybrid SAR and pipeline ADC architecture [19], this work has a state-of-the-art FOM among the pipeline ADCs.

VII. Conclusion

This paper describes a self-biased ring amplifier. The elimination of external biasing makes the ring amplifier more practical

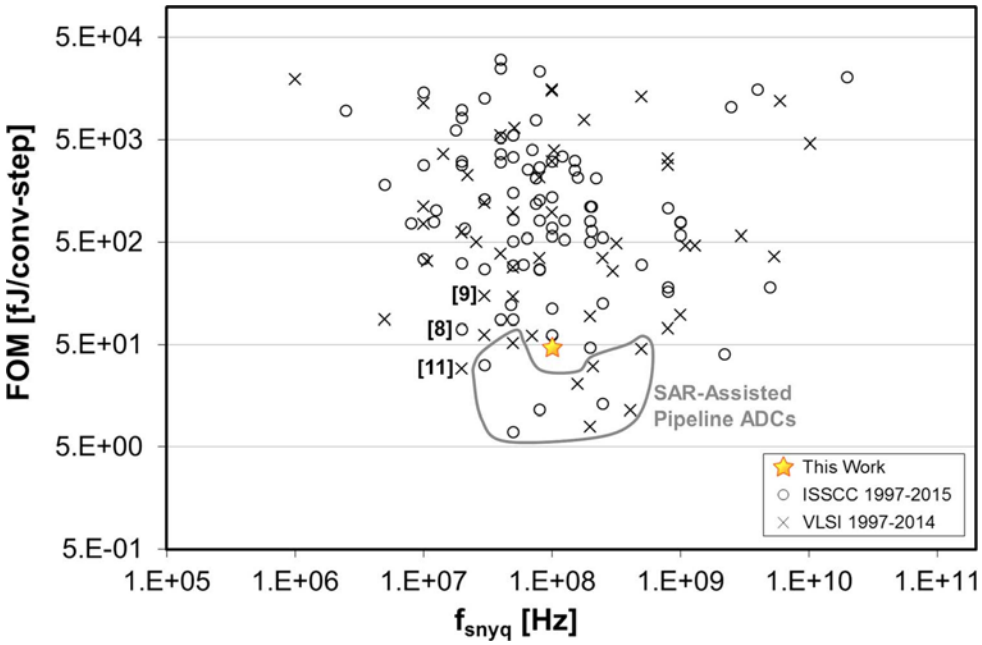

Fig. 26. FOM comparison with pipeline ADCs presented at ISSCC 1997–2015 and VLSI 1997–2014 [18].

TABLE II
PERFORMANCE COMPARISON WITH THE CONVENTIONAL RING AMPLIFIER BASED ADCS

		This Work	VLSI 2012 [9]	ISSCC 2012 [8]	VLSI 2013 [11]
Resolution		10.5 bit	10.5 bit	15 bit	15 bit
Sampling Rate		100 MSPS	30 MSPS	20 MSPS	20 MSPS
ADC Architecture		1.5b/stage	1.5b/stage	3b/stage	3b/stage
Amp. Structure		Self-biased ring amp only	Ring amp only	Ring amp + split-CLS	Coarse + fine ring amplifier
Technology		65 nm CMOS	180 nm CMOS	180 nm CMOS	180 nm CMOS
Active Area		0.097 mm^2	0.50 mm^2	1.98 mm^2	1.98 mm^2
Peak result	**ENOB**	9.33 bit	9.9 bit	12.5 bit	12.3 bit
Nyquist freq.	**ENOB**	9.11 bit	~9.18 bit (from JSSC 2012 [10] graph)	~11.83 bit (from JSSC 2012 [10] graph)	-
Total Power		2.46 mW	2.6 mW	5.1 mW	2.96 mW
FoM (peak result)		38.4 fJ/conv-step	90 fJ/conv-step	45 fJ/conv-step	29 fJ/conv-step
FoM (Nyquist freq. input)		44.5 fJ/conv-step	149.4 fJ/conv-step	70 fJ/conv-step	-

and power efficient while keeping the benefits of the conventional ring amplifier, such as slew based charging and a near rail-to-rail output swing. The use of high threshold voltage devices for the last-stage inverter and simple resistor-based dynamic biasing in the second stage facilitate a single inverter second stage and the elimination of external biasing. In addition, an improved auto-zero scheme eliminates the gain error caused by the parasitic capacitor of the auto-zero switch. The ring amplifiers function as continuous time comparators for the sub-ADCs. Thanks to these techniques, the prototype ADC achieves 56.6 dB SNDR for a Nyquist frequency input, sampled at 100 MS/s, and consumes only 2.46 mW.

APPENDIX
RING AMPLIFIER GAIN CONSIDERATIONS

The ring amplifier has high gain, thanks to its three stages. One might argue that the dead- zone voltage (V_{OS} in this paper) determines the gain of the ring amplifier. Indeed, [10] analyzes the error of the virtual ground (i.e., the inverse of the ring amplifier gain) is defined as $|V_{OS}/A_1|$, where A_1 is the gain of the first stage inverter. The dead-zone approximation is based on the assumption that the last stage transistors become ideal on/off current sources. In practice, all three stages contribute to the gain of the ring amplifier because the last stage still conducts sub-threshold current in steady-state condition and acts as inverter having low bandwidth. Fig. 27 plots the simulated ring amplifier small signal gain and effective gain from a SC amplifier configuration versus the embedded offset, V_{OS}. The conceptual ring amplifier in Fig. 2 (without first stage offset cancelation) is used for this simulation. The effective ring amplifier gain is back calculated from the gain error of the SC amplifier in Fig. 19.

As shown in Fig. 27, the effective gain of the ring amplifier tracks the small signal gain of the ring amplifier when there

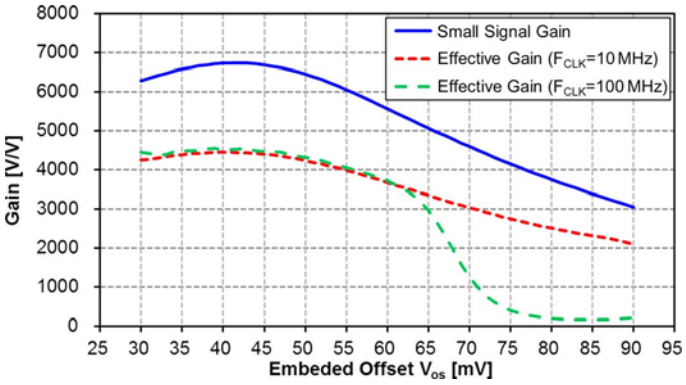

Fig. 27. Simulated ring amplifier small signal gain and the effective ring amplifier gain calculated from the gain error of Fig. 19 MDAC gain stage with various embedded offset voltage V_{OS}. The effective gain is simulated at two different clock frequencies of 10 MHz and 100 MHz to separate the insufficient settling time caused gain error from the gain error due to the finite ring amplifier gain.

is a sufficient settling time (i.e., with a slow clock frequency, 10 MHz for this simulation). Here, the gain reduction between the small signal gain and the effective gain is caused by capacitive divider formed by the offset storage capacitor, $C_{C,}$ and the first stage input capacitance and the common mode feedback capacitor. With a faster clock frequency (100 MHz), the effective gain of the ring amplifier drops steeply as V_{OS} increases when V_{OS} is higher than 65 mV. This drop in effective gain is because the bandwidth of the ring amplifier is not sufficient to settle for the given operating frequency, and not because the error is proportional to V_{OS}. The gain of the ring amplifier falls if V_{OS} is increased over 40 mV because the gain of second stage inverter falls as one of the transistors in the second stage inverter starts operating in the triode region.

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