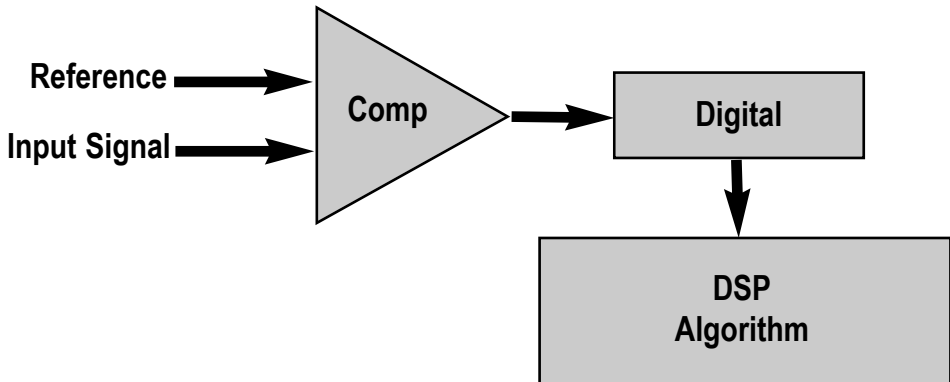

Very-Low-Power Analog-Digital Conversion for Low-Power Wireless Transceivers

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Block diagram of the ADC.

Reducing the power consumption and chip area of analog-to-digital converters is a big challenge in today's research since analog-to-digital converters are key building blocks in all communication, sensing, and imaging systems. As CMOS dimensions scale down, the time-domain resolution of digital signals improves, but the voltage resolution of analog signals degrades. In this work, to be presented at *ISSCC '09*, we introduce a new ADC architecture based on Pulse Position Modulation (PPM), which relies more on time resolution than on amplitude resolution.

A prototype was fabricated in 90nm digital CMOS and occupies 0.06mm². The analog circuits run off a 1V supply and the digital blocks operate at near-threshold from a 400mV supply. The input signal bandwidth is 300KHz and the measured ENOB is 7.9 bits for $F_s=1\text{MHz}$, over the entire bandwidth. The measured power consumption of the entire system is 14 μW (excluding digital post-processing). The figure of merit is 98fJ per conversion-step. This project is supported by the Engineering Research Centers Program of the National Science Foundation under Award Number EEC-9986866 and in part by National Semiconductor.
