A Regenerative Comparator Structure With Integrated Inductors

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***Abstract*—We employ on-chip inductors to improve the sampling speed and power consumption of regenerative comparators. Since these inductors are far smaller than those used in typical RF designs, the addition of inductors has little impact on area. Simulations based on accurate inductor models indicate more than a doubling of comparator sampling speed for a given power consumption, or a halving in power consumption for a given sampling speed. We present a detailed analysis of the new scheme. The technique is verified with test measurements of 16 comparators, implemented in 0.18-μm digital CMOS, sampling at 3.84 GHz.**

***Index Terms*—Flash analog-to-digital converter, monolithic inductor, regenerative comparator, regenerative time constant.**

I. Introduction

COMPARATORS are used in analog-to-digital converters (ADCs), data transmission, switching power regulators, and many other applications [1]. Sampling speed and power consumption are key metrics in comparator design. Although the sampling speed and the power consumption of comparators continue to improve as transistor gate length decreases, performance improvements for a given technology are difficult to attain. For example, in 0.18-μm CMOS, a sampling frequency above 2 GHz is difficult to achieve [2]–[4]. This is because the speed of a regenerative comparator strongly depends on gate length and is ultimately related to the transistor f_t [1]. In a regenerative comparator, the ratio of the transconductance of the cross-coupled transistors to the parasitic capacitance determines speed. For a given CMOS technology, alternative circuit techniques, such as time-interleaving, are required to further increase sampling speed. With time-interleaving, parallel comparators running with offset clocks are employed to increase the overall sampling rate. However, time-interleaving requires multiple, accurately-spaced clocks, and furthermore mismatches in interleaved comparators can cause distortion and spurious tones [5].

We present a method that improves comparison speed for a given power consumption, in a given CMOS technology. Alternatively, this technique can be used to reduce power consumption for a given sampling speed. In Section II, we review regenerative CMOS comparators, focusing on time constant analysis.

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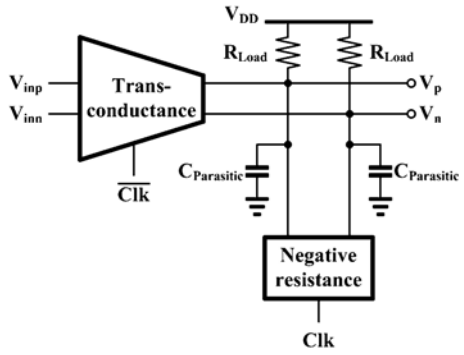

Fig. 1. Regenerative comparator.

Section III presents a circuit technique that employs inductors to reduce the time constant of comparison. We discuss the practical implementation of inductors in a comparator in Section IV. Simulation data presented in Section V verify the improvement in power consumption and speed. We present measurement of the performance of prototype comparators in Section VI.

II. Background

As shown in Fig. 1, most comparators have two components: a preamplifier, formed by the combination of a transconductance and a load resistance $(R_{\rm Load})$, and a regenerative latch, formed by the combination of a negative resistance (usually implemented with cross-coupled transistors) and a load resistance. In the figure, $V_{\rm inp}$ and $V_{\rm inn}$ are the differential inputs and V_p and V_n are the differential output signals. The operation of the comparator is controlled by the complementary clocks $\rm Clk$ and $\overline{\rm Clk}$. While $\rm Clk$ is low, the comparator is in *tracking* mode. During this phase, the latch is disabled, and the transconductance of the preamplifier is enabled. The preamplifier amplifies the difference between the input signals (i.e., $V_{\rm inp} - V_{\rm inn}$) so that the output voltage difference (i.e., V_p-V_n) tracks the input signal. When $\rm Clk$ goes high, the preamplifier is disabled, preventing the analog input from further influencing the comparison. Instead, the negative resistance is enabled, forming a regenerative circuit that amplifies V_p and V_n to digital logic levels (*latching*). At the beginning of the next cycle, $\rm Clk$ returns low. The preamplifier removes any memory of the latched output (*reset*) from the previous cycle and tracking begins again.

Pre-amplification has some important benefits. The preamplifier attenuates kickback noise. In addition, the input-referred offset of the latch is reduced by the gain of the preamplifier. The gain of the preamplifier also decreases the probability of metastability [6], [7]. However, for comparators operating with multi-gigahertz sampling frequencies, a low preamplifier gain

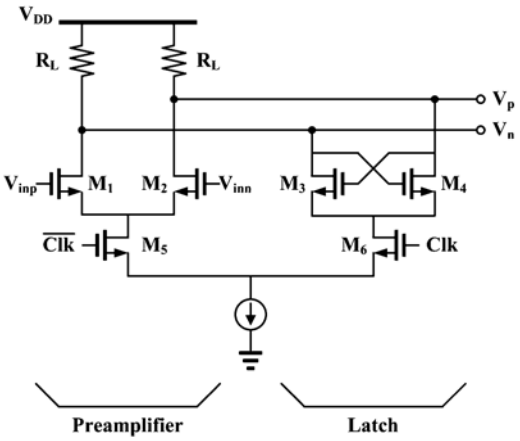

Fig. 2. Regenerative comparator for analysis.

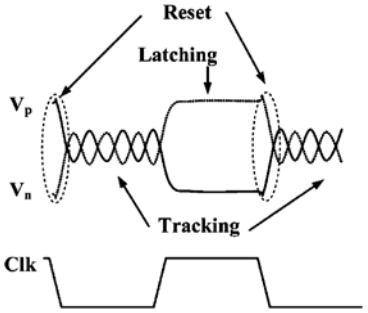

Fig. 3. Waveforms during tracking, latching, and reset.

is preferred, so that a large bandwidth can be assigned to the preamplifier. For example, the comparator in [8] has a preamplifier gain of 3.

We base our analysis on the regenerative comparator shown in Fig. 2. Transistors M_{1-2} provide the transconductance of the preamplifier, while the cross-coupled transistors M_{3-4} generate negative resistance during the latching phase. We base our explanation on this comparator, but our analysis is applicable to any comparator, similar in structure, to that shown in Fig. 1. Fig. 3 shows typical output voltage waveforms (i.e., V_p and V_n) during the operation of the preamplifier (*reset* and *tracking*) and during latching.

We now use small-signal analysis to estimate the speed of the comparator. First, the time constant of the preamplifier is derived. Once the latch is disabled, the preamplifier clears the differential voltage at the output nodes from the previous latching phase, and the output begins to track the input signal. We use the simple small-signal model shown in Fig. 4 to model the preamplifier phase. In the figure, g_{m_in} is the transconductance of the input transistors M_{1-2}, and R and C represent the total resistance and capacitance at the output nodes during the preamplifier operation. The output voltages V_p and V_n satisfy

$$g_{m\_in} \cdot V_{inn} + \frac{V_p}{R} + C\frac{dV_p}{dt} = 0$$
$$g_{m\_in} \cdot V_{inp} + \frac{V_n}{R} + C\frac{dV_n}{dt} = 0. \quad (1)$$

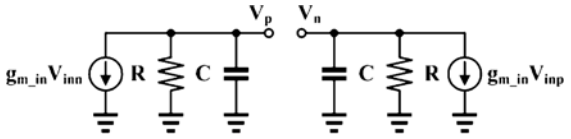

Fig. 4. Small-signal model of comparator in the preamplifier phase.

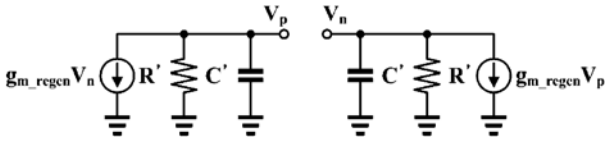

Fig. 5. Small-signal model of the comparator in the latching phase.

The output difference voltage $V_{\text{diff}} = V_p - V_n$ is given by

$$V_{\text{diff}}(t) = V_{\text{pre\_initial}} \cdot e^{-t/\tau_{\text{pre}}} + g_{m\_} \cdot \cdots \quad (2)$$

where the time constant of the preamplifier τ_{pre} is given by $\tau_{\text{pre}} = RC$. The initial condition $V_{\text{pre\_initial}}$ is the final differential output voltage at the end of the *previous* latching phase. The first term in (2) represents the *reset* process, whereas, the second term is related to *tracking*. We see that a smaller τ_{pre} leads both to faster *reset* and *tracking*.

Fig. 5 shows the small-signal model of the comparator in the latching phase. In the figure, g_{m_regen} is the transconductance of the cross-coupled nMOS transistors (M_{3-4}). R' and C' represent the total resistance and capacitance at output nodes during latching. The output voltages V_p and V_n satisfy

$$g_{m\_\text{regen}} \cdot V_n + \frac{V_p}{R'} + C'\frac{dV_p}{dt} = 0$$
$$g_{m\_\text{regen}} \cdot V_p + \frac{V_n}{R'} + C'\frac{dV_n}{dt} = 0. \quad (3)$$

Solving for $V_{\text{diff}} = V_p - V_n$, we get

$$V_{\text{diff}}(t) = V_{\text{latch\_initial}} \cdot e^{t/\tau_{\text{regen}}} \quad (4)$$

where the regeneration time constant τ_{regen} is given by

$$\tau_{\text{regen}} = \frac{C'}{g_{m\_\text{regen}} - \frac{1}{R'}}. \quad (5)$$

The initial condition $V_{\text{latch\_initial}}$ is the final output voltage at the end of the preamplifier phase. We see that V_{diff} grows exponentially if g_{m_regen} is greater than $1/R$ (i.e., making τ_{regen} positive). Although this analysis is valid only for small signals, it does give us a reasonable estimate of latching speed.

From (4), we see that a large output voltage at the end of tracking ($V_{\text{latch\_initial}}$) is preferred. On the other hand, the gain of the preamplifier is limited because of the preamplifier gain-bandwidth tradeoff. For a given capacitance C', increasing g_{m_regen} reduces the regeneration time constant τ_{regen} from (5). g_{m_regen} can be increased either by using wider transistors or by using larger bias currents. However, increasing transistor

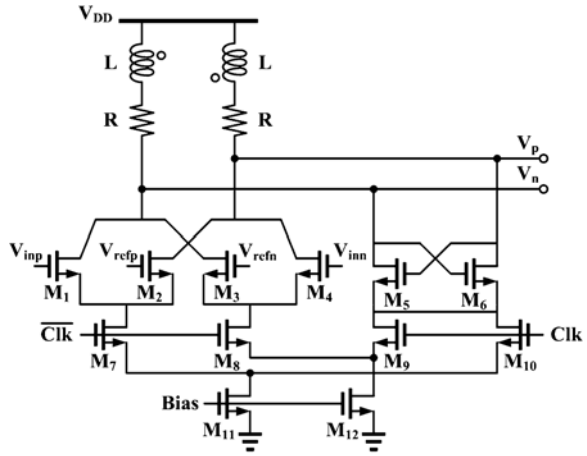

Fig. 6. Proposed comparator.

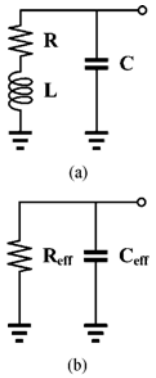

Fig. 7. Concept of effective resistance and capacitance. (a) The output load. (b) Equivalent load formed with R_{eff} and C_{eff}.

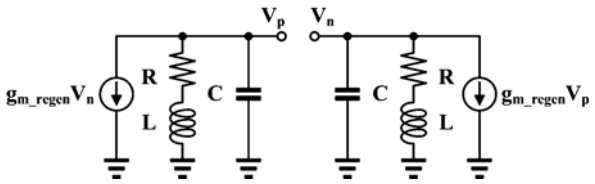

Fig. 8. Simplified small-signal model (latching) with inductance L.

width also increases parasitic capacitance, so that ultimately an increase in speed requires additional power consumption. The next section describes a technique that decreases regenerative time constant τ_{regen} without increasing power consumption. This is achieved with the help of inductors.

III. New Comparator Structure

A. Addition of Inductors

We introduce inductors both to increase the bandwidth of the preamplifier and to reduce the regenerative time constant τ_{regen}. The new comparator structure is shown in Fig. 6. The load resistor R_L is replaced by a combination of a resistor R and an inductor L. Inductors have been used for bandwidth extension in continuous-time circuits, such as amplifiers [9]. However, we show that inductors can be used in comparators to improve both tracking and latching speed.

B. Qualitative Analysis

To understand how this scheme works, we first study the effective resistance and capacitance of the load. Fig. 7(a) shows the load of the proposed comparator, comprising of resistor R, series inductor L, and a parasitic capacitance C. In Fig. 7(b), we model the entire load as a parallel combination of a resistance R_{eff} and a capacitance C_{eff}. In (6), we calculate the total admittance (Y) of the load and then derive expressions in (7) and (8) for R_{eff} and C_{eff} in terms of R, L, C, and frequency ω

$$Y = \frac{1}{R + j\omega L} + j\omega C = \frac{1}{R_{\text{eff}}} + j\omega C_{\text{eff}} \tag{6}$$

where

$$R_{\text{eff}} = R + \frac{\omega^2 L^2}{R} \tag{7}$$

and

$$C_{\text{eff}} = C - \frac{L}{R^2 + \omega^2 L^2}. \tag{8}$$

Thanks to the introduction of inductance L, R_{eff} is increased and C_{eff} is decreased, reducing the regeneration time constant τ_{regen}. [Please refer to (5) for the regeneration time constant equation.]

If L is too large, the effective reactance becomes *inductive*, instead of *capacitive*. In (8), C_{eff} becomes negative if the inductance L is large. If the effective capacitance is negative, then the overall load behaves as an *RL load* (a resistor and an inductor). The regenerative circuit becomes an oscillator if the capacitance is exactly cancelled (i.e., $C_{\text{eff}} = 0$). However, oscillation only occurs with a large value of inductance,[1] and in practice the inductor itself contains significant parasitic capacitance, further reducing the risk of oscillation.

C. Regenerative Time Constant

The concept of the equivalent resistance and capacitance (R_{eff} and C_{eff}) gives us a good intuitive understanding of how the introduction of inductors improves latching speed. However, it is not straightforward to calculate R_{eff} and C_{eff} since (7) and (8) require an estimate of frequency ω. For more quantitative analysis, we model the comparator in the s domain. Fig. 8 shows a simplified small-signal model of the comparator in the latching phase. This model includes the transconductance of the cross-coupled devices and the added inductance L. From this small-signal model, the output voltage difference $V_{\text{diff}}(= V_p - V_n)$ satisfies

$$-g_{m\_\text{regen}} \cdot V_{\text{diff}}(s) + \frac{V_{\text{diff}}(s)}{R + sL} + sC \cdot V_{\text{diff}}(s) = 0. \tag{9}$$

[1]From (8), $C_{\text{eff}} > C - L/R^2$. As an example, if $R = 1000\ \Omega$, then L (in nanohenry) must be greater than C (in femtofarad) for C_{eff} to be negative.

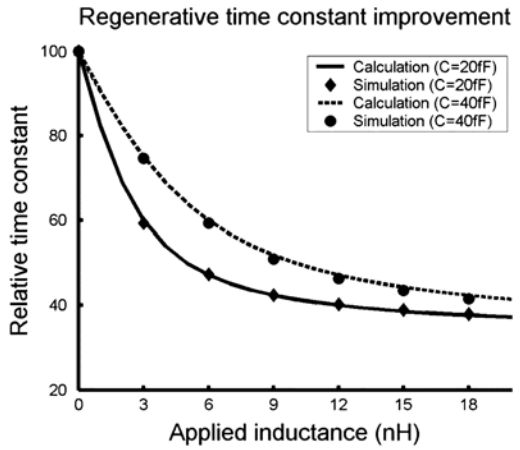

Fig. 9. Regeneration time constant improvement versus inductance for two values of capacitance (20 and 40 fF). The solid/dotted lines show the estimated regeneration time constant [$1/s_1$ from (12)], while the discrete points are derived from simulations of circuit shown in Fig. 8.

Rearranging (9), we get a quadratic equation

$$(s^2+\alpha s+\beta)\cdot V_{\text{diff}}(s)=0, \text{ with}$$
$$\alpha=\frac{R}{L}-\frac{g_{m\_\text{regen}}}{C}$$
$$\beta=\frac{1-g_{m\_\text{regen}}\cdot R}{LC}. \quad (10)$$

From (5), we know that $g_{m\_\text{regen}}R$ must be greater than 1 for the latch to function, and therefore, β is negative. Since any quadratic equation of the form $s^2+\alpha s+\beta=0'$ with real α and negative β has one positive real root and one negative real root, we let the two roots of the quadratic equation be positive s_1 and negative s_2. From (10), V_{diff} in the time domain is given by

$$V_{\text{diff}}(t)=B_1\cdot e^{s_1 t}+B_2\cdot e^{s_2 t} \quad (11)$$

where the constants B_1 and B_2 are determined by the initial conditions of V_{diff} and its derivative. Since s_2 is negative, the second term in (11) decays as latching proceeds. $1/s_1$ is the new regeneration time constant and from the quadratic equations s_1 is given by

$$s_1=\frac{1}{2}\left[\frac{\left(\frac{g_{m\_\text{regen}}}{C}-\frac{R}{L}\right)+}{\sqrt{\left(\frac{g_{m\_\text{regen}}}{C}-\frac{R}{L}\right)^2+4\left(\frac{g_{m\_\text{regen}}\cdot R-1}{LC}\right)}}\right]. \quad (12)$$

In Fig. 9, we plot (solid/dotted lines) the new regenerative time constant $\tau_{\text{regen}}(=1/s_1)$ versus inductance, for capacitance values of 20 fF and 40 fF. In these plots, we normalize the time constant to that of a similar comparator without inductors. We assume $R=500\ \Omega, g_{m\_\text{regen}}=3$ mA/V, and ignore the output resistance of transistors. The time constants predicted by Spectre simulations are overlaid on the plots in Fig. 9 (discrete points). These simulations indicate that the estimate of time constant $(1/s_1)$ very accurately predicts the improvement in performance.

From Fig. 9, we see that we can achieve significant improvements in comparator performance with practical values of on-chip inductance. For example, with $C=20$ fF and $L=18$ nH, the regeneration time constant is reduced by 62%. This allows a 163% increase in sampling speed, with the same probability of metastability [6], [7] and without an increase in power dissipation. In practice, the inductor itself also introduces parasitics. However, we see in Section V, that even when the parasitics of a practical inductor are considered, we still achieve very significant reductions in the regeneration time constant. We note that since τ_{regen} falls continuously as inductance increases, an exact inductance value is not needed[2] This technique becomes more attractive as feature sizes shrink: since the parasitic capacitances become smaller, we see from Fig. 9 that a smaller inductance is required for the same improvement in regeneration time constant.

For a given sampling speed, power consumption is reduced with the addition of inductors. Thanks to the inductors, the transconductance of the cross-coupled transistors required to achieve a given regeneration time constant can be smaller, so that a smaller bias current is sufficient. The probability of metastability is reduced for a given sampling speed, since this probability decreases exponentially with reduction in the regenerative time constant [6], [7].

Two prototype comparators, one designed for improved speed and the other designed for improved power consumption are discussed in Section V.

IV. Inductor Design

When monolithic inductors are used in RF circuits, for example, in a low-noise amplifier (LNA) [10] or in a voltage-controlled oscillator (VCO) [11], the design goals are to achieve a certain inductance value and a high quality factor (i.e., a small series parasitic resistance). The skin effect, proximity effects [12], eddy currents [11], and substrate loss all degrade the quality factor. Eddy currents generate nonuniform current flow in the inner turns, and this usually mandates a relatively large, hollow center in the inductor. To reduce these effects, monolithic inductors tend to be large, typically two orders of magnitude larger than neighboring transistors. Area is a major consideration when the comparators are used in a flash ADC. As an example, we consider the addition of two 11-nH inductors to each comparator. If we adopt a conventional RF inductor structure (e.g., 10-μm metal trace width, 5-μm metal trace spacing, and 30% hollow center area), simulations indicate that the overall diameter of a 7 turn inductor is 290 μm. The two inductors alone would occupy 0.17 mm^2, a far larger area than that of a typical comparator.

The required area can be dramatically reduced by considering the required characteristics of the inductor, in particular parasitic resistance. In the proposed comparator, the inductor is connected in series with the load resistance. We can tolerate a large inductor parasitic, if this parasitic resistance is considered as part of the load resistor. For example, if a 1-kΩ load resistance is required and if the inductor has a parasitic resistance of 500 Ω, then a 500-Ω load resistor in series with the 500-Ω parasitic

[2]Using a larger inductance is better for a bigger ratio of latching speed to power consumption. However, the inductance is limited by: a) the available area; b) the self-resonant frequency and c) the output voltage ringing during the reset phase due to under-damped behavior of the output load.

resistance functions in a similar way [9].[3] Since the parasitic resistance does not need to be minimized, a narrow metal width can be used.

The use of thinner metal lines in the inductor has significant benefits. The self-resonant frequency is increased, since a reduction in inductor area also reduces the parasitic capacitance between the inductor and the substrate. Simulations indicate a much higher self-resonant frequency than the targeted low-gigahertz sampling frequencies. A stacked inductor structure can be used to further reduce layout area. Since the self-resonant frequency is very high, the reduction in self resonant frequency due to stacking is not an issue. For a given area, a stacked inductor, comprised of two metal winding layers in series, exhibits four times more inductance than an inductor built with single metal layer [13].

V. Performance Comparison

To validate the ideas presented in Sections III and Section IV, three prototype comparators (COMP I, II, and III) are designed in 6-metal 0.18-μm digital CMOS. A reference design COMP I does not incorporate inductors. COMP II incorporates an inductor load, but is designed to have the same power consumption as COMP I. COMP III has the same inductor load as COMP II, but runs with half the bias current (i.e., half the power consumption). P-type poly-silicon is used to implement load resistors. The values of the load resistors are chosen so that each preamplifier has the same low-frequency voltage gain.

A stacked inductor is formed with the second (M2) and fifth metal (M5) layers. We choose these metal layers to maximize the self-resonant frequency. Fifteen turns of metal width 0.3 μm and metal spacing 0.3 μm, gives an overall inductor size of 30 μm by 30 μm. The simulated inductance, series resistance, and self resonant frequency are 18.0 nH, 661 Ω, and 8.4 GHz, respectively. The inductor occupies around 1% of the area of a typical RF inductor of the same inductance value.

We use Spectre simulations, including extracted parasitics, to compare the performance of the three comparators. A dummy load capacitance of 4 fF is connected at the output nodes to represent the input capacitance of the next stage. Two overdrive tests with the input frequency set at the Nyquist frequency are performed. Fig. 10(a) shows the clock signal, while Fig. 10(b) and (c) shows the input voltage waveforms for the two overdrive tests. With the input waveforms of Fig. 10(b), the output of the comparator should not change. On the other hand, with the inputs shown in Fig. 10(c), the comparator output should alternate between 0 and 1. The minimum clock periods for which COMP I, COMP II, and COMP III pass both overdrive tests are shown in Table I. Although COMP I and COMP II have the same power consumption, COMP II is 2.6 times faster than COMP I. COMP I and COMP III have the same maximum operating frequency, but the power dissipation of COMP III is halved thanks to the introduction of the inductors.

We also use Spectre simulations to estimate the time constants of the preamplifier phase and of the latching phase. In these simulations, the sampling frequency is 1 GHz and the comparator input is a 500-MHz differential pulse train. Table I summarizes the time constants of the preamplifiers and of the latches. With the same power consumption, COMP II requires much less time for regeneration than COMP I. The regeneration time constant $\tau_{\rm regen}$ of COMP III is smaller than that of COMP I, indicating that the same latching speed can be achieved with less than half the power consumption. COMP II has roughly the same preamplifier time constant ($\tau_{\rm pre}$) as COMP I. COMP III has a larger preamplifier time constant because a larger load resistance is required to achieve the same preamplifier voltage gain at dc. ($\tau_{\rm pre}$ is proportional to the output resistance.)

We now consider a "figure of merit" that incorporates power consumption (*power*), the maximum sampling frequency at which the comparator passes the overdrive tests ($f_{\rm ms}$), and the probability of metastability (P_m).The proposed figure of merit F_c for a comparator is given by

$$F_c = \frac{f_{\rm ms}}{\rm power} \cdot \log_e \frac{1}{P_m} (\text{samples/joule}). \tag{13}$$

[3]In [9], the inductor parasitic resistance is used as part of the load resistance in an inductively peaked amplifier.

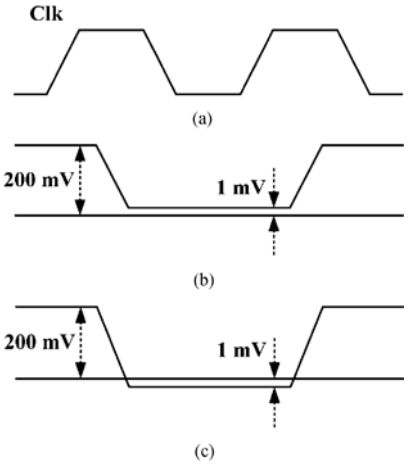

Fig. 10. Overdrive tests. (a) Clock waveform. (b) Nonoverlapping input waveforms. (c) Overlapping input waveforms.

TABLE I
Summary Of Comparator Performances (Simulation)

Comparator	Minimum clock period	$\tau_{\rm regen}$	$\tau_{\rm pre}$	F_c
COMP I	650 ps	55 ps	38 ps	1
COMP II	250 ps	33 ps	36 ps	7.8
COMP III	650 ps	41 ps	62 ps	3.3

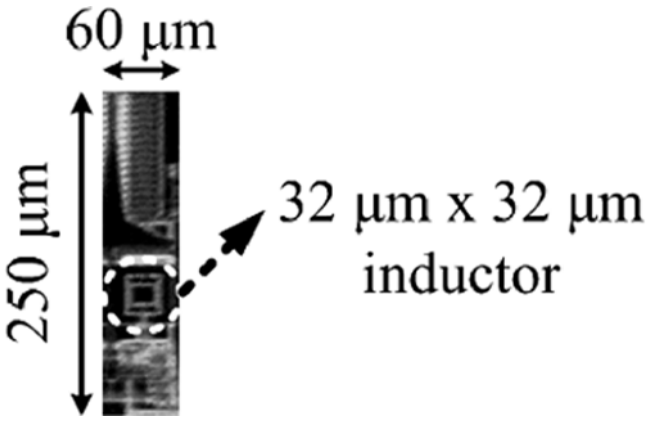

Fig. 11. Die photo of the comparator.

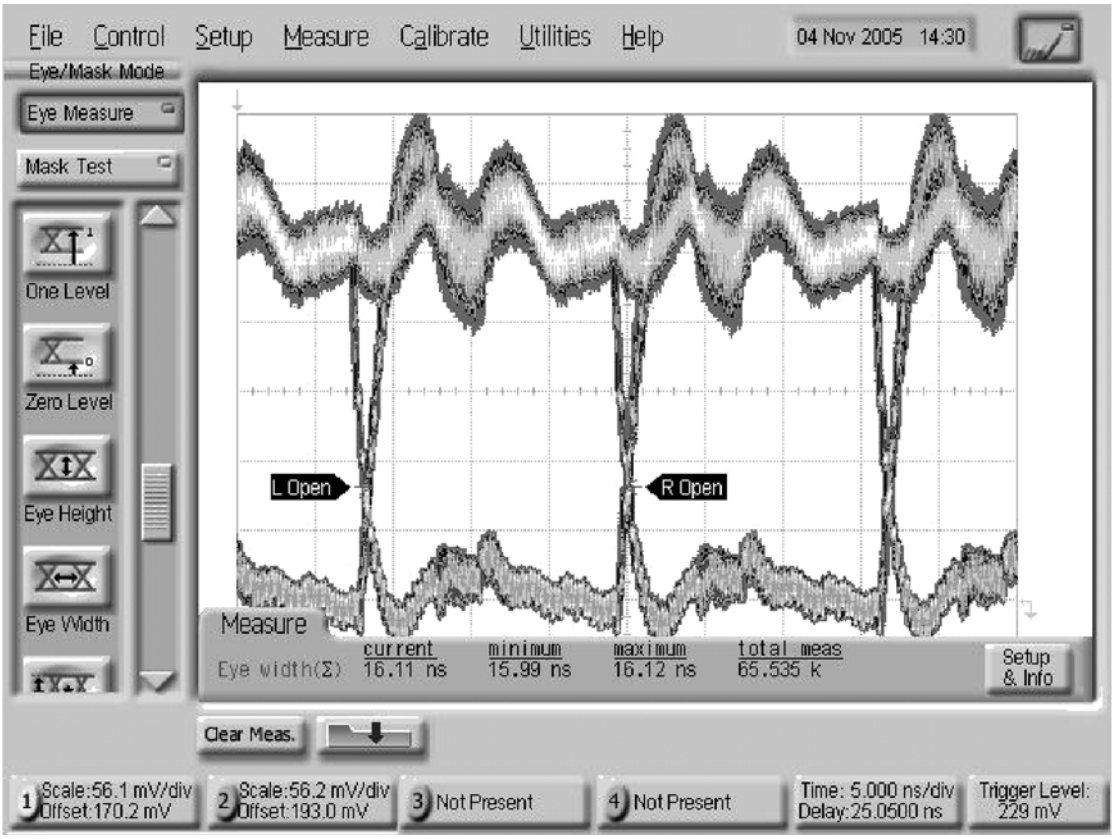

Fig. 12. Eye diagram of the comparator output.

The natural log is used to prevent P_m from being over-stated. The relative values of the figure of merit, F_c, for COMP I, COMP II, and COMP III, are summarized in Table I, quantitatively showing the benefits of the inductor load.[4]

VI. Measurement Results

A prototype comparator with a differential inductor was fabricated in 0.18-μm digital CMOS. Fig. 11 shows a die photo of a single comparator. Fig. 12 shows an eye diagram of a comparator output recorded during 16.2 hours continuous operation. We use a sampling frequency of 3.84 GHz and the sinusoidal analog input frequency of 1.9 GHz ($= 2027/4096{*}3.84$ GHz), that is close to the Nyquist frequency. This choice of frequency is made to achieve coherent sampling [15]. Thanks to coherent sampling, the input voltage to the comparator, at the sampling instant, can have almost any voltage value, over a range equivalent to the peak-to-peak amplitude of the sinusoidal input, and can be arbitrarily small. The comparator's output is decimated by 64, and then buffered to facilitate testing of the prototype. With a 1/64 decimation rate, a metastability error rate of less than $2.9{*}10^{-13}$ is indicated.

Fig. 13 shows the measurement of the overdrive test and Fig. 13(a) explains the methodology used for this measurement. We apply a differential reference voltage $V_{\rm ref}$ (i.e., $V_{\rm refp}$ - $V_{\rm refn}$ in Fig. 6) of 206 mV, and a sinusoidal input with an amplitude $V_{\rm in}$ (i.e., $V_{\rm inp}$ - $V_{\rm inn}$ in Fig. 6). For the input amplitude greater than $V_{\rm ref}$, the comparator generates a digital output of "1," and generates "0" for the input amplitude smaller

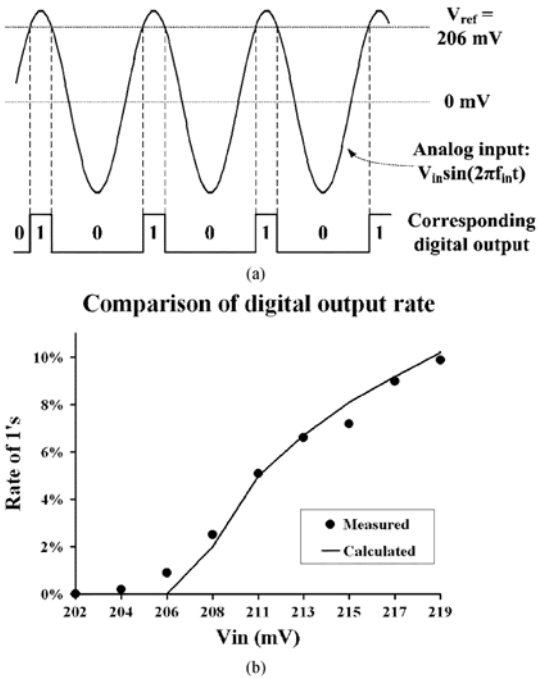

Fig. 13. Overdrive test at 3.2 GS/s with 1.584-GHz input frequency. (a) Analog input and reference. (b) Comparison of measured rate of 1's with that predicted from calculation.

[4] P_m from [14] is used. (A_0 : low-frequency small-signal gain of preamplifier, T_C : allowed time for regeneration)

TABLE II
SUMMARY OF THE COMPARATOR (FABRICATED)

Merit	Value
Maximum sampling frequency	3.84 GHz
Power consumption	1.85 mW (1.8 V × 1.028 mA)
Differential inductor area	32 μm × 32 μm, (10 turns, metal width = 0.4 μm*)
Inductor parameters (simulated)	11.88 nH, 203 Ω, Q = 0.68 (at 4 GHz)
Comparator input capacitance	30 fF
Comparator offset	Minimum: -19 mV, maximum: 28 mV standard deviation : 14.8 mV
M_{1-4} **	10 μm/0.18 μm
M_{5-6}**	6 μm/0.18 μm
M_{7-10}**	4 μm/0.18 μm
R**	1 KΩ

* Metal width is limited by the lith ography limitations.
** See Fig. 6.

than V_{ref}. As the amplitude of the input sinusoid is increased, the differential input signal amplitude becomes greater than the differential reference for a larger duty cycle, increasing the expected number of 1's. To evaluate the overdrive test result at the Nyquist rate, we count the number of output 1's over 4096 samples. We use a 3.2-GHz sampling frequency and a 1.584-GHz ($= 2027/4096^{*}$ 3.2-GHz) input frequency. Fig. 13(b) compares the measured rate of 1's, with what is predicted for an ideal comparator. In this calculation, we incorporate the measured 4-mV input offset of the comparator. We see that the comparator performs very accurately with only a small deviation from the calculation.

Table II summarizes performances of the comparator, and gives the transistor sizes, load resistance, and information about the inductor. We implement the inductor as a differential inductor, comprised of two metal layers in series (M2 and M5).

VII. CONCLUSION

A technique which improves the speed of regenerative comparators, without increasing power consumption, is presented. The technique is applicable to all types of regenerative comparators with resistive loads. The introduction of an inductor reduces the effective load capacitance, significantly improving latching speed. The technique does not require an exact value of inductance. Both power consumption and the probability of metastability are reduced. The technique becomes more beneficial as gate lengths shrink, since the same relative improvement can be achieved with a smaller inductance. Since parasitic resistance does not need to be minimized, the inductors occupy far less area than those typically used in RF design. We estimate that these inductors require around 1% of the area of those of the same inductance in a typical RF design. Simulations based on extracted layout data and accurate models of practical on-chip inductors show that the use of inductor loads leads to more than a factor-of-two improvement in sampling rate or alternatively a halving of comparator power consumption. Measurements of a prototype comparator implemented in 0.18-μm CMOS show that the proposed comparator structure achieves a maximum sampling speed over 3 GHz.

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