A 9-bit, 14 μW and 0.06 mm^2 Pulse Position Modulation ADC in 90 nm Digital CMOS

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***Abstract*—This work presents a compact, low-power, time-based architecture for nanometer-scale CMOS analog-to-digital conversion. A pulse position modulation ADC architecture is proposed and a prototype 9 bit PPM ADC incorporating a two-step TDC scheme is presented as proof of concept. The 0.06 mm^2 prototype is implemented in 90 nm CMOS and achieves 7.9 effective bits across the entire input bandwidth and dissipates 14 μW at 1 MS/s.**

***Index Terms*—ADC, PPM, TDC.**

I. Introduction

SMALL, low-power analog-to-digital converters (ADCs) have numerous applications in areas ranging from power-aware wireless sensing nodes for environmental monitoring, to biomedical monitoring devices in point-of-care (PoC) instruments. This work presents a compact, low-power, time-based ADC architecture for nanometer-scale CMOS. In addition, for the first time, a fundamental comparison between time-based and voltage-based analog-to-digital conversion is presented. Technology scaling reduces the supply voltage and this limits voltage headroom in amplifier design, reducing signal-to-noise ratio in thermal-noise-limited circuits. Furthermore, short-channel transistors suffer from lower output resistance and lower intrinsic gain. A promising way to overcome the challenges of low-voltage design is to process signals in the time domain [1]–[4]. Despite the reduction in supply voltage, time resolution has improved in nanometer-scale devices thanks to the reduction of gate delay [1]. Hence, time-domain processing potentially offers a better solution for submicron processes.

There are a number of different ADC architectures that quantize time or frequency instead of voltage or current. Low sampling speed is the main disadvantage of slope and integrating ADC architectures [5]. In order to achieve high resolution, the clock frequency must be high, leading to high power consumption. Researchers have recently demonstrated high-speed slope based ADCs which replace the counter with more efficient time-to-digital conversion techniques [6], [7]. Certain asynchronous ADCs [8]–[11] can also be considered as time-based ADCs. In another category of time-based ADCs, a voltage-controlled delay cell converts the input signal voltage to a delay, and a time-to-digital converter digitizes this delay [12], but designing a linear voltage-controlled delay cell with a large dynamic range is a challenging task. The main challenge in the voltage-to-frequency-conversion based ADC architecture [13], [14] is the precision and linearity of voltage-to-frequency conversion.

We present a pulse-position modulation (PPM) architecture. Pulse-position modulation is an elaboration of pulse-width-modulation (PWM) based A/D conversion, first described by Reeves in a 1939 patent [15]. The input signal is first pulse-width modulated and then the width is quantized with a time-to-digital converter (TDC). In our implementation, signal information is converted to a time-domain representation using a ramp generator and a continuous-time comparator and then a two-step TDC converts the time domain information to digital code. The use of a two-step TDC allows us to achieve both high resolution and high dynamic range, with low power consumption. An iterative recovery algorithm processes the output samples to suppress distortion [16], [17]. This recovery technique requires only slight oversampling, increasing the effective input signal bandwidth. Section II introduces the PPM ADC system architecture. The implementation of the main ADC circuit blocks including the ramp generator, comparator, and two-step TDC is described in Section III. Measurements of the prototype device are presented in Section IV.

Appendix I discusses and analyzes the advantages of time-domain signal processing over voltage-based methods for nanometer CMOS analog-to-digital conversion. Our analysis shows that time-to-digital based analog-to-digital conversion is fundamentally more energy efficient for moderate resolution conversion in nanometer CMOS processes.

II. PPM ADC Architecture

A PPM ADC block diagram is depicted in Fig. 1 and Fig. 2 shows some of the key waveforms. The input signal is continuously compared with a voltage ramp. When the input signal and the ramp intersect, the comparator generates a pulse. The time interval between the start of the ramp and the instant the input signal crosses the ramp (i.e., $[t_1, t_2, t_3, \ldots]$) in Fig. 2 is measured by a time-to-digital converter. Assuming the ramp slope is constant, the time vector $[t_1, t_2, t_3, \ldots]$ is proportional to the signal amplitude at the crossover points.

Manuscript received January 11, 2010; revised March 22, 2010; accepted April 01, 2010. Date of current version August 25, 2010. This paper was approved by Associate Editor Kunihiko Iizuka. This work was supported in part by the Wireless Integrated Microsystems Engineering Research Center, National Semiconductor and NSF Career Grant 0346874.

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Digital Object Identifier 10.1109/JSSC.2010.2050945

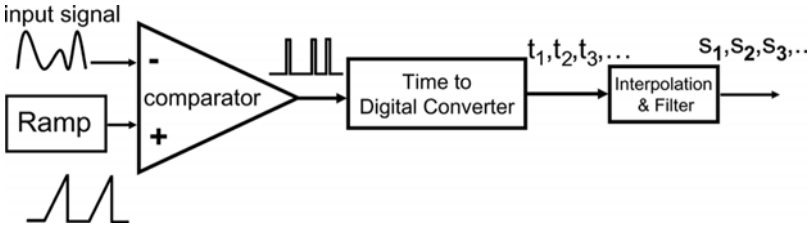

Fig. 1. PPM ADC block diagram.

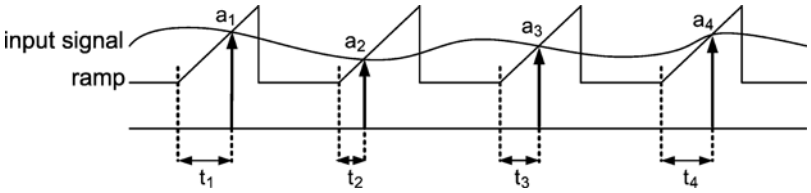

Fig. 2. PPM ADC typical waveforms.

A. ADC Resolution

The ADC resolution is determined by the TDC resolution and the ramp slope. Supposing the ramp is linear from voltage A to voltage B, and assuming the ramp slope is s, the time input range to the TDC is $(B-A)/s$. (As a rule of thumb, a ramp linearity of at least two bits more than the ADC resolution should be targeted.) If the TDC operates with a resolution t_b (i.e., t_b is the LSB in time), ideally we expect an N bit ADC where

$$N = Log_2\left(\frac{B-A}{s \cdot t_b}\right). \tag{1}$$

B. Time-to-Digital Conversion

The TDC architecture is a tradeoff between power consumption and linearity. The TDC in the PPM ADC measures the time intervals, $[t_1, t_2, t_3, \ldots]$, between the start of the ramp and the crossover point of the ramp and the input signal. Although the simplest form of a TDC is a digital counter, a very high counter frequency is required to achieve a high resolution. Delay line circuits [18]–[20] are more energy efficient for time measurement, however, the delay line must be long to measure long periods of time, significantly degrading INL and effective resolution [21]. To achieve both energy efficiency and a large dynamic range, a two-step TDC combining a low frequency counter and a delay line TDC is proposed. The counter is used as the coarse quantizer to span a wide dynamic range and the delay line is employed as a fine quantizer. The delay line resolves the residual error of the counter measurement and helps to achieve high resolution [21]–[23]. The implementation of this TDC is discussed in detail in Section III.

C. Non-Uniform Sampling

In a PPM ADC, measuring $[t_1, t_2, t_3, \ldots]$ results in non-uniform samples of the signal, given as time and amplitude pairs of 's_1-t_1', 's_2-t_2', 's_3-t_3', ...'. Since each sample has an accurate time stamp, the information can be directly applied in many applications. However, if these samples are misinterpreted as uniform, then harmonic distortion is apparent in the output frequency spectrum of the ADC. As an example, the frequency spectrum shown in Fig. 3 is derived assuming the samples are uniform (i.e., a uniform FFT). Low-pass filtering is a straightforward linear technique for constructing uniform samples from non-uniform sample information (Fig. 3). Generally an oversampling ratio of 8 or higher is required [16]. Another approach is to apply a time-varying, nonlinear recovery technique [17] which allows us to sample the signal at a frequency close to the Nyquist rate. This way we can sample higher input frequencies with lower power consumption, but at the cost of more complexity in digital post-processing. An iterative recovery algorithm described in [17] is used in this work to construct uniform samples. With the help of this recovery algorithm, non-uniform samples are converted to uniform samples and the harmonic distortion in the frequency spectrum is suppressed.

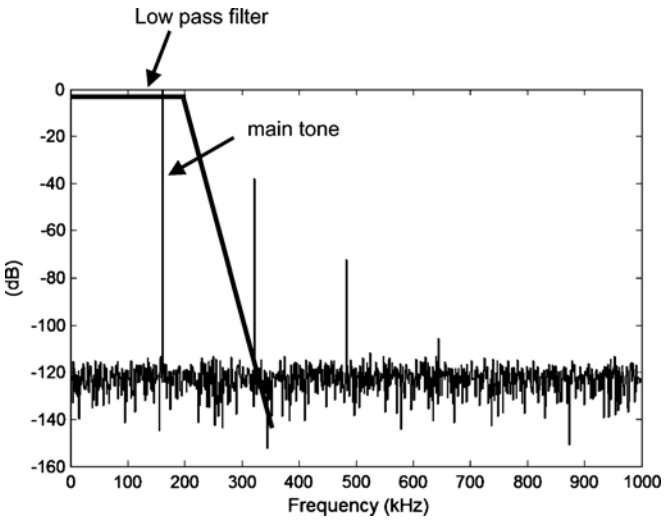

Fig. 3. An example showing that distortion artifacts caused by misinterpreting samples as uniform are suppressed by low-pass filtering.

III. Circuit Implementation

A block diagram of the PPM ADC, along with the TDC block, is depicted in Fig. 4. An unclocked comparator compares the

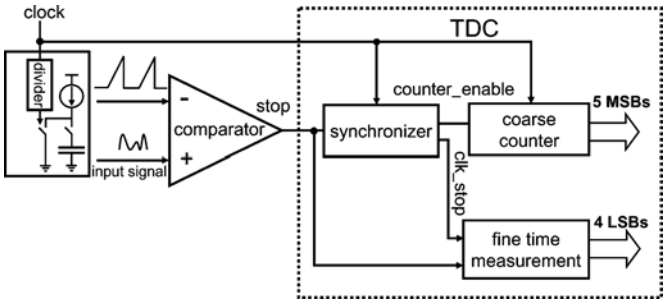

Fig. 4. ADC block diagram showing the TDC building blocks.

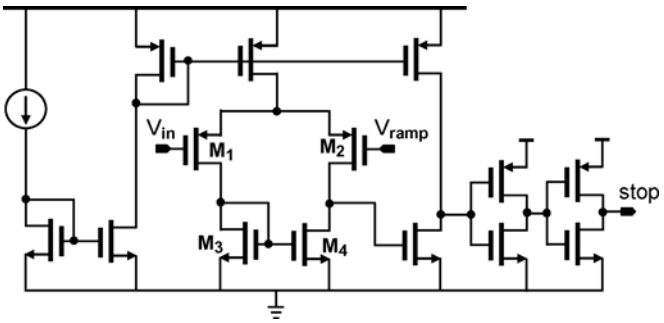

Fig. 6. Continuous-time comparator.

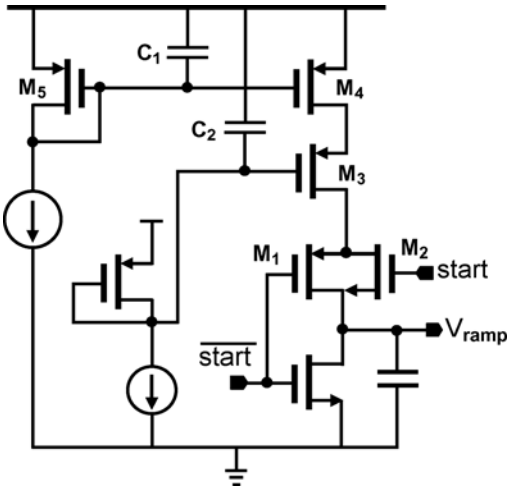

Fig. 5. Ramp generator.

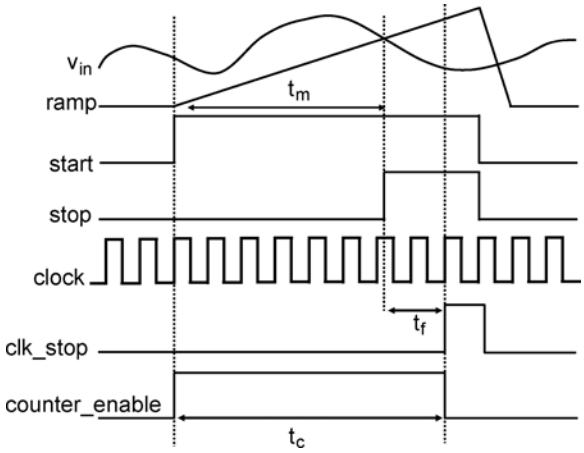

Fig. 7. PPM ADC timing signals.

output of a ramp generator with the input signal. A *stop* signal is generated when the ramp voltage exceeds the input signal. In the prototype, the two-step 9 bit TDC consists of a 5 bit counter as the coarse quantizer and a fine TDC that resolves 4 bits. The reference clock frequency, f_{clk}, is 128 MHz, so that the counter achieves a 5 bit resolution over the 250 ns TDC input time signal range. A synchronizer ensures the coarse and fine time measurements are correctly aligned. The ramp generator is synchronized with the reference clock of the system, which is the time reference in time-to-digital conversion block. These blocks are explained in detail in the following sections.

A. Ramp Generator Circuit

The ramp generator, shown in Fig. 5, consists of a cascoded current source charging a constant capacitance under the control of digital switches, M_1 and M_2. These switches are controlled by the *start* signal, which is obtained by dividing the reference clock by 128. Therefore, the ramp signal frequency is set at 1 MHz. Since the input signal is compared with the ramp only during charging, there is no requirement to match the charging and discharging rates and capacitor discharge is achieved simply with a switch to ground. The key challenges are ramp linearity and noise. Due to the low frequency operation of this ADC, flicker noise (1/f noise) is the dominant source of noise. Current source transistors, M_4 and M_5, are oversized to reduce flicker noise and biased at low g_m to reduce thermal noise. The noise contribution of cascode transistor M_3 is negligible compared with that of M_4 and M_5. Decoupling capacitors C_1 and C_2 filter out the noise coming from the bias transistors. The switching transistors M_1 and M_2 contribute little to the flicker noise [24]. To achieve an almost 11-bit-linear ramp with large dynamic range, transistors M_3 and M_4 must be biased with small $V_{\mathrm{DS}}(\mathrm{sat})$ to allow more headroom for the ramp voltage swing. $V_{\mathrm{DS}}(\mathrm{sat})$ is proportional to $(2 \cdot I/g_m)$ and reducing $V_{\mathrm{DS}}(\mathrm{sat})$ necessitates high transconductance (g_{m4}) in M_4 for a constant current. Increasing g_{m4} results in more current noise in the ramp generator and this indicates a tradeoff between ramp voltage range and output noise. Simulations indicate that a linearity of 11 bits is achieved over a 600 mV ramp range.

B. Comparator Circuit

The continuous-time comparator shown in Fig. 6 consists of a pMOS input differential amplifier followed by a common source stage. The input transistors, M_1 and M_2, operate in the subthreshold region. In addition to saving power, this allows a larger input common mode range and therefore larger ramp dynamic range. To avoid ADC distortion, the propagation delay variation with respect to the input common mode in this design is less than one LSB of the time measurement. This is done in part by sizing transistors, M_2 and M_4, such that the output impedance of the differential stage is dominated by the output resistance of M_4, which is relatively small. In this way, a wide bandwidth is achieved, and in addition, the output resistance of M_2, which

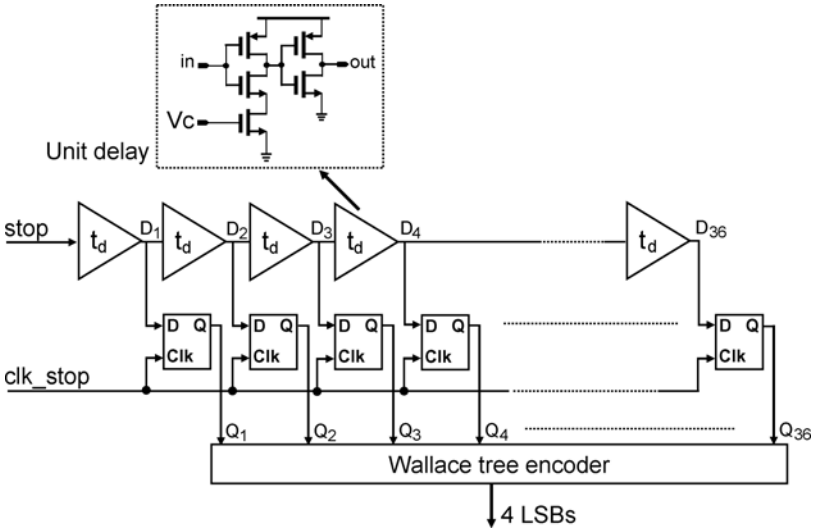

Fig. 8. Delay line TDC.

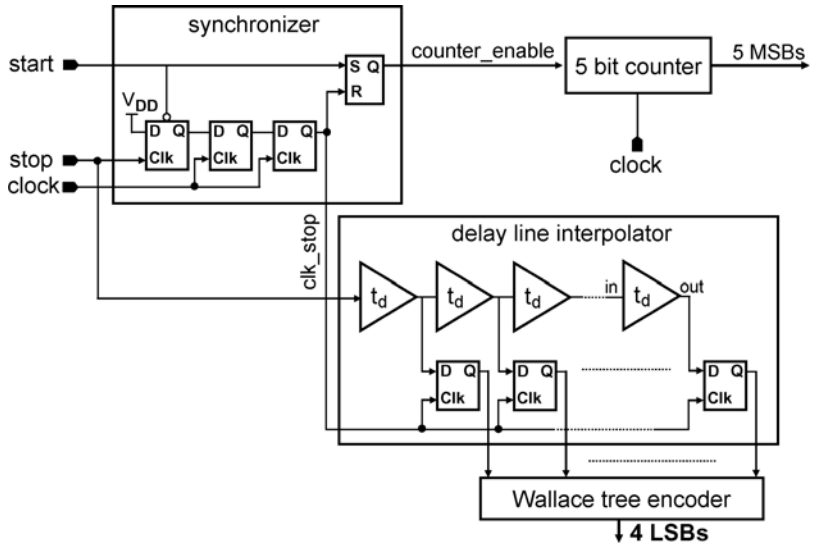

Fig. 9. Complete TDC architecture.

varies with the input common-mode level, does not affect the bandwidth.

C. Time-to-Digital Converter

The TDC measures the time interval between the start of the ramp to the crossover point of the ramp and the input signal. This time interval, denoted as t_m in Fig. 7, is between the rising edges of the *start* signal which is synchronized to the reference clock, and the *stop* signal which is generated by the comparator. As discussed in Section II, in order to efficiently measure t_m with high resolution, a two-step hybrid TDC is used.

To realize a two-step TDC, in addition to *start* and *stop*, two more signals are generated: *clk_stop* and *counter_enable*. The signal *clk_stop* is set by the arrival of the second-next rising edge of *clock* after the *stop* signal. The second *clock* rising edge is selected to avoid metastability issues, which will be addressed later. The *counter_enable* signal is set by *start* and reset by *clk_stop*. A coarse time quantizer, formed using a counter, measures the number of reference clock cycles while the *counter_enable* signal is high, thus measures t_c. The fine TDC measures the time t_f, defined as the time between the

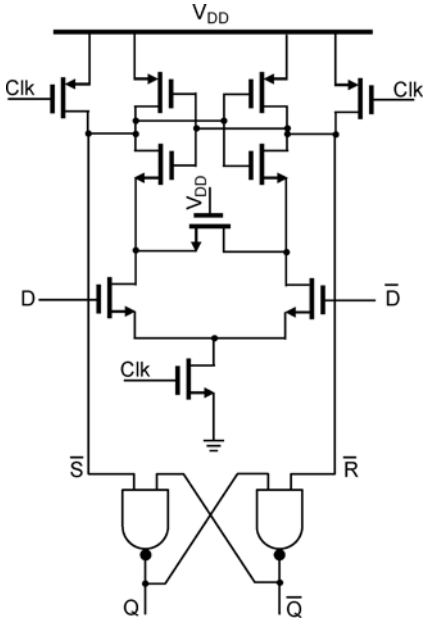

Fig. 10. Sense-amplifier flip-flop.

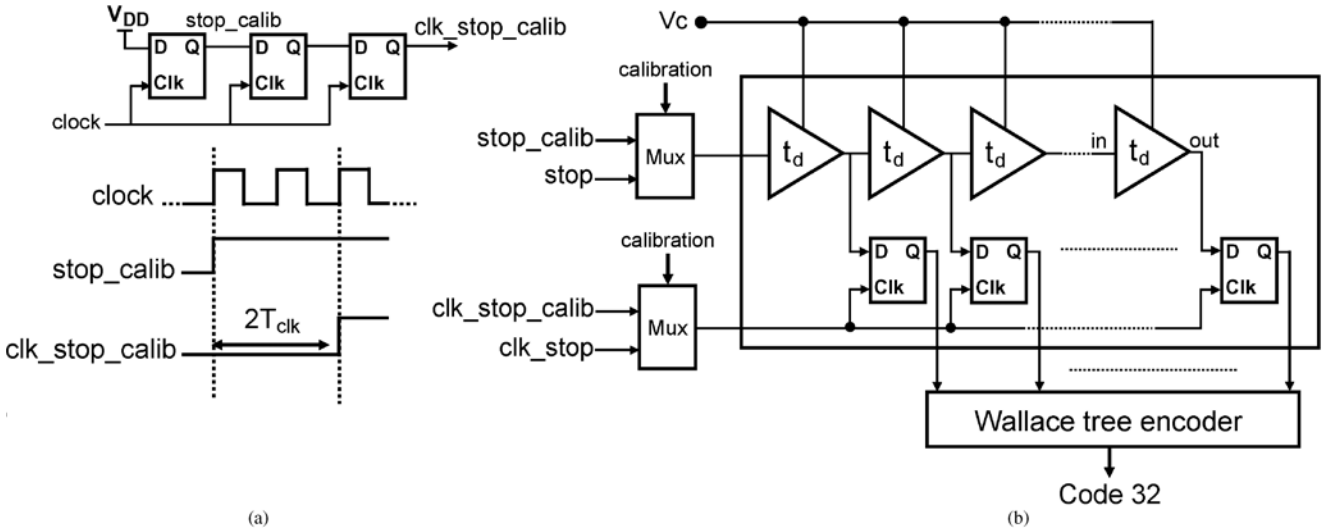

Fig. 11. Delay line interpolator calibration scheme.

stop signal and *clk_stop* rising edges. The overall TDC output is $t_m = t_c - t_f$.

A fine delay line TDC measures the interval t_f, shown in Fig. 7, from the *stop* rising edge to the *clk_stop* rising edge. The 32-element delay line, shown in Fig. 8, is tuned so that the required 32 delay steps span two full periods of the reference clock. A range of two reference clock periods is required since the synchronous *clk_stop* signal is the second-next reference-clock edge after the comparator *stop* signal. The asynchronous comparator output signal, i.e., *stop*, is the input to the delay line. 32 flip-flops, clocked by the *clk_stop* signal, sample delayed versions of the *stop* signal. The outputs of these flip-flops form a thermometer code with the number of 1's indicating the time from the *stop* rising edge to the *clk_stop* rising edge. Running the interpolating delay line off the *stop* edge, and not off the reference clock, saves power since the delay cells are only activated when there is a comparator transition. As the 32 delay cells span two reference clock periods, the fine TDC divides one clock period into 16 equal slices and resolves 4 LSBs.

The delay line is composed of 32 current-starved buffers with nMOS footer transistors (see Fig. 8). A tuning voltage V_c controls the gate voltage of the nMOS footer devices in the buffers. We ensure that the V_c control can enable a buffer delay of $2T_{\mathrm{clk}}/32$ over the full PVT range. In addition the pMOS and nMOS transistors of the buffer stage are oversized to reduce mismatch. Based on Monte Carlo analysis, the maximum delay variation due to mismatch in the buffers is 2% of the TDC LSB.

The complete TDC architecture is shown in Fig. 9. Sense-amplifier-based flip-flops [25], [26], shown in Fig. 10, are used in the TDC, because they can have a very narrow metastability window. One of the flip-flop inputs is connected to the delay line and the other input is connected to a reference voltage which is a fraction of the digital supply voltage. In this design, two design criteria regarding these flip-flops are considered. First, the input transistors are oversized to reduce mismatch. Second, the setup time of the sense-amplifier flip-flops is designed to be less than 2% of the delay line resolution, across PVT. Although the probability of metastability is reduced, errors can still occur, potentially causing large errors in the output thermometer code. A Wallace tree encoder [27] encodes the thermometer code, suppressing potential bubble and sparkle codes.

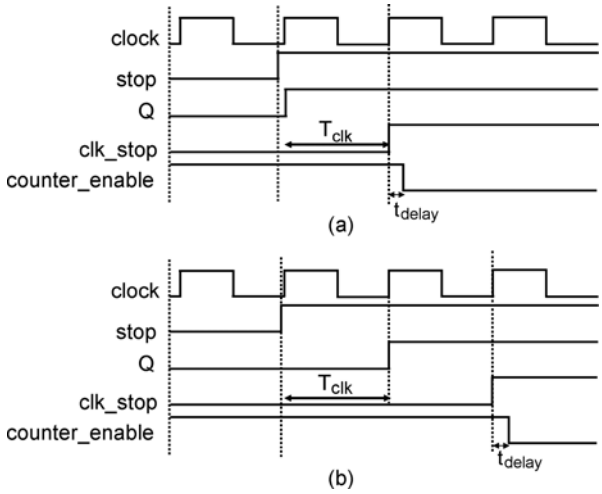

Fig. 12. Correct TDC operation whether the *stop* signal meets (a) and does not meet (b) the flip-flop setup time in synchronizer block.

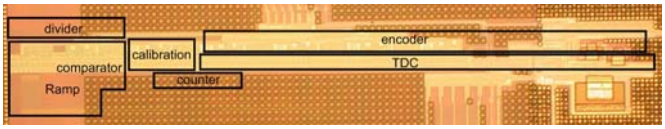

Fig. 13. Die microphotograph [29].

The delay buffers are calibrated during a calibration cycle in which *stop_calib* and *clk_stop_calib* signals are sent to the delay line interpolator through two multiplexers, as shown in Fig. 11. The time difference between the rising edges of these two signals is set to $2T_{\mathrm{clk}}$. In this mode, V_c is tuned to activate all 32 sampler flip-flop outputs. Additional delay stages at the tail of the 32 buffer chain detect possible buffer overflow errors. The calibration cycle in this prototype is carried out under off-chip

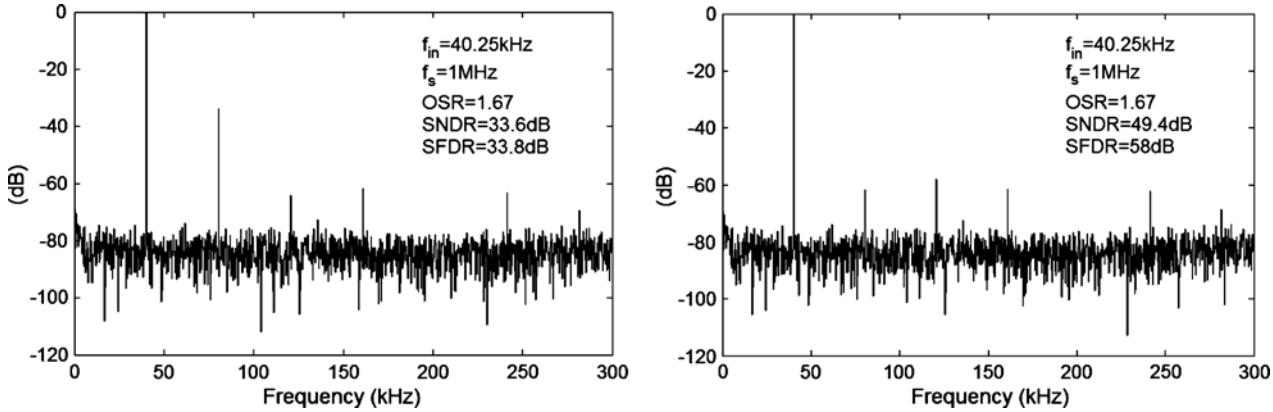

Fig. 14. (a) Raw data and (b) after post-processing measured spectrum of a single tone $f_{\rm in} = 40.25$ kHz and $f_s = 1$ MS/s.

control. Nevertheless, it is possible to make calibration automated and on-chip [28].

D. Synchronizer Block

The synchronizer ensures that the coarse and fine time measurements are correctly aligned. The synchronizer block (shown in Fig. 9), which consists of three flip-flops in series, generates the two signals, *counter_enable* and *clk_stop*. The first flip-flop detects the arrival of the *stop* signal while the second flip-flop catches the next rising edge of the *clock* right after the *stop* signal. The second-next rising edge of *clock* after the *stop* signal rising edge is detected by the third flip-flop. *stop* is an asynchronous signal, which arrives at an arbitrary time with respect to the reference clock. Consequently, it can lie within the metastability window of the second flip-flop. Waiting for another clock cycle in the third flip-flop significantly reduces the chance of metastability. In effect, this is a tradeoff between latency and accuracy, and at the expense of adding one clock period as an offset to the fine TDC block. The synchronizer also generates the *counter_enable* signal, discussed in Section III-C.

Thanks to the synchronizer, the coarse time measurement made by the counter is always correctly stitched to the fine time measurement, whether or not the *stop* signal arrival meets the setup time requirement of the second flip-flop in the synchronizer block (see Fig. 9). This is illustrated graphically with the waveforms shown in Fig. 12(a) and (b). It should be noted that in this design, the flip-flop setup time is designed to be a small fraction of the LSB in time measurement. One possible scenario is illustrated in Fig. 12(a), in which the *stop* signal rising edge occurs just before a *clock* rising edge (less than one TDC LSB) but it is still early enough to meet the flip-flop setup time. Therefore, the output (Q) of the second flip-flop of the synchronizer block goes high with the next rising edge of *clock* after the *stop*. The fine TDC measures one clock period, $T_{\rm clk}$, which is essentially the offset in TDC measurement.

In the second scenario as shown in Fig. 12(b), the *stop* signal rising edge occurs just before the *clock* rising edge (less than one LSB) but in this case the flip-flop setup time is not met and the output Q is set at the second-next rising edge of *clock* and thus the third rising edge of *clock* after *stop* is sampled as *clk_stop*. The fine TDC measures $2T_{\rm clk}$. Although there is an error of one $T_{\rm clk}$, since *counter_enable* is reset by *clk_stop*, the counter has already counted an extra clock period and the error is canceled out.

Since the *counter_enable* is reset by *clk_stop*, we ensure that it is reset with a certain delay with respect to *clk_stop*, denoted by $t_{\rm delay}$ in Fig. 12. It is important to guarantee that $t_{\rm delay}$ allows enough time for the counter to count the clock edge prior to the *clk_stop* within all PVT variations. In other words, $t_{\rm delay}$ must be longer than the hold time requirement of the flip-flops inside the counter block. In this way, we assure that there is no uncertainty in the counter measurement and no MSB error in the TDC result.

IV. Prototype and Measurement Results

The prototype 9 bit PPM ADC is implemented in 90 nm digital CMOS and occupies an active area of 0.06 mm^2, and a total area of 1 mm^2 including pads [29]. The layout of the prototype is shown in Fig. 13. It is worth noting that even though many of the analog components are removed in this architecture, the area is still dominated by the area of the remaining analog blocks. The analog circuits operate with a 1 V supply, while the digital blocks operate at near-threshold from a 400 mV supply.

The ramp repetition frequency, which is the sampling frequency f_s in this ADC, is 1 MHz. The input signal bandwidth is 300 kHz and therefore, the oversampling ratio is 1.7. The measured ENOB is 7.9 bits over the entire input bandwidth. The measured power consumption of the entire system is 14 μW (excluding digital post-processing). The analog and digital blocks each consume 7 μW. The figure of merit $(\text{power}/(2 \times \text{BW} \times 2^{\text{ENOB}}))$ is 98 fJ per conversion-step.

The measured spectrum for a 40.25 kHz tone sampled at $f_s = 1$ MHz is shown in Fig. 14(a). This FFT incorrectly assumes uniform sampling and so large harmonics due to non-uniform sampling are apparent. The spectrum of the same signal after the iterative algorithm is applied is shown in Fig. 14(b). As can be seen, the artifacts are suppressed and the SNDR and SFDR are improved by creating uniform samples in post-processing. The same plots are repeated in Fig. 15 for a signal at 290.25 kHz, close to the upper end of the input bandwidth. Measured DNL, INL, and SNDR versus $f_{\rm in}$ are illustrated in Fig. 16. The maximum measured DNL is 1.2 LSB and the maximum measured INL is 1.5 LSB. In another test, two tones at

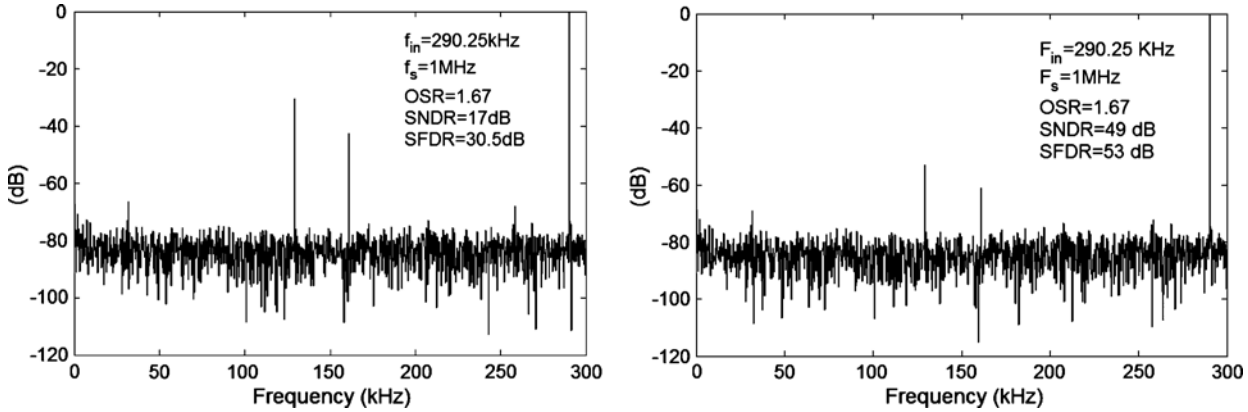

Fig. 15. (a) Raw data and (b) after post-processing measured spectrum of a single tone at $f_{\rm in} = 290.25$ kHz and $f_s = 1$ MS/s.

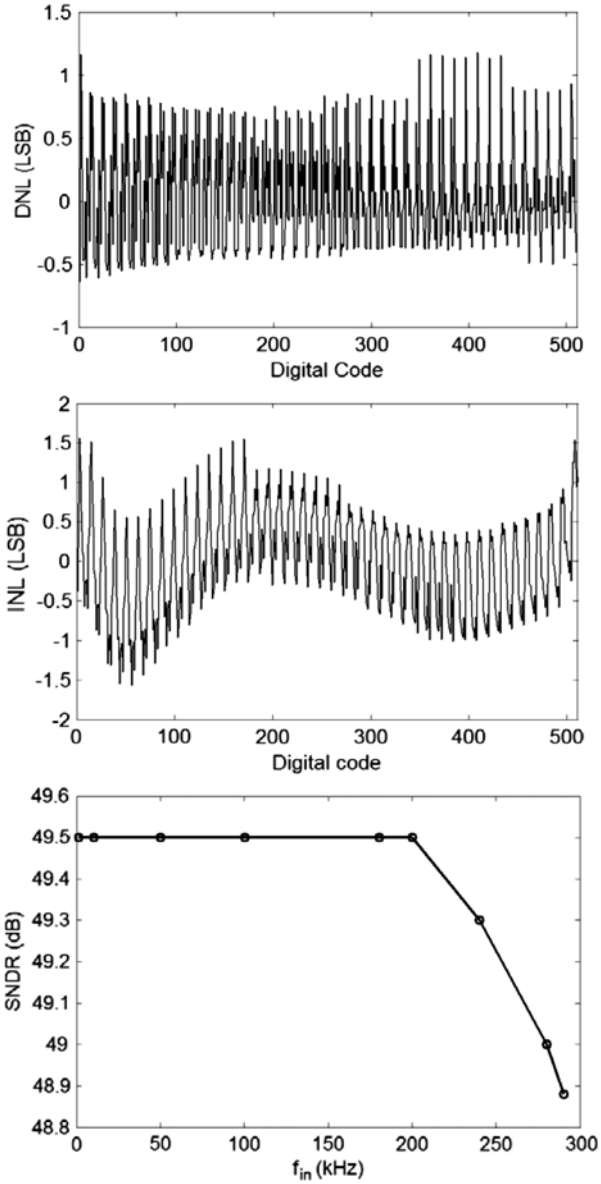

Fig. 16. Measured DNL, INL, and SNDR versus $f_{\rm in}$ at $f_s = 1$ MHz.

100.25 kHz and 20.25 kHz are applied to the ADC to observe the effect of possible inter-modulation distortion. The results are shown in the plots of Fig. 17. The top plot, Fig. 17(a), is the raw data before the post-processing. As evidenced in Fig. 17(b), the extra harmonics are suppressed and the inter-modulated products are below the noise floor. A summary of the measured chip performance is given in Table I.

TABLE I
PERFORMANCE SUMMARY

Sampling frequency	1 MHz
Input bandwidth	300 KHz
ENOB	7.9
DNL(max)	1.2 LSB
INL(max)	1.5 LSB
Digital voltage supply	400 mV
Analog voltage supply	1 V
Digital power	7 μW
Analog power	7 μW
Area	0.06 mm^2

V. CONCLUSION

By applying pulse-position-modulation to the input signal, we replace voltage measurement with time measurement, and employ digital circuitry to significantly reduce the power consumption and required silicon area. The analog circuitry is simplified to a ramp generator and comparator, leading to less design complexity and lower power consumption. An energy efficiency of 98 fJ/conv.step is achieved with a 9 bit prototype device. Many applications can directly use non-uniformly sampled data. A design trade-off for applications that require uniform samples is that digital post-processing is required to convert non-uniform samples to uniform ones, but this trade-off is quite favorable given recent technological advancements in nanometer CMOS technologies.[1] A comparative analysis between time-domain and voltage-domain flash ADC architectures shows that time-domain circuits become more energy

[1]The power overhead of digital post-processing is directly dependent on the chosen reconstruction algorithm and how it is optimized [30] (e.g., multistage interpolation). This ADC is ideally suited to sensor networks, where digital post-processing is done at a base station. The goal is to reduce complexity, area and power consumption of ADCs in the sensor nodes while the complexity is transferred to digital processing at a base station.

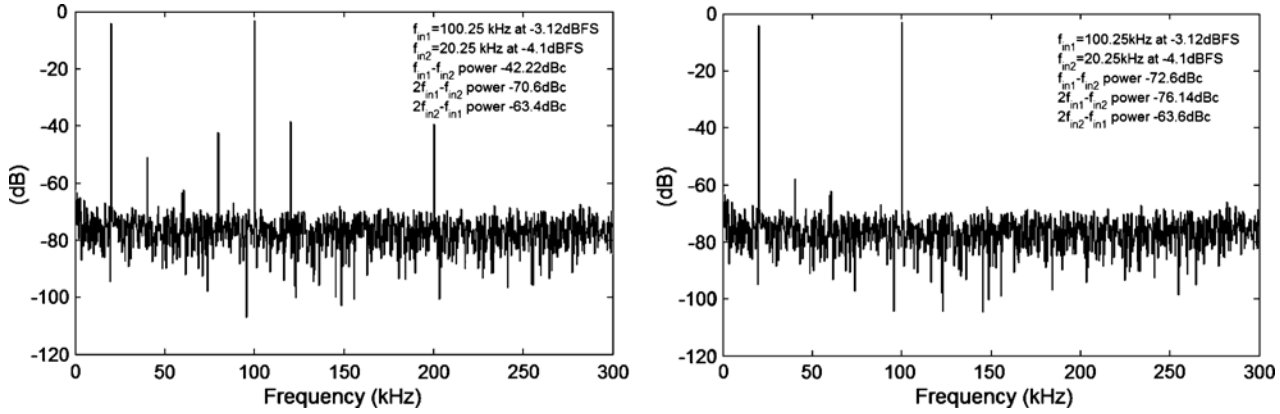

Fig. 17. Inter-modulation test results for $f_{\rm in1} = 100.25$ kHz and $f_{\rm in2} = 20.25$ kHz.

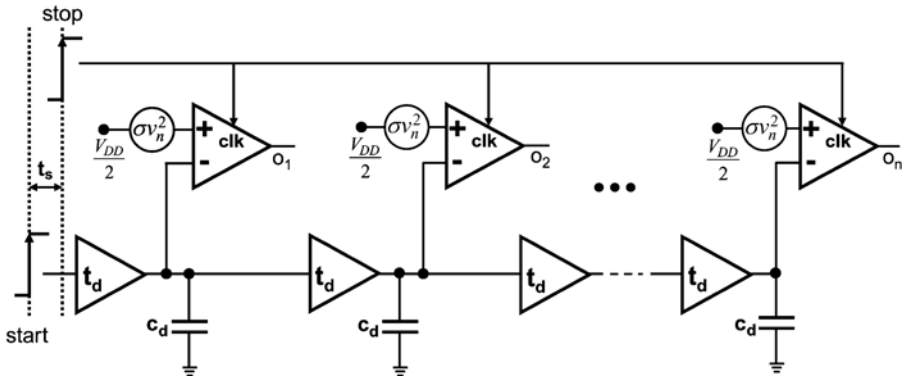

Fig. 18. Time-domain flash ADC.

efficient than noise-limited voltage-based ADC circuits as we move to more advanced nanometer CMOS technology nodes.

APPENDIX I

In order to quantify the advantage of time-based circuits over voltage-based ones, a fundamental comparison of time-domain and voltage-domain analog-to-digital conversion is presented here. We compare the minimum possible power consumptions in the thermal-noise-limited regime of a flash ADC and its analog, a delay line TDC, operating in the time domain. This is an appropriate comparison since a delay line TDC is really a flash ADC in the time domain. According to [31], the minimum power consumption of a thermal-noise-limited flash ADC with resolution B is

$$\frac{}{V_{\rm DD}} \cdot 2^{2B} \qquad (2)$$

where f_s is the sampling frequency and $V_{\rm eff}$ is $(V_{\rm GS} - V_{\rm th})/2$ in the square law model and is set to 80–100 mV in submicron transistors for better efficiency [31].

For the purpose of analyzing time-domain flash ADCs, we consider the TDC architecture shown in Fig. 18, which measures the time t_s between the rising edges of *start* and *stop*. The *start* signal is fed to the input of the delay line and the comparators, which function as flip-flops, are clocked by the *stop* signal. The comparators sample the outputs of the delay buffers outputs, forming a thermometer code, which quantizes the time between the *start* and *stop* rising edges. The delay line buffers are self-loaded and capacitors, C_d, represent the input capacitances of the next stage and the comparator input. The time resolution is limited to the smallest buffer delay available in the technology node.

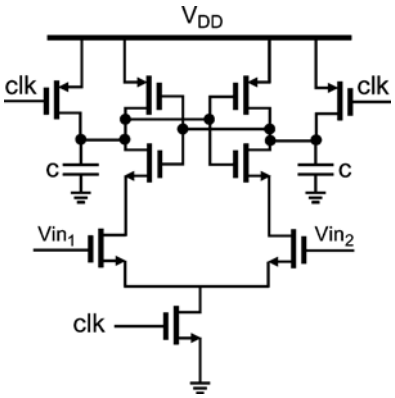

Fig. 19. Dynamic comparator.

To make a consistent comparison with a voltage-domain flash ADC, the flip-flops in this scheme (shown in Fig. 19) are the dynamic comparators [31]. One comparator input is connected to the delay line tap and the other one is tied to $V_{\rm DD}/2$. The outputs of the dynamic comparator are initially pre-charged to $V_{\rm DD}$ (i.e., during $clk =$ '0'). At the onset of the conversion (i.e.,

$clk =$ '1'), the regenerative latch either pulls the output exponentially towards zero or keeps it at $V_{\rm DD}$, depending on the difference between the input and the associated reference voltage, $V_{\rm DD}/2$, of that comparator. The delay line should complete its measurement in $1/2f_s$ since the TDC sampling frequency is f_s. The time resolution of TDC measurement is one buffer delay, denoted by t_d. Since the TDC conversion is done in the time domain and in a sequential way, the worst case conversion delay occurs with a full range input and the signal has to travel all the way to the end of the delay line. In this case, the conversion delay $t_{\rm conversion}$ is equal to

$$t_{\rm conversion} = t_{\rm comp} + 2^B t_d = \frac{1}{2f_s}, \tag{3}$$

where $t_{\rm comp}$ is the comparator conversion time. During $t_{\rm comp}$, the comparator should settle to the correct output voltage for a differential input voltage of $V_{\rm DD}/2$ to the comparator.[2]

Based on the regenerative nature of dynamic comparators, $t_{\rm comp}$ can be obtained through the following formulas:

$$V_{\rm in} \cdot e^{\frac{t_{\rm comp}}{\tau}} = V_{\rm DD} \tag{4.a}$$

where $V_{\rm in}$ is the differential input, τ is equal to C_c/g_m, and C_c is the capacitive load of the dynamic comparator. In this analysis, we are assuming that one comparator input is connected to the delay line tap and the other one is tied to $V_{\rm DD}/2$. Therefore, when the delay line tap becomes '1' (i.e., $V_{\rm DD}$), the input differential $V_{\rm in}$ is $V_{\rm DD}/2$, and so $t_{\rm comp}$ is calculated as

$$t_{\rm comp} = \tau \ln 2. \tag{4.b}$$

Now, we rewrite (3) by replacing g_m with $I_D/V_{\rm eff}$ in (4.b). Thus,

$$t_{\rm conversion} = 2^B t_d + \frac{C_c V_{\rm eff}}{I_D} \ln 2 = \frac{1}{2f_s}. \tag{5}$$

Deriving I_D from (5), we calculate the total comparator power consumption $P_{\rm comp}$ for the 2^B comparators as

$$P_{\rm comp} = 2^B \cdot \frac{C_c V_{\rm eff} \ln 2 \cdot V_{\rm DD}}{\frac{1}{2f_s} - 2^B t_d}. \tag{6}$$

Consequently, the total power consumption of the delay line (2^B buffers) and of the 2^B comparators, denoted by P_T, is equal to

$$P_T = 2^B \cdot C_d V_{\rm DD}^2 \cdot f_s + 2^B \cdot \frac{C_c V_{\rm eff} \ln 2 \cdot V_{\rm DD}}{\frac{1}{2f_s} - 2^B t_d} \tag{7}$$

where the first term in the right-hand side (RHS) of (7) describes the power consumed by the buffers in the delay line. This term is calculated based on the fact that, for each input sample taken at f_s, the signal edge has to travel all the way to the end of the delay line and toggle all 2^B buffers. The second part in the RHS of (7) comes from (6) and represents the power consumed by the comparators.

[2]It is important to realize that there is another constraint on the comparator speed, which is that the metastability window of the comparator must be a small fraction of the TDC resolution, t_d. For simplicity, we ignore this requirement as is done in analysis of a voltage-domain flash ADC in [31].

At this point, we consider thermal noise to assess the minimum power consumption. Generally speaking, thermal noise manifests itself as jitter in time-domain circuits. Individual jitter sources originate from each buffer, and these can be considered independent. The total jitter noise at an inverter output is calculated in [32], and by rearranging the equations from [32] we can express inverter jitter $\sigma^2_{\rm jinv}$ as

$$\sigma^2_{\rm jinv} = \left(\frac{8kT\gamma}{C_d V_{\rm DD}(V_{\rm DD} - V_{\rm th})} + \frac{4kT}{C_d V_{\rm DD}^2} \right) t_d^2. \tag{8}$$

This mean-squared jitter of a non-inverting delay buffers is twice $\sigma^2_{\rm jinv}$.

Comparators also introduce jitter. It has been previously shown that the input-referred noise of the dynamic comparator can be derived as [31], [33]

$$\sigma^2_{\rm ncomp} = \kappa \frac{kT\gamma}{C_c} \tag{9}$$

where κ is an architecture-dependant parameter and γ is a process-dependant parameter related to thermal noise. In this analysis, we assume both κ and γ are '1' for both voltage-domain and time-domain circuits to simplify our calculations. The jitter variance caused by the dynamic comparator $\sigma^2_{\rm jcom}$ can be approximated as the comparator input-referred noise power $\sigma^2_{\rm ncomp}$ divided by the square of the inverter slope s, as

$$\sigma^2_{\rm jcomp} = \frac{\sigma^2_{\rm ncomp}}{s^2}. \tag{10}$$

Assuming that the inverter output goes from zero to $V_{\rm DD}/2$ in t_d:

$$s = \frac{V_{\rm DD}}{2t_d}. \tag{11}$$

Substituting (9) and (11) in (10) gives us

$$\sigma^2_{\rm jcomp} = \frac{kT}{C_c} \cdot \frac{4t_d^2}{V_{\rm DD}^2}. \tag{12}$$

The maximum jitter is at the end of the delay line, where we observe the aggregate jitter of all the previous buffer stages. Since the inverter and comparator noise can be considered uncorrelated, the total jitter noise in the last stage of the delay line, $\sigma^2_{\rm jtotal}$, is

$$\sigma^2_{\rm jtotal} = 2^B \cdot \sigma^2_{\rm jinv} + \sigma^2_{\rm jcomp} \tag{13}$$

or

$$\sigma^2_{\rm jtotal} = \left(\frac{2^{B+1} \cdot 8kT\gamma}{C_d V_{\rm DD}(V_{\rm DD} - V_{\rm th})} + \frac{2^{B+1} \cdot 4kT}{C_d V_{\rm DD}^2} + \frac{4kT}{C_c V_{\rm DD}^2} \right) t_d^2. \tag{14}$$

We assume the minimum power consumption is achieved when this jitter power is equal to the time-domain quantization noise power; hence

$$\sigma^2_{\rm jtotal} = \frac{t_d^2}{12}. \tag{15}$$

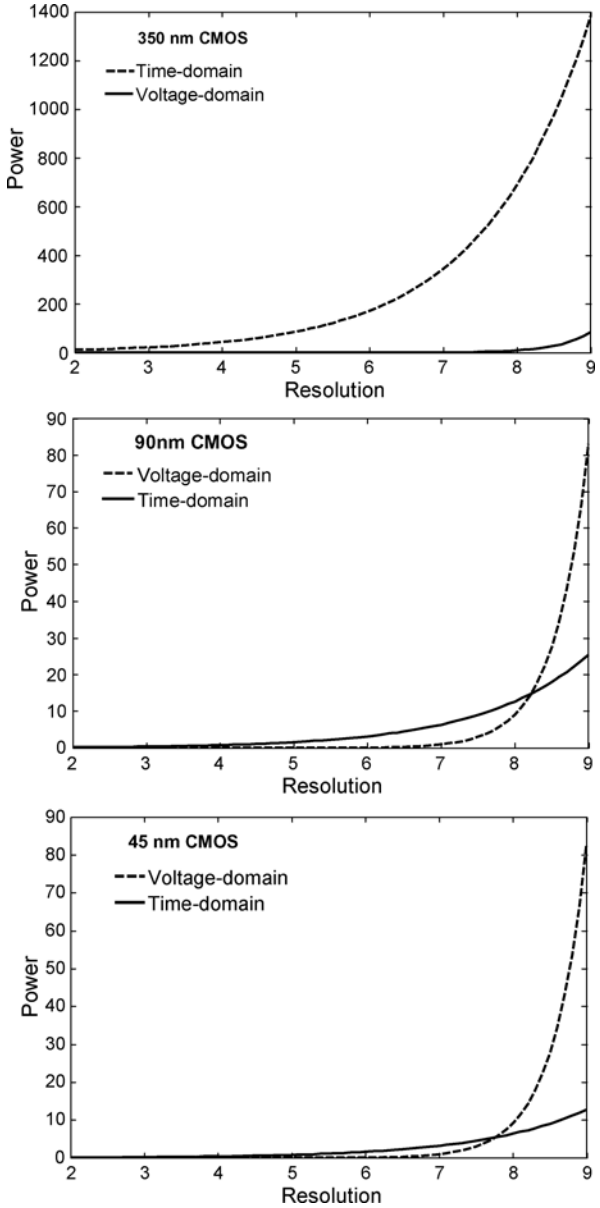

Fig. 20. Time-domain and voltage-domain minimum power consumption.

Combining (14) and (15), we get

$$\frac{\sigma^2_{\text{jtotal}}}{t_d^2} = \left(\frac{2^{B+1}\cdot 8kT\gamma}{V_{\text{DD}}(V_{\text{DD}}-V_{\text{th}})} + \frac{2^{B+1}\cdot 4kT}{V_{\text{DD}}^2}\right) \cdot \frac{1}{C_d} + \left(\frac{4kT}{V_{\text{DD}}^2}\right)\cdot\frac{1}{C_c} = \frac{1}{12}. \tag{16}$$

The input inverter capacitance C_d of a fan-out of one inverter chain can be estimated in each CMOS technology. The comparator capacitance C_c is then computed from (16) based on the allowed amount of jitter. Having determined C_d and C_c, we can then examine the minimum total power from (7) at different sampling frequencies.

The minimum power consumption of time-domain and voltage-domain flash ADC structures (P_T and P_v, respectively) for 0.35 μm, 90 nm, and 45 nm CMOS are compared in Fig. 20. A relatively low sampling frequency of 10 MHz is chosen so that the time-domain flash ADC can be implemented in all three CMOS technology nodes. In other words, 10 MHz is low enough to be feasible in 0.35 μm CMOS. As evident, in 0.35 μm CMOS, the voltage-domain flash ADC has lower power consumption in the conventional flash architecture resolution range (i.e, below 9 bits). In 90 nm CMOS technology, the power of the voltage-domain flash ADC becomes larger than the power of the time-domain flash ADC at approximately 8.5 bits of resolution. Moving to 45 nm CMOS, this crossover happens at a lower resolution, around 7.5 bits. This comparison suggests that time-based architectures are more efficient in advanced technologies with smaller gate lengths.[3]

ACKNOWLEDGMENT

The authors acknowledge the support of National Semiconductor.

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