An IF 8-Element 2-Beam Bit-Stream Band-Pass Beamformer

Jaehun Jeong [1], Nicholas Collins [2], and Michael P. Flynn [3]
Electrical Engineering and Computer Science, University of Michigan, Ann Arbor, MI 48109, USA
[1] jaehun@umich.edu, [2] ncolins@umich.edu, [3] mpflynn@umich.edu

***Abstract* — We introduce a new ADC-digital co-design approach to IF digital beamforming (DBF) that combines continuous-time band-pass ΔΣ modulators (CTBPDSMs) and bit-stream processing (BSP) to achieve highly flexible and low-cost DBF. Our prototype DBF IC digitizes eight 260MHz IF signals at 1040MS/s with band-pass ADCs, and performs DBF directly on the over-sampled, un-decimated ADC outputs, achieving band-pass filtering in both spatial and frequency domains. With 12b programmable complex weights, the prototype generates two simultaneous beams, and achieves an SNDR of 63.3dB with an 8.9dB array improvement over a 10MHz bandwidth. Fabricated in 65nm CMOS, the prototype is the first IC implementation of IF DBF, occupies 0.28mm^2, and consumes 124mW.**

***Index Terms* — Beam steering, narrowband, delta-sigma modulation.**

I. Introduction

Beamforming improves SNR, and enables spatial filtering of interferers in receivers. However, high power consumption, large area, and routing complexity are bottlenecks to implementing an efficient beamforming system, especially for large numbers of elements. Conventionally, beamforming is implemented in the analog/RF domain [1, 2] in ICs. With RF beamforming, since signals are combined in the RF domain, the IF and baseband hardware, including mixers and ADCs, can be minimized. However, RF beamforming is limited by high insertion loss, component mismatch, and low SNR.

Digital beamforming (DBF) offers the highest accuracy and flexibility. Another significant advantage is that DBF can simultaneously form multiple beams. However, despite these advantages, the adoption of DBF has been limited by high power consumption and large die area due to the need for multiple high-performance ADCs and extensive DSP. For these reasons, DBF is largely confined to base station applications, and implemented with FPGAs [3] or in software [4]. IF DBF is even more compelling because it simplifies the receiver chain by moving the ADCs closer to the antennas, and allowing I/Q down-conversion to be accurately implemented in the digital domain. However, power consumption and die area of conventional high-speed ADCs are prohibitive.

We introduce a new power and area efficient ADC-digital co-design approach to IF DBF that combines continuous-time band-pass ΔΣ modulators (CTBPDSMs) and bit-stream processing (BSP). An array of compact (0.03mm^2), low-power (13.1mW) CTBPDSMs directly digitizes 260MHz IF signals from eight input elements. DBF is directly performed on the over-sampled, un-decimated low-resolution outputs of the CTBPDSM array.

The unique combination of CTBPDSMs and BSP has several advantages. First, the CTBPDSMs efficiently digitize the relatively high-frequency IF signals, while the continuous-time architecture relaxes the anti-alias filter requirements, simplifying the RF front-end design. Second, with direct IF sampling, most of the signal processing, including digital down-conversion (DDC), is carried out in the digital domain, and I/Q mismatch effects are minimized. Third, over-sampling and noise shaping in the CTBPDSMs enable a high SNR with a relatively low quantizer resolution (i.e. 5-level digital output). We take advantage of the very low word width to implement energy-efficient BSP arithmetic. Fourth, since BSP is directly performed on the over-sampled, un-decimated outputs of the CTBPDSMs, decimation filtering, a high-cost operation, is needed only once for the final output.

Combined with the CTBPDSMs, our prototype DBF IC performs band-pass filtering in both spatial and frequency domains. The narrowband nature of the CTBPDSM is ideal for phase-shift beamforming of narrowband signals.

II. System Overview

A block diagram of the 8-element, 2-beam prototype DBF IC is shown in Fig. 1. Eight CTBPDSMs directly digitize 260MHz IF signals from eight input elements at

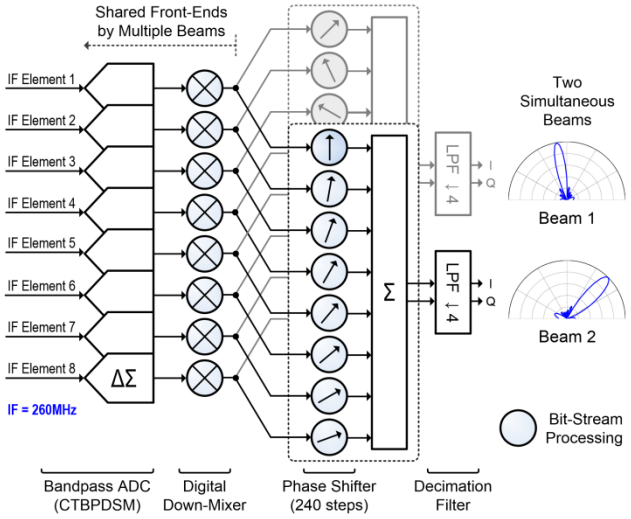

Fig. 1. Overview of the 8-element 2-beam prototype DBF IC

1040MS/s over a 20MHz bandwidth. The 5-level digital outputs of the CTBPDSMs are down-mixed, and phase-shifted by multiplication with programmable 12b complex weights. In this approach, the 5-level digitized signals are directly processed without decimation filtering for I/Q DDC and phase shifting. This BSP approach replaces bulky digital multipliers with simple multiplexers (MUXs), greatly reducing circuit complexity. Phase-shifted signals are summed to create 1040MS/s 10b I/Q beam outputs, which are low-pass filtered and decimated by four to produce the overall 260MS/s 13b I/Q beam outputs.

III. Continuous-Time Band-Pass ΔΣ Modulators

The circuit implementation of the 4th order CTBPDSM is shown in Fig. 2. Since an *N*-element digital beamformer requires *N* ADCs, the power consumption and area of ADCs play a large role in the power consumption and area of the entire beamformer.

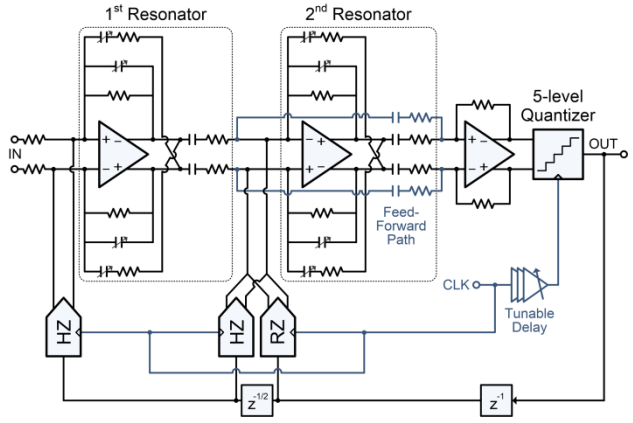

Fig. 2. Circuit implementation of the 4th order CTBPDSM

In the modulator, single op-amp resonators [5] consume less power, and are smaller than conventional LC-tank resonators. A high quality factor resonator is realized with a single op-amp by using positive feedback. The resonator center frequency of $f_s/4$ (260MHz) simplifies the design of DDC. 4b tunable capacitors adjust the center frequency.

A single feed-forward path around the 2nd resonator further improves efficiency. The modulator still retains the 2nd order anti-alias filtering of the 1st resonator. The feed-forward path reduces the signal swing at the output of the 2nd resonator op-amp, and relaxes power and linearity requirements. In addition, the feed-forward path removes a return-to-zero (RZ) feedback DAC to the 1st resonator input, reducing the input-referred noise of the modulator. Overall, the modulator has one RZ and two half-clock-delayed return-to-zero (HZ) current steering DACs.

The output currents from the two resonators are summed together, converted to voltages, and quantized by a 5-level 1040MS/s flash quantizer. The low quantizer resolution facilitates MUX-based multiplication for phase shifting. Programmable trim currents calibrate comparator offsets. A 3b tunable delay corrects any excessive loop delay, aligning the sampling at the quantizer and feedback current triggering.

The prototype beamformer contains eight CTBPDSMs. Each modulator consumes 13.1mW, and occupies only 0.03mm^2, which is almost an order of magnitude smaller than the CTBPDSM in [5].

IV. Digital Down-Conversion and Phase Shifting

Fig. 3(a) summarizes the mathematical operations of DDC and phase shifting by complex weight multiplication (CWM). The I/Q outputs of the down-mixers are weighted, and combined to generate phase-shifted I/Q outputs. In our BSP approach, the digital outputs of the CTBPDSMs are directly processed before they are low-pass filtered and decimated to enable MUX-based implementation of DDC and phase shifting. As a result, eight MUXs (Fig. 3(b)) replace six multipliers and two adders (Fig. 3(a)).

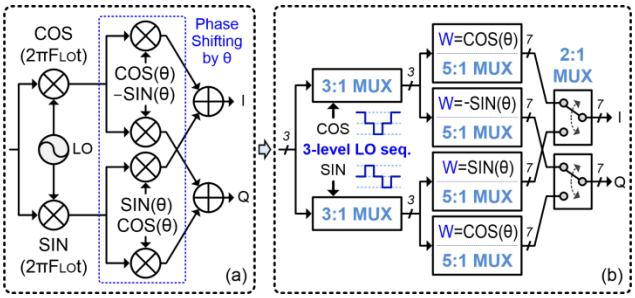

Fig. 3. (a) Mathematical operations of DDC and CWM
(b) MUX-based BSP implementation

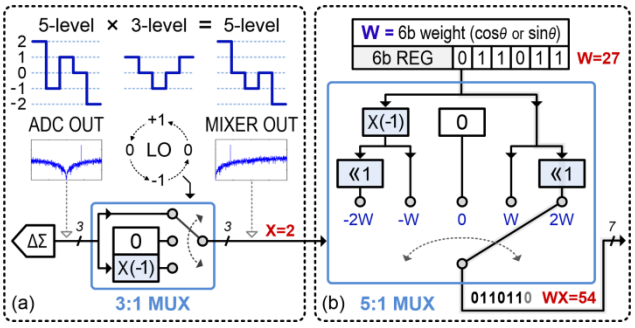

Fig. 4. (a) DDC implemented with a 3:1 MUX
(b) CWM implemented with a 5:1 MUX

A. Digital Down-Conversion with a 3:1 MUX

Choosing a CTBPDSM center frequency of $f_s/4$ greatly simplifies the design of DDC [6], since the LO signals, $\cos[n\pi/2]$ and $\sin[n\pi/2]$, are now represented by only three values (-1, 0, and +1). DDC (Fig. 4(a)) is performed with a simple 3:1 MUX: pass-through, zero, and sign-change. Moreover, after multiplication by the 3-level LO signals (-1, 0, or +1), the down-mixed 5-level CTBPDSM outputs are still represented by five levels (-2, -1, 0, +1, and +2).

B. *Phase Shifting with a 5:1 MUX*

We expand the multiplier-less single-bit DSP, proposed more than two decades ago in [7] to 5-level streams. Since all five levels of the down-mixed signals are powers of 2, only 1b left-shift ($\ll 1$) and sign-change are required for multiplication. As shown in Fig. 4(b), the 5-level output of the down-mixer determines the 5:1 MUX operation (i.e. sign-change, zero, and 1b left-shift) on the 6b stored weight ($\cos\theta$ or $\sin\theta$). In this way, a 5:1 MUX performs multiplication with the 6b weight, and the result is a 7b output. In addition, since the 3-level I/Q LO sequences are alternately zeroes, only the I or the Q output of the down-mixer is non-zero at any time. As a result, the sum of two 5:1 MUX outputs is implemented with a 2:1 MUX, and the result is still a 7b output. Two 2:1 MUX outputs represent the result of multiplication with a 12b complex weight ($e^{j\theta}$). Overall, four multipliers and two adders required for phase shifting are implemented with six MUXs, greatly reducing circuit complexity.

V. Comparison between DSP and BSP

The CTBPDSM array achieves very efficient IF digitization, and enables BSP. Fig. 5 compares our BSP implementation of an 8-element digital beamformer with a conventional DSP implementation. We compare the two implementations in terms of power consumption and area based on the simulation of synthesized digital blocks.

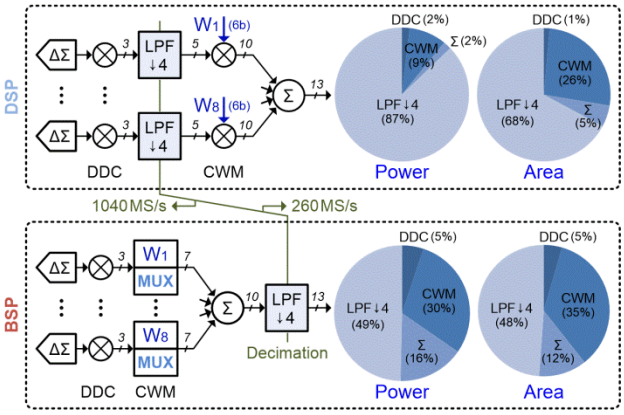

Fig. 5. DSP/BSP implementations of an 8-element beamformer

In conventional DSP with over-sampling ADCs, the over-sampled ADC outputs are decimated before further processing so that back-end digital circuits can operate at lower data rates (but with increased word width), resulting in less power consumption. However, in a weighted-sum system (e.g. beamformer) with multiple inputs and a single output, the cost of decimation filtering increases linearly with the number of inputs, and decimation filtering becomes a power and area bottleneck (Fig. 5).

In BSP, decimation filtering, a high-cost operation, is performed only once after all multiple paths are combined. This, however, requires CWM for phase shifting to operate at higher data rates, but with lower word width. The penalty of higher data rate in BSP is overcome by replacing bulky multipliers with simple MUXs. As a result, despite the higher data rate, MUX-based weighting achieves comparable power consumption to conventional multiplier-based weighting at a lower data rate, and greatly reduces area. The power consumption and area of our BSP implementation are 36% and 32%, respectively, of a conventional DSP implementation (Fig. 6).

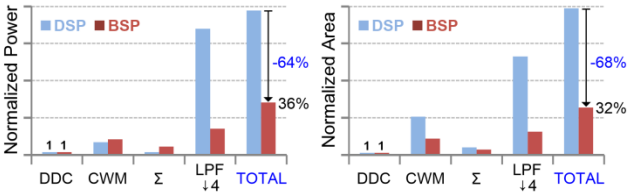

Fig. 6. Power and area comparison between DSP/BSP

VI. Measurements

The 8-element, 2-beam DBF IC is fabricated in 65nm CMOS (Fig. 11), and occupies a core area of 0.28mm^2 (0.24mm^2 for eight ADCs and 0.04mm^2 for the DBF core).

Each CTBPDSM consumes 13.1mW from a 1.4V supply. For a single CTBPDSM with a 266MHz input sinusoid, the measured SNDR is 54.4dB over a 20MHz bandwidth (Fig. 7(a)).

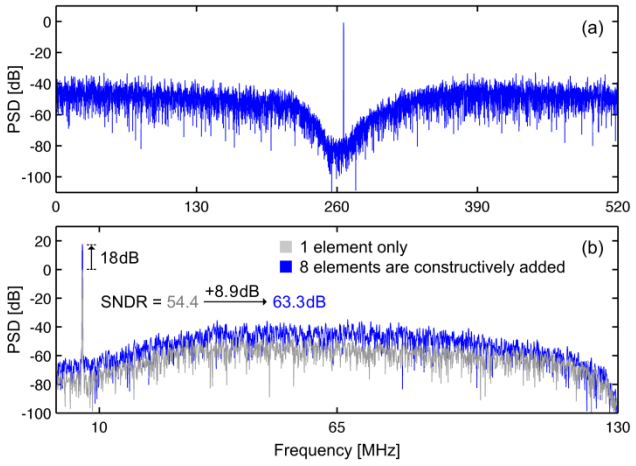

Fig. 7. (a) Measured spectrum of the single CTBPDSM output (b) Measured spectrum of the beam output

The outputs of the eight CTBPDSMs are fed to the Verilog synthesized DBF core, which consumes 18.9mW from a 0.9V supply. When the eight CTBPDSM outputs are down-mixed, phase-shifted, and constructively added, the fundamental tone linearly increases by 18dB while element noise is uncorrelated, resulting in an SNDR of 63.3dB corresponding to an 8.9dB array improvement over a 10MHz bandwidth (Fig. 7(b)).

The prototype DBF IC produces two independent beams from eight input elements. Various weighting functions can be applied with 12b programmable weights.

Phase shifting with a set of complex weights of $e^{j(k\theta)}$ adjusts the delay of the received and down-mixed signal (x_k) at the k-th element to create a beam ($=\sum_{k=0}^{7} x_k e^{j(k\theta)}$) with one main-lobe at a desired angle. A 12b resolution of the complex weight provides 240 phase-shift steps with an average step size of 1.5°. Fig. 8 shows the measured single main-lobe beam patterns overlaid on ideal beam patterns. During measurements, eight synchronized direct digital synthesizers (DDSs) generate poly-phase sinusoidal inputs to mimic the received signals from an antenna array with λ/2 spacing. The beam measurement step size is 2.5°.

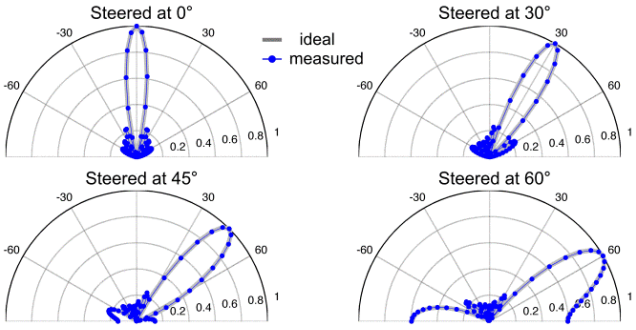

Fig. 8. Measured and ideal beam patterns (with one main-lobe)

In addition, combining two single main-lobe responses creates a single beam with two main-lobes. This can be easily done in the digital domain by using combined complex weights of $(e^{j(k\theta_1)} + e^{j(k\theta_2)})/2$ at the cost of a 6dB reduced array gain (Fig. 9). The measured beam patterns with two main-lobes are shown in Fig. 10.

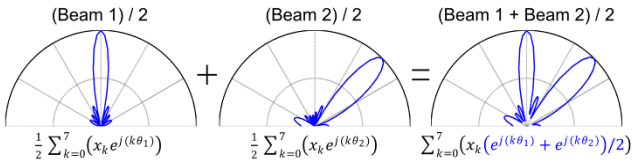

Fig. 9. Creating a single beam with two main-lobes

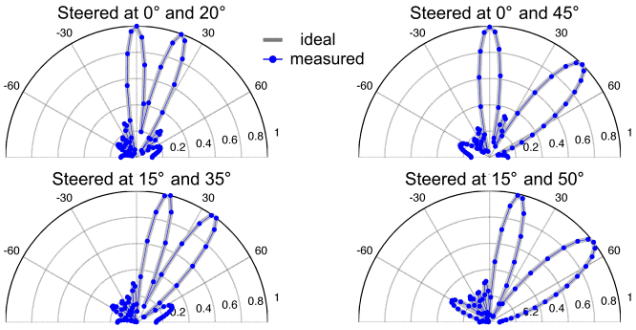

Fig. 10. Measured and ideal beam patterns (with two main-lobes)

A second simultaneous beam can be configured with the same flexibility. The measured beam patterns show great consistency with the ideal patterns, which is difficult to achieve in analog beamforming (ABF).

VII. Conclusion and Acknowledgements

This paper describes the first IC implementation of IF DBF. The unique combination of CTBPDSMs and BSP avoids high power consumption and large area, which have prevented the low-cost implementation of DBF. Compared to ABF ICs [1,2], the prototype DBF IC has more elements, more beams, more phase-shift steps, better array SNDR improvement, and has the advantages of the inherent accuracy and flexibility of digital processing. The power consumption per unit element of the prototype is only 6% of the FPGA implementation in [3].

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TABLE I
Performance Summary and Comparison

Metric	This Work	[1]	[2]	[3]
Beamforming Domain	Digital	Analog/RF	Analog/RF	Digital
# of Elements	8	4	4	2
# of Beams	2	1	1	1
IF Bandwidth(1) [MHz]	20	300	3.3	–
Array SNDR [dB]	63.3	–	–	–
SNDR Improvement [dB]	8.9(2) / 9(3)	– / 6(3)	4(2) / 6(3)	– / 3(3)
# of Phase-Shift Steps	240	32	8	–
Power [mW]	124	65 - 168	34 - 119	500
Active Area [mm^2]	0.28	0.18	0.65	–
Technology	65nm CMOS	65nm CMOS	28nm CMOS	FPGA

(1) for 1-element (2) measured (3) theoretically expected

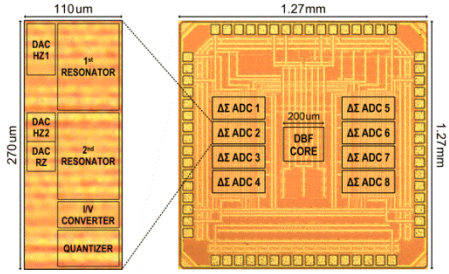

Fig. 11. Die micrograph

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