A 77dB-SFDR Multi-Phase-Sampling 16-Element Digital Beamformer with 64 4GS/s 100MHz-BW Continuous-Time Band-Pass ΔΣ ADCs

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***Abstract*— This paper tackles the fundamental limitation of distortion in large-scale digital beamforming. SNR improves by 3dB for every doubling of array size; however, distortion is correlated and so is not improved by the array gain. This work introduces the concept of multiple ADCs per element, with each sampling at a different phase, to both reduce distortion of the ADCs and RF frontend. A further advantage is that multi-phase-sampling with continuous-time band-pass delta-sigma modulators (CTBPDSMs) reduces the ADC clock-jitter sensitivity. A prototype 16-element 1GHz-IF digital beamformer employs four multi-phase-sampling sub-ADCs per element. The prototype beamformer IC integrates 64 4GS/s sub-ADCs and digital processing to generate four simultaneous beams. Bit-stream digital beamform processing efficiently handles the aggregate 0.256TS/s from the entire ADC array. The measured beamformer SNDR and SFDR are 56dB and 77dB, respectively. Multiphase sampling improves measured HD3 by 9dB.**

***Keywords*— Digital beamforming, phased-array, receiver, linearity, delta-sigma modulator (ΔΣM).**

I. Introduction

Large-scale beamforming is essential for emerging RF and mm-wave communication systems. Digital beamforming has important advantages for large arrays including accurate beam patterns, multiple simultaneous beams, and fast steering [1-2]. ADC performance is critical for large arrays but despite some progress [2], distortion from the element ADCs remains a fundamental limitation. Distortion is a limitation because although averaging in large arrays improves SNR (i.e., ideally a 3dB "array gain" for doubling of array size), averaging cannot reduce distortion. Techniques to improve ADC SNR and distortion [3] invariably lead to much higher power consumption and much larger die area. This work introduces the new approach of using multiple sub-ADCs per-element to significantly improve both SNR and distortion. We demonstrate a 1GHz IF input, 64-ADC 16-element digital beamformer with a measured SFDR of 77dB.

The Continuous-Time Bandpass Delta Sigma Modulator (CTBPDSM) ADC is very attractive for digital beamforming but is limited in SNDR and SFDR. CTBPDSMs benefit from high speed, low power, and compact area. In a digital beamformer, CTBPDSMs can directly digitize a high frequency IF, and facilitate very efficient digital bit-stream beam processing [2]. However, practical considerations such as the nonlinearity of the feedback DACs, the finite amplifier GBW, and clock jitter limit the SNDR of GHz input-frequency CTBPDSMs to ~40dB [2]. ADC techniques to mitigate these challenges consume high power and area and are prohibitive for high-bandwidth beamformer array applications [4].

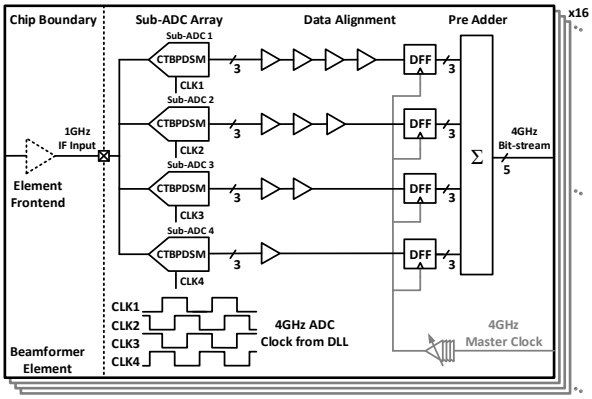


Fig. 1: Four sub-ADCs per-element sample the 1GHz IF input. The sub-ADCs bit-stream outputs are digitally aligned and added together.

Our new approach gets around the limitations of the CTBPDSM ADC by replacing the per-element ADCs in a conventional beamformer with multiple lower-performance ADCs. To circumvent the beamformer ADC performance bottleneck, we introduce two new techniques: 1) multiple parallel per-element ADCs; and 2) multi-phase parallel ADC sampling. These techniques improve ADC SNR by 7dB, improve HD3 by 9dB, and relax the clock phase noise requirement by 5.6dB.

II. Multi-Phase-Sampling Continuous-Time Bandpass Delta-Sigma Modulator

A. Multiple per-element ADCs and multi-phase-sampling

We replace the single, per-element ADCs in a conventional digital beamformer with multiple (i.e. four) parallel sub-ADCs per element to effectively and efficiently improve SNR and

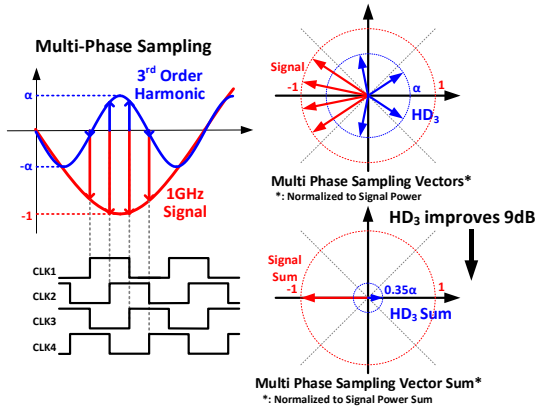


Fig. 2: ADC multi-phase-sampling attenuates odd harmonics.

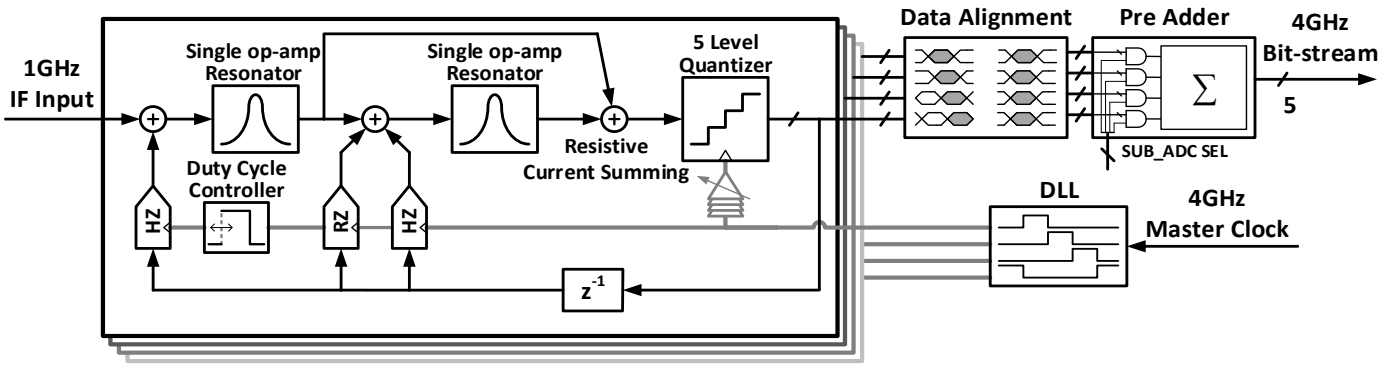


Fig. 3. Multi-phase sampling continuous-time bandpass delta-sigma modulator (CTBPDSM) sub-ADC array with duty cycle controller.

SFDR, As shown in Fig. 1, for each element, four bandpass sub-ADCs sample the IF signal from the RF frontend. Furthermore, these sub-ADCs sample at phase-shifted clock edges, instead of sampling at the same clock instant. As we will see, multi-phase sampling in the sub-ADCs and summing the result cancels distortion and suppresses jitter.

Combining the outputs of multiple ADCs that sample at the same instant improves SNR and SNDR, but this improvement is limited by ADC distortion. In multi-phase sampling, we distribute the phases of the sampling clocks of the parallel ADCs to provide two significant benefits: 1) suppression of harmonic distortion both within the ADCs and from the frontend, and; 2) averaging of in-band noise including that introduced by clock jitter.

We explain the distortion cancellation with the sampling plot and vector plots of Fig. 2. Our prototype system employs four parallel bandpass sub-ADC sampling the 1GHz IF input at 4GS/s. This sampling frequency is four times the IF carrier frequency and the sampling instants for the four sub-ADCs are spaced in 90-degree increments of the sampling clock. As depicted in Fig 2, the summation of these time-offset samples suppresses odd harmonics. The vector diagram in the figure shows that summing the time-offset samples leads to a substantial attenuation of the 3rd-order harmonic. Considering the slight attenuation of the fundamental, HD3 improves by 9.1dB. This filtering effect extends to higher-order odd harmonics (i.e. 12.6dB suppression of HD5). It filters both harmonics from the ADC and from the frontend. Suppression

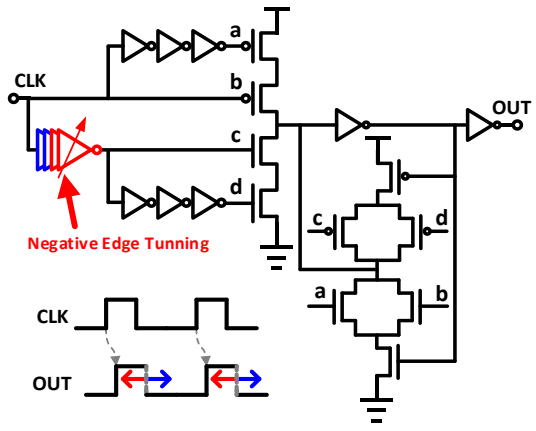


Fig. 4: Duty cycle controller first-stage HZ DAC.

of these harmonics is vital because they would otherwise alias into the band of interest. Another advantage is that multi-phase sampling attenuates uncorrelated jitter noise, and hence suppresses effects of clock jitter. Multi-phase sampling relaxes the phase noise requirement of the clock by an estimated 5.6dB.

B. Continuous-time bandpass delta-sigma modulators

CTBPDSMs are inherently suited to multi-phase sampling thanks to their small size – four sub-ADCs measure only a total of 390µm x 140µm. Another essential advantage of CTBPDSMs is that quantization noise is highly uncorrelated allowing an SNR improvement of 3dB for every doubling in the number of sub-ADCs. (In contrast, Nyquist ADCs could not be used as the quantization noise of parallel Nyquist ADCs tends to be correlated). Moreover, clock jitter-induced noise among different sub-ADCs is highly uncorrelated and therefore also benefits from a 3dB improvement every doubling of ADCs.

Beyond the benefits of multiphase sampling, there are several practical benefits to using multiple sub-ADCs per element. Although a constant ADC FoM predicts the same power when using multiple ADCs, we see the following benefits: 1) the sub-ADC power is much smaller simplifying power routing; 2) device mismatch is averaged out among the sub-ADCs; 3) the much smaller sub-ADC size means relaxed routing for time-critical feedback loops, and; 4) flexibility in trading power and performance through enabling and disabling sub-ADCs.

Fig. 3 shows the implementation of the sub-ADC array. The multi-phase sampling clocks are generated by an on-chip per-element delay-lock-loop (DLL). The ADC output bit-streams are digitally aligned. A pre-adder sums the bit-streams together, forming a combined 4G/s 5-bit stream. To facilitate testing, each sub-ADC bit-stream is gated by AND gates, so that we can observe arbitrary combinations of sub-ADCs.

The sub-ADCs are identical, except that they sample at different clock phases. The sub-ADCs employ a 4^{th}-order architecture similar to [2]. Single op-amp resonators are adopted for power efficiency. Since the coefficient of the first-stage Return-to-Zero (RZ) DAC is small, this RZ DAC is omitted to save power and reduce noise with little stability penalty. In this work, we introduce duty-cycle control of the Half-delay return-to-Zero (HZ) feedback DAC, to optimize the ADC linearity and stability. The duty cycle of the first-stage HZ

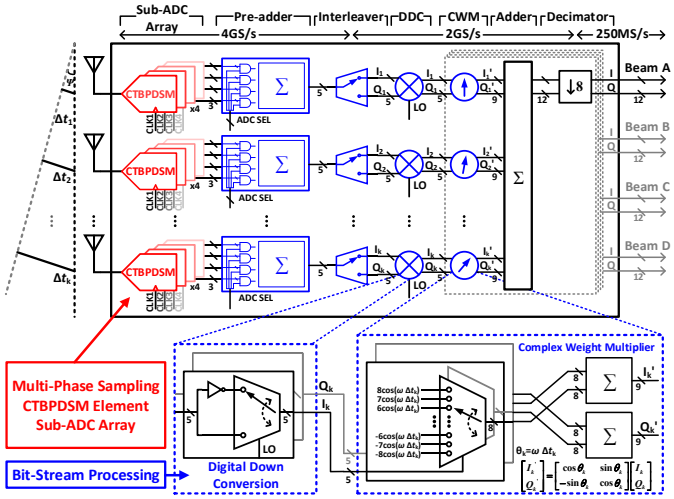


Fig. 5. System architecture of bit-stream processing digital beamformer with multi-phase sampling sub-ADC array and bit-stream processing.

current DAC is critical to the linearity and stability of the CTBPDSM. We tune the DAC clock duty cycle with a delay chain (Fig. 4 [5]) to optimize the positions of NTF/STF zeros and poles. Behavioral simulations indicate that this duty-cycle optimization reduce harmonics related to the DAC by ~10dB.

III. Digital Beamformer System Architecture

Fig. 5 shows the system architecture of the bit-stream-processing digital beamformer. Four CTBPDSM sub-ADCs digitize each 1GHz IF input. These four ADCs share the same 1GHz IF element input, but each sub-ADC samples on a different phase (CLK1, 2, …) of the 4GHz clock. The four sampling clock phases, spaced in 90-degree increments, are generated by a Delay Lock Loop (DLL). The sub-ADC outputs are digitally synchronized to a single 4GHz digital clock domain and summed. The combined ADC output is interleaved to reduce the sample rate by a factor of two to 2GS/s. Interleaving takes advantage of the 4x relationship between the sampling rate and the IF input frequency. Because the I and Q LO mixing sequences are alternately 0, we can dispense with half of the samples fed to the I and Q down-conversion mixers. Digital Down-Conversion (DDC) down-converts the half-rate interleaved streams to baseband I and Q signals. 10-bit Complex Weight Multiplication (CWM) rotates the baseband I/Q bit-stream vectors. An adder combines 16 phase-shifted signals to generate a beam. Finally, the beam is decimated by 8 by a 4th-order CIC decimator to produce a 250 MS/s 12-bit beam output. Four sets of CWMs, summers, and decimators produce four independent instantaneous beams.

Bit-stream processing (BSP) efficiently supports the 0.256TS/s aggregate sampling rate of the 64 4GS/s ADCs. In BSP [2], the quantizer outputs of the CTBPDSMs are directly processed without filtering or decimation. BSP takes advantage of the short digital word length to implement down-conversion, and weight multiplication with simple digital MUXes, saving power and area compared to a conventional DSP approach. The digital beamform processing for all four beams occupies 0.14mm^2 and consumes 200mW.

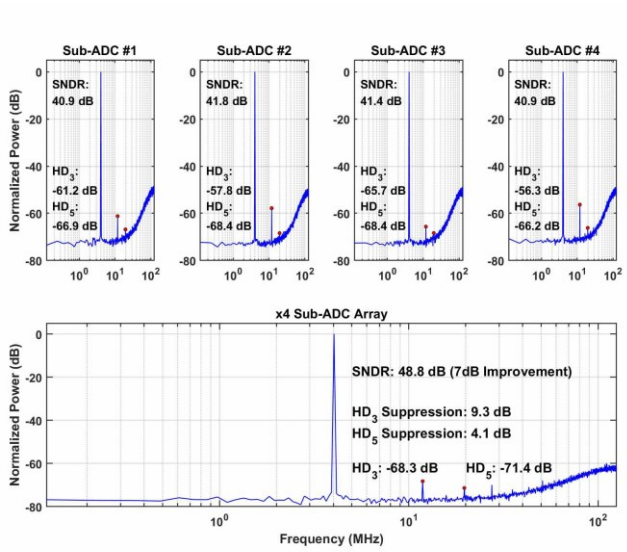
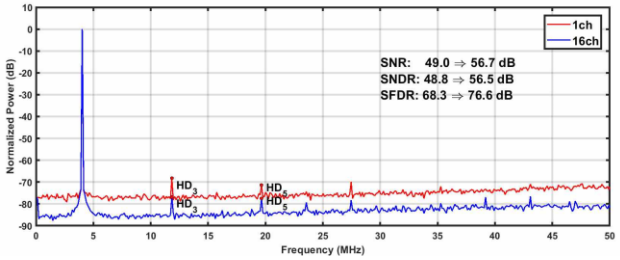


Fig. 6. Measured power spectra of four sub-ADCs (top) and combined 4x sub-ADC array (bottom).

IV. Measurements

The prototype 16-element four-beam beamformer is fabricated in 40nm CMOS and occupies a total area of 4.6mm^2 (Fig. 9). The active area of the 64 sub-ADCs is 0.9mm^2. Fig. 6 shows the measured power spectra for a single sub-ADC and for four combined sub-ADCs. The measurements confirm two advantages of using multi-phase sub-ADC array: 1) the overall SNDR increases by 7dB because of the thermal noise, jitter noise and quantization noise are decorrelated among sub-ADCs; and 2) the combined HD3 and HD5 are improved by 9.3dB and 4.1dB[1]. Fig. 7 shows the measured power spectrum of the entire



Modulation	512QAM	1024QAM	2048QAM
Constellation Diagram			
EVM	-40.4dB	-40.3dB	-39.9dB
Symbol Error Rate	<10^{-4}*	<10^{-4}*	<10^{-4}*
Symbol Rate	5M/s	5M/s	5M/s
Data Rate	45Mbps	50Mbps	55Mbps

* No error symbols found in 16000 symbols

Fig. 7. Measured power spectra (top) and measured constellations (bottom) for the 16-element digital beamformer IC.

[1] HD3, HD5 are -59, -67.3dB if the ADCs are combined in-phase. With multi-phase sampling the measured HD3, HD5 are -68.3, -71.4dB corresponding to improvements of 9.3, 4.1dB, respectively.

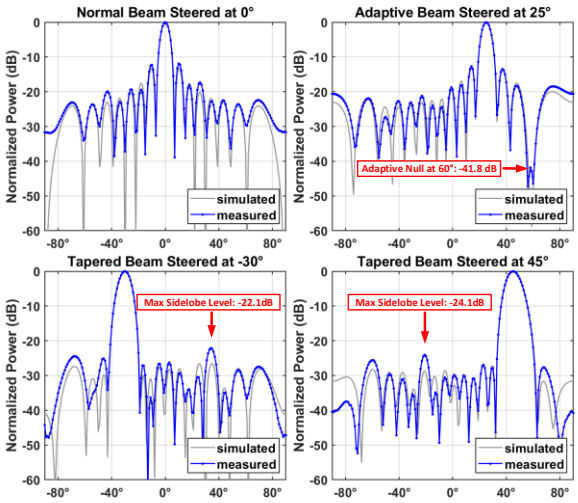


Fig. 8: Measured beampatterns overlaid on simulated beampatterns.

16-element, 64 sub-ADC. The measured SNDR is 56dB (9.1-bit ENOB) and SFDR is 77dB when the beam is steered to 45°. This high SNDR allows the prototype beamformer to receive 2048QAM without symbol errors in 16000 test symbols. The measured EVMs are -40.4dB, -40.3dB, -39.9dB for 512QAM, 1024QAM, 2048QAM respectively. The total power consumption of the IC is 2W.

As shown in Fig. 8, the measured beampatterns are near ideal. Digital beamforming enables more advanced beampatterns such as adaptive nulls and tapered beams. As an example, the adaptive null in Fig. 8 has a measured 41.8dB rejection ratio. Also shown in Fig. 8, tapering reduces the measured nearest side-lobe power by 14dB for steering angles of -30 degrees and 45 degrees.

V. Conclusion

Multi-phase sampling with multiple sub-ADCs per element is introduced to overcome the ADC linearity bottleneck of the large-scale digital beamforming. The measured HD3 suppression is 9dB. The clock phase-noise requirement is relaxed by 5.6dB compared to single-element CTBPDSM. A total of 64 4GS/s sub-ADCs along with digital beamform processing are integrated onto a single prototype chip. Bitstream processing efficiently forms four beams from the aggregate 0.256TS/s data stream generated by the ADC array. The measured overall SNDR and SFDR are 56dB and 77dB, respectively. This excellent performance is verified by 2048QAM modulation testing showing a measured EVM of -39.9dB.

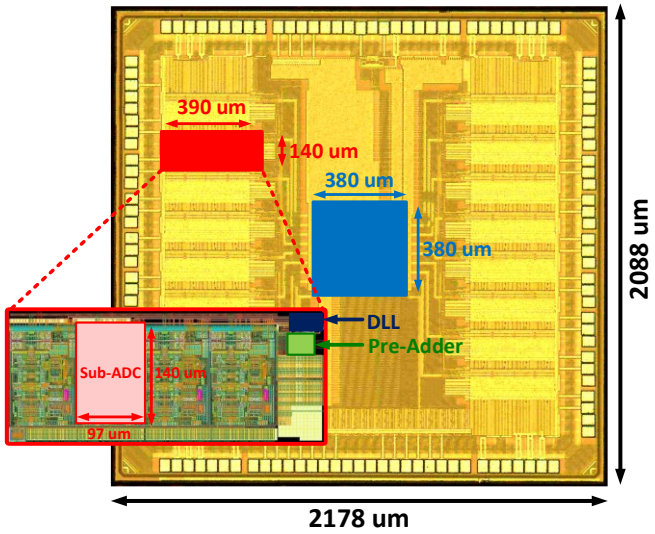


Fig. 9: Die micrograph and layout of the element sub-ADC array.

TABLE I
Performance Summary

# of Elements	16
# of Simultaneous Beams	4
Aggregate Sample Rate	0.256TS/s
Bandwidth	100MHz
Array SNDR	56.5dB
Array SFDR	76.6dB
Coefficient Resolution	10bits
Adaptive Null	-41.7dB
Multiple Beam	Supported
Tapering Beam	Supported
Active Area	1.04mm^2
ADC Power (64 sub-ADCs with DLLs + Data Alignment +Pre-adders)	1.8W
Digital Power	200mW
Total Power (64 sub-ADCs + Clock + DBF)	2W
Integration	Bandpass ADC + Digital Beamformer
Technology	40nm CMOS

Acknowledgment

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