A 5.8GHz Digital Arbitrary Phase-setting Type II PLL in 65nm CMOS with 2.25° Resolution

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***Abstract* — A fully-integrated 5.8GHz PLL modulator implemented in 65nm CMOS achieves digitally-controlled arbitrary phase generation. The PLL consists of a Type II fractional-N PLL with a 1-bit TDC as its PFD. Digital phase setting, which operates by adding a proportional signal to the PFD output, is incorporated in the PLL. The prototype achieves an average phase resolution of 2.25° and a phase range of more than 720°. The entire PLL and output buffer consumes 11mW.**

I. Introduction

Accurate phase control of high-speed signals is required in serial links, radar, beam-steering, clock distribution and medical imaging systems. One of the main challenges in realizing these applications in CMOS is the implementation of a precise, flexible, and physically small phase shifter [1,2]. Multi-phase VCOs haves limited resolution, RF phase shifters are expansive and hard to design, and baseband phase shifters require bulky components [3]. On the other hand, phase interpolation requires quadrature inputs, has limited linearity and is prone to phase error due to amplitude variation.

We present a digital PLL architecture that can both generate an arbitrary frequency and also precisely set the phase of this output signal. We achieve phase control in the digital domain; no additional analog circuits are required other than the PLL itself. This phase generation mechanism consumes little power, and it does not affect the phase noise of the PLL. This work presents a fully integrated 5.8GHz PLL modulator for arbitrary phase generation in 65nm CMOS. The modulator utilizes a Type II frac-N PLL architecture with a 1-bit TDC as its PFD. The system achieves a measured 2.25° phase resolution and more than 720° of phase range.

II. Overview of the Phase Control Mechanism

This work presents a new mostly-digital fractional-N PLL architecture to implement precise, high-resolution programmable setting of phase. To explain the new approach we first consider the most straightforward way of achieving a phase change at the output of a PLL which is to introduce a time delay Φ to the input reference path as shown in Fig. 1(a). Instead, we achieve the same result by adding a signal $K_{pd}\cdot\Phi$ at the PFD output that is proportional to the PFD gain, K_{pd}, as show in Fig. 1(b). In the first case, the output phase θ_o is

$$\theta_o = \frac{K_o K_{pd} F(s)}{s}(\theta_i + \Phi - \theta_o) \quad (1)$$

where F(s) is the loop filter transfer function, K_o is the VCO gain and θ_i is the input reference phase. In the second case, θ_o is

$$\theta_o = \frac{K_o F(s)}{s}(K_{pd}(\theta_i - \theta_o) + K_{pd}\Phi) \quad (2)$$

And in both cases, θ_o can be represented as

$$\theta_o = \frac{K_o K_{pd} F(s)}{K_o K_{pd} F(s) + s}(\theta_i + \Phi) \quad (3)$$

Comparing equation (3) to a standard PLL's transfer function

$$\theta_o = \frac{K_o K_{pd} F(s)}{K_o K_{pd} F(s) + s}(\theta_i) \quad (4)$$

We see that the resulting phase change at the output of the PLL is Φ times the PLL closed loop response in equation (4). Using this phase setting technique in combination with a digital PLL architecture, very precise phase can be set. Moreover no additional analog circuitry is required.

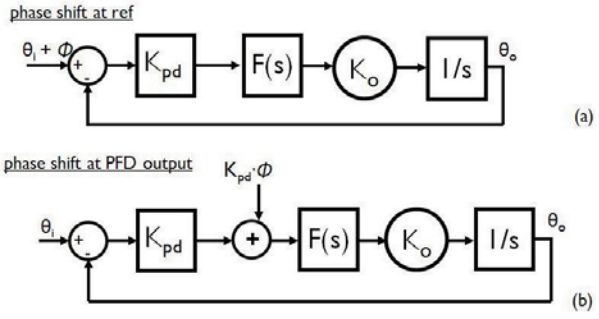

Figure 1: (a) and (b) Two conceptual approaches to phase setting

In an analog PLL, the $K_{pd}\cdot\Phi$ signal addition might be done by adding a current proportional to K_{pd}, (usually proportional

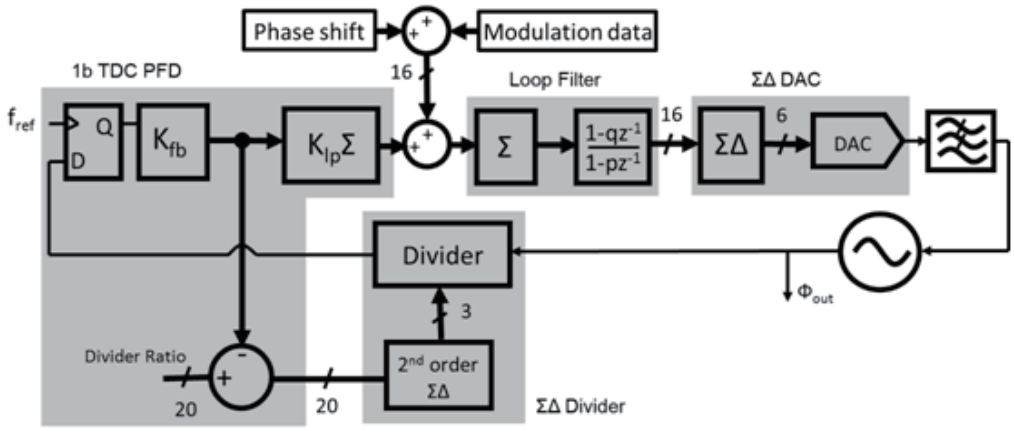

Figure 2: PLL modulator architecture

to the charge pump current), and the desired phase shift. However, this analog approach is impractical, because it requires a very well-controlled and programmable current source. Instead, we introduce a digital PLL implementation of this concept that avoids the limitations of the analog approach. In this work, a digital 1-bit TDC PFD with a phase alignment loop introduced in [4] is used. The advantage of this approach is that a digital phase-shift equivalent of $K_{pd} \cdot \Phi$, matched to the PFD gain, can be added at the output of the PFD. Since the PFD gain is digitally well-controlled, very accurate phase shifting can be achieved. The output phase change is only dependent on digital parameters. This allows almost infinite theoretical phase resolution. In practice, phase resolution is limited by phase noise and the length of the phase shifting code word.

III. PLL Architecture

The phase-setting PLL, shown in Fig. 2, leverages the oversampling 1-bit TDC digital architecture presented in [4]. Its digital nature and precise PFD gain is very well suited for our goal. The architecture mainly consists of a 1-bit TDC PFD, a loop filter, a 6-bit resistor-string ΣΔ DAC, a 2nd order ΣΔ fractional-N divider and a VCO. A 1-bit TDC PFD compares a 430MHz reference clock with the divided down feedback signal. After passing though the digital loop filter, the digital output is converted to analog by a 6-bit resistor-string ΣΔ DAC and fed to the VCO. An 8-15 programmable divider, controlled by a 3-bit 2nd order ΣΔ modulator, divides down the VCO output. Finally, a simple power-amplifier, implemented as a two-stage self-biased amplifier, buffers the VCO output (Fig. 3). Everything in the loop, with the exception of VCO gain is digital, and therefore the loop characteristics can be digitally controlled.

In the proposed PLL scheme, phase is adjusted adding a 16-bit word to the output of the digital PFD, before the second integrator. As discussed earlier, a PLL's output phase can be shifted by adding a proportional signal at the output of the PFD. Since most of the loop characteristics are digitally controllable, the 16-bit digital value can be set to achieve a precise phase. The phase shift precision is limited only by the 16-bit code word resolution. The instantaneous phase accuracy is limited only by the PLL's phase noise. We introduce a Type II PLL characteristic helps to substantially reduce any phase error compared to the reference clock.

Phase modulation can also be introduced through the same port as the phase shift. Digital modulation data is added to the phase shift data and applied to the output of the PFD. Consequently the PLL can achieve both phase modulation and phase setting.

A. 1-bit TDC PFD

One of the key components in this approach is the 1-bit TDC PFD with a phase alignment loop. Unlike conventional TDC PFDs, this 1-bit TDC, which is simply a flip flop, has no linearity or mismatch issues. The reference clock samples the divided down VCO output on its rising edge and determines whether the VCO output is ahead or behind. Oversampling increases the amount of information provided by the PFD. Using an ADC analogy, a multi-bit TDC is akin to flash ADC, whereas the oversampled 1-bit TDC is analogous to oversampled ADC. The reference clock is much faster than the loop bandwidth to achieve this oversampling. For this oversampling TDC to work, dithering is also required, otherwise the output might be stuck at 1 or 0. Fortunately dithering comes almost for free in this architecture in the form of quantization noise from the divider. The ΣΔ controlled feedback divider of the PLL introduces significant ΣΔ quantization noise to the divided down VCO output and dither the signal. The final output of the TDC is integrated to remove the ΣΔ noise, shown in Fig.2 as the $K_{lp}\Sigma$ block.

An additional feedback loop, from K_{fb} output to the divide ratio shown in Fig. 2, minimizes the phase difference between the reference clock and the divided-down clock. This additional feedback avoids the problem that would otherwise occur with a 1 bit TDC when the phase difference is large causing the 1-bit TDC to rail to 1 or 0. The output of the TDC phase detector is scaled by a factor, K_{fb} and fed back to the divider ratio input. The feedback signal is subtracted from the divide ratio as shown in Fig. 2.

B. Type II PLL

We introduce a type II PLL architecture in this design to remove the dc phase error, which is prone to variation, associated with a type I PLL such as [4]. Type II architecture improves the phase shift reliability and also suppresses close-to-carrier up-converted flicker noise.

The extra feedback loop in the PFD introduces a differentiation in the overall loop that cancels the integration and therefore without another integral in the loop, this PLL is type I, as in [4]. However there is no fundamental reason why the 1-bit TDC PFD cannot be used to realize type II architecture.

An additional integrator and a stabilizing zero are required to achieve type II behavior. Therefore to stabilize the PLL, a digital pole zero pair is added to the loop filter, shown in Fig. 2 after the second summation. Designing the pole zero pair presents a challenge, since it's in the discrete time domain, and the VCO is in the continuous time domain. To design the pole zero pair, we first assume the system is continuous time and design an analog transfer function. Then by using a simple bilinear transform, $s = \frac{2}{T}\frac{z-1}{z+1}$ we get the discrete time domain transfer function and from it the digital pole zero pair can be derived.

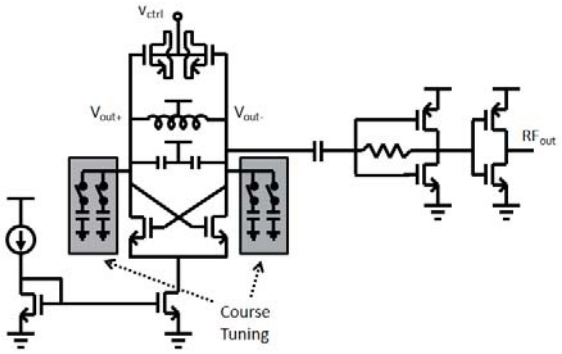

Figure 3: VCO schematic and output buffer

IV. Results

The prototype is implemented in 65nm CMOS and occupies 0.133mm^2. A die micrograph is shown in Fig. 4. The entire device consumes 11mW, including the estimated 3mW power consumption of the output buffer. The analog circuitry consumes 8mA from a 1V supply, and digital circuitry consumes 3mA from a 1V supply.

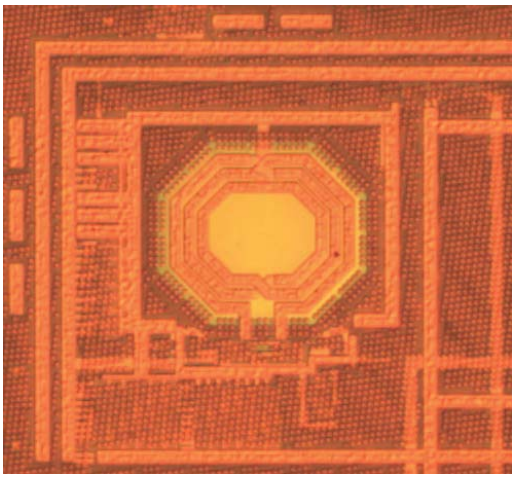

Figure 4: Die micrograph of 0.133mm^2 65nm CMOS prototype.

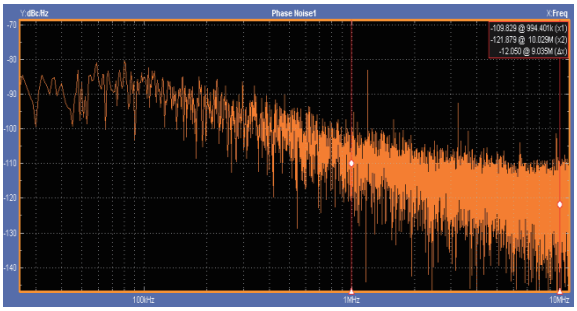

Figure 5: Phase noise plot of the Type II PLL.

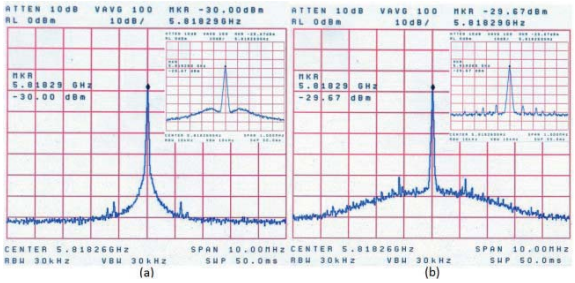

Figure 6: (a) Type II PLL spectrum and zoomed in 1MHz spectrum (b) Type I PLL spectrum and zoomed in 1MHz spectrum with the same loop parameters as the type II in (a)

The 5.8GHz PLL achieves a measured phase noise of -110dBm at 1MHz offset and -122dBm at a 10MHz offset. The measured rms jitter is 1.03ps. The phase noise plot of the type II PLL is shown in Fig. 5. Type II behavior of the loop suppresses in-band noise below 100kHz. Type II operation can be enabled or disabled in the prototype with all

parameters staying the same, except that the second integrator is turned off in type I mode. Measured spectrum profiles for Type I and Type II modes are compared in Fig. 6. As expected, the type II mode suppresses in-band noise much better than type I.

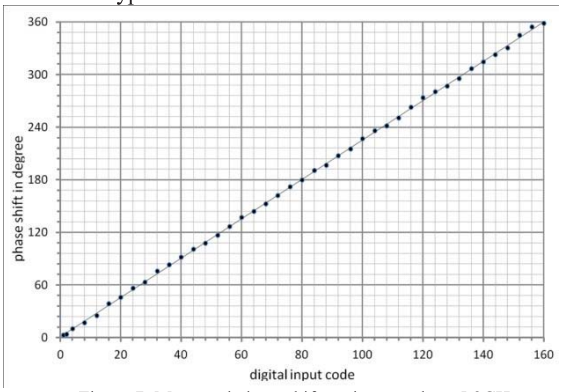

Figure 7: Measured phase shift vs. input code at 5.8GHz.

Fig. 7 shows a plot of the measured input digital code versus phase shift from 0-360°. Phase shift is measured by measuring the average phase difference between two phase-setting PLLs, with one generating a fixed phase to serve as a measurement reference. An average phase shift of 2.25° or 7.3bits of phase resolution and a phase range of more than 720° are achieved. The maximum phase shift is limited by the size of the internal digital buffers, and the minimal phase shift is limited by phase noise. A phase shift of 90° settles to within 3° accuracy within 10µs. The modulator is capable of most PSK modulations. The constellation plot of a 30.05 kHz 8-nary PSK is shown in Fig. 8. The eight symbols are well apart which tells us that there is no overshoot or ringing when setting the phase. Modulation data is generated externally and feed to the prototype. The measured performance and a comparison with recent works are summarized in Table 1.

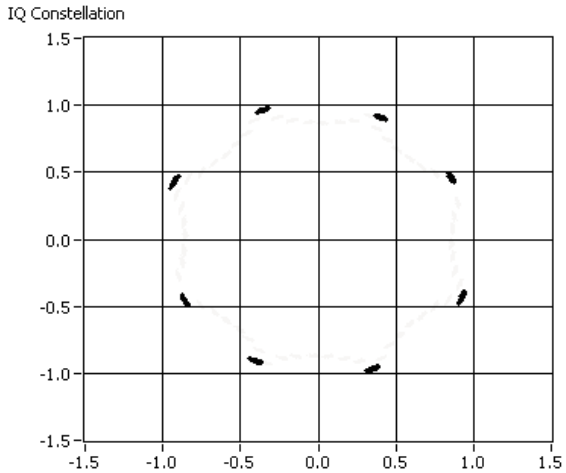

Figure 8: Constellation plot of 30 kHz 8-nary PSK

TABLE 1
Results summary and comparison with other work.

	This Work	[3]	[5]	[6]	[7]
process	65nm CMOS	0.25um CMOS	0.18um CMOS	MEMS	MEMS
frequency	5.8GHz	5.2GHz	4GHz	1-2GHz	100MHz-40GHz
phase shift resolution	2.25°	10°	N/A	5.625°	22.5°
power consumption	11mW	61mW	66mW	N/A	N/A
modulation	PSK	64-QAM	OOK	N/A	N/A

VII. Conclusion

In this work, a novel arbitrary phase generating PLL is presented. Here, by adding a digital signal at the output of a digital PFD, a well-controlled phase with unprecedented resolution of 2.25° and a phase range of more than 720° is achieved. Unlike other schemes, there is no signal loss since the phase is directly introduced in signal generation. A type II digital PLL with 1-bit TDC removes variation-prone DC error present in a type I digital architecture. The new architecture is also capable of phase modulation.

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