A 1-GHz 16-Element Four-Beam True-Time-Delay Digital Beamformer

Sunmin Jang, *Student Member, IEEE*, Rundao Lu, *Member, IEEE*, Jaehun Jeong, *Member, IEEE*, and Michael P. Flynn, *Fellow, IEEE*

***Abstract*— Phased arrays are widely used due to their low power and small area usage. However, phased arrays depend on the narrowband assumption and, therefore, are not suitable for high-bandwidth applications. Emerging communication standards require increasingly higher bandwidths for improved data rates, which results in a need for timed arrays. However, high power consumption and large area requirements are drawbacks of radio frequency (RF) timed arrays. To resolve these issues, we introduce the first true-time-delay digital beamforming IC, which eliminates beam squinting error by adopting a baseband true-time-delay technique. Furthermore, we present a constant output impedance current-steering digital-to-analog converter (DAC), which improves the spurious-free dynamic range (SFDR) of a bandpass delta–sigma modulator by 7 dB. Due to the new DAC architecture, the 16-element beamformer improves SFDR by 13.7 dB from the array. Measured error vector magnitudes (EVMs) are better than 37 dB for 5-MBd quadratic-amplitude modulation (QAM)-64, QAM-256, and QAM-512. The prototype beamformer achieves nearly ideal beam patterns for both conventional and adaptive beamforming (i.e., adaptive nulling and tapering). The difference between normalized measured beam patterns and normalized simulated beam patterns is less than 1 dB within the 3-dB beamwidth. The beamformer, including 16 bandpass analog-to-digital converters (ADCs) occupies 0.29 mm^2 and consumes 453 mW in total power.**

***Index Terms*— Delay line, digital beamforming, linear array, linearity, multiple-input multiple-output (MIMO), phased array, receiver, true-time-delay.**

I. Introduction

PHASED arrays use phase shifting to mimic time delay and are widely used due to their relatively simple implementation and low power consumption. However, phase shifting only approximates time delay, which is not identical to the actual time delay. Thus, phased arrays suffer from beam squinting [1] and array inter-symbol interference (ISI) [2], which is discussed further in Section II. In emerging communication applications, high bandwidths are required to support high data rates and large arrays are desirable due to the high path loss of millimeter waves [3]. However, higher bandwidths and large arrays suffer from greater levels of beam squinting [1] and array ISI [2].

Radio frequency (RF) timed arrays [4], [5] partly address this challenge by introducing RF time delays. Although RF timed arrays address the problem of beam squinting, they are usually limited to a single beam. Chu and Hashemi [6] describe a multi-beam RF timed array; however, a drawback is that dividing a signal in the RF domain causes signal power loss [7]. Also, RF timed arrays are prone to process-voltage-temperature (PVT) variation and delay variation over the bandwidth range. The maximum time delay in [4] and [5] is limited to 1.7 ns and 550 ps, respectively. Furthermore, large die size (0.6 and 0.07 mm^2, respectively) and high power consumption (52 and 90 mW per element, respectively) make RF delay unsuitable for large arrays. We present a baseband true-time-delay digital beamformer (DBF) with a measured beam squinting level less than 1° and a power consumption of only 28 mW per element.

The advantage of large arrays is also limited by analog-to-digital converter (ADC) nonlinearity. The array gain allows the SNR of the entire receiver to improve by 10 log N dB, where N is the array size. However, the IMD3 of the entire receiver is not improved from the array gain when the dominant nonlinearity is systematic[1] [7]. Therefore, the systematic nonlinearity of a single element can limit the performance of an array, which means that beyond a certain array size, increasing array size does not further increase signal to noise and distortion ratio (SNDR). We introduce a new feedback digital-to-analog converter (DAC) architecture to improve ADC linearity. Our new feedback DAC architecture eliminates the dependency of the DAC's output impedance on input code, which increases the spurious-free dynamic range (SFDR) of the ADC by 7 dB.

This paper is an extension of [8] and is organized as follows. Section II discusses the limitations of phased arrays. Section III provides a mathematical explanation of baseband true-time-delay. Section IV introduces our proposed architecture. It describes the baseband digital true-time-delay beamformer and the continuous-time bandpass delta–sigma modulator (CTBPDSM) with a constant output impedance current feedback DAC. Section V presents measurement results and Section VI concludes this paper.

Manuscript received September 10, 2018; revised December 31, 2018; accepted January 14, 2019. This work was supported in part by the Defense Advanced Research Projects Agency (DARPA) Arrays at Commercial Timescales (ACT) and in part by a Samsung Scholarship. This paper was approved by Guest Editor Mona Hella. *(Corresponding author: Sunmin Jang.)*

S. Jang was with the Department of Electrical Engineering and Computer Science, University of Michigan, Ann Arbor, MI 48109 USA. He is now with Apple Inc., Sunnyvale, CA 94085 USA (e-mail: smjang@umich.edu).

R. Lu and M. P. Flynn are with the Department of Electrical Engineering and Computer Science, University of Michigan, Ann Arbor, MI 48109 USA.

J. Jeong is with Broadcom Corporation, Irvine, CA 92618 USA.

Color versions of one or more of the figures in this paper are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/JSSC.2019.2894357

[1] By systematic nonlinearity, we mean that the nonlinearity is identical for each element.

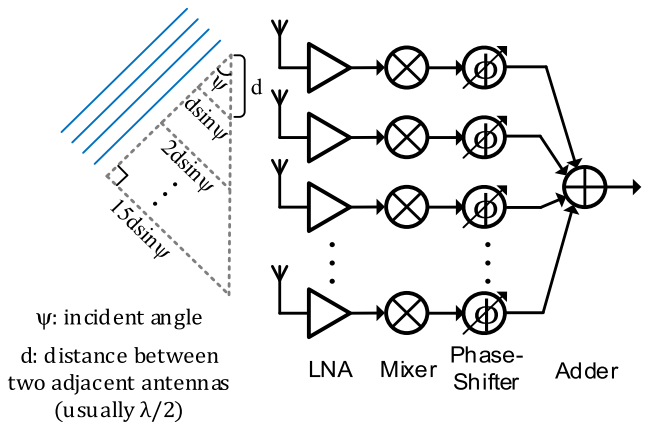


Fig. 1. Conventional phased array with 16 elements, 1-GHz center frequency, and 100-MHz bandwidth.

II. Phased Arrays

A. Operation of Phased Arrays

Phased arrays mimic time delay with phase shifting and are widely used for narrowband applications [9], [10]. To understand the principle of phase shift beamforming, we consider the 16-element, 1-GHz carrier, 100-MHz bandwidth phased array shown in Fig. 1. For a given angle, the propagation delay between the first element and the kth element is

$$\tau_k = (k-1)d\frac{\sin\psi}{c} \tag{1}$$

where τ_k is the propagation delay, k is the element number, d is the distance between two adjacent antennas, ψ is the steered angle, and c is the speed of light. $d = \lambda/2$ is chosen as a good tradeoff between 3-dB beamwidth and number of grating lobes [2]. As $c = \lambda f_c$, (1) is equivalent to

$$\tau_k = (k-1)\frac{\sin\psi}{2f_c}. \tag{2}$$

By defining $\tau = (\sin\psi/2f_c)$, (2) can be simplified to

$$\tau_k = (k-1)\tau. \tag{3}$$

When a phased array is receiving a narrowband sine wave signal centered at ω_c, the kth element receives a signal $R_k(t)$ which is

$$R_k(t) = \cos((\omega_c + \Delta\omega)(t-\tau_k)) \tag{4}$$

$$= \cos((\omega_c + \Delta\omega)t - (\omega_c + \Delta\omega)\tau_k). \tag{5}$$

Using the narrowband assumption ($\omega_c + \Delta\omega \approx \omega_c$), we simplify (5) to

$$R_k(t) \approx \cos((\omega_c + \Delta\omega)t - \omega_c\tau_k). \tag{6}$$

One can eliminate the k-dependent term $-\omega_c\tau_k$ in (6) by phase shifting the signal by $\omega_c\tau_k$ and get

$$R'_k(t) = \cos((\omega_c + \Delta\omega)t). \tag{7}$$

In this way, after phase shifting, we recover the same signal from all the array elements. Because the noise in each element is independent of each other, the addition of the phase-shifted signals (R'_k) results in a higher overall SNR.

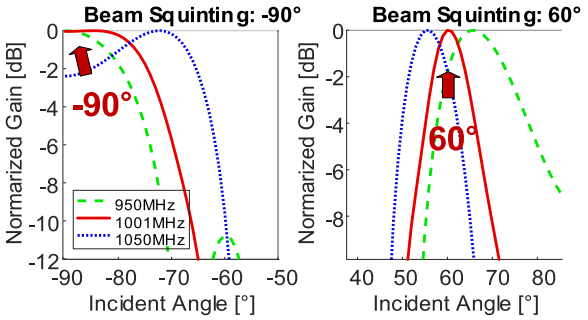


Fig. 2. Beam squinting errors for the phased array in Fig. 1.

B. Limitations of Phased Arrays

Since phased arrays are simpler to implement than timed arrays, they are more widely used. However, the operation of phased arrays is based on the narrowband assumption, which means they produce errors when used in high-bandwidth applications. Specifically, they suffer from beam squinting error in the spatial domain and array ISI in the time domain.

1) Spatial Domain (Beam Squinting Error): Beam squinting due to the narrowband approximation can be observed in the spatial domain. For example, Fig. 2 shows beam squinting errors for a 16-element, 1-GHz center frequency, 100-MHz BW beamformer. As shown in Fig. 2, the narrowband approximation causes the direction of the beam to depend on the frequency. To get a sense of how much beam squinting error occurs for phased arrays, [11] estimates the error as

$$\Delta\theta = -\frac{\tan\theta_0}{f_c}\Delta f \tag{8}$$

where $\Delta\theta$ is the squinting error, θ_0 is the steered angle, f_c is the carrier frequency, and Δf is the offset frequency. Although the squinting error in (8) is not dependent on the array size, large arrays suffer more than small arrays because the 3-dB beamwidth is narrower for large arrays. For the beamformer in Fig. 1 that has a 1-GHz center frequency and a ±50-MHz bandwidth, the estimated error for a 60° steered beam is ±5°, which matches the plot in Fig. 2. This squinting error is larger than the ±4° 3-dB beamwidth for a 16-element linear array.

2) Time Domain (Array Inter-Symbol Interference): As discussed in Section II-A, the narrowband assumption is only valid when the propagation delay to the elements can be approximated with a constant phase shift over the signal bandwidth [2]. When the propagation delay is large, phased arrays suffer from array ISI, which causes some array elements to receive different data symbols than others. For example, Fig. 3(a) shows a four-element phased array steered at 30°. In Fig. 3(a), D1–D4 represent data symbols. Antenna 1 is receiving D2, while the other antennas are receiving D1. Since D1 and D2 are independent, D2 is merely a distortion of D1, and the performance of the array degrades after beamforming. This phenomenon is called array ISI because a subsequent symbol (D2) interferes with the current symbol (D1).

The array ISI is not severe when the array has a low data rate [Fig. 3(b)], a small steered angle [Fig. 3(c)], or a small array size [Fig. 3(d)]. This is because the low data rate increases the symbol period, and smaller steered angles or small array sizes decrease the maximum propagation delay across the

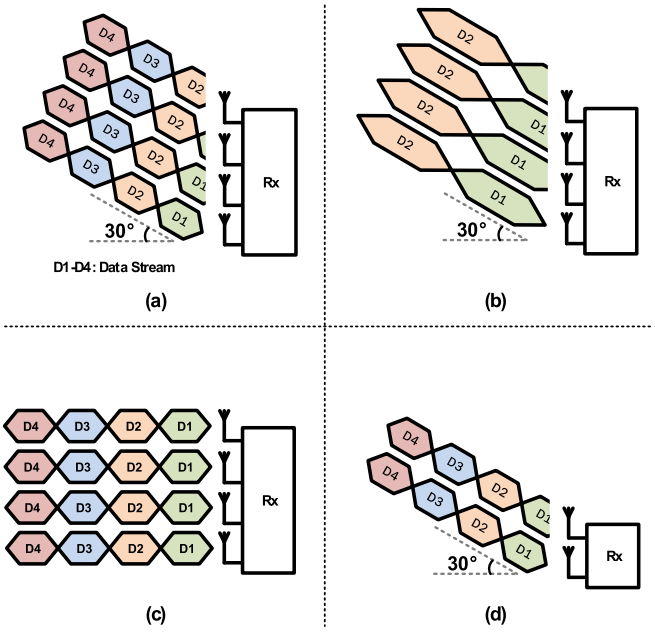


Fig. 3. (a) Example of an ISI and why it is less likely to occur when the array has (b) low data rate, (c) small steered angle, and (d) small array size.

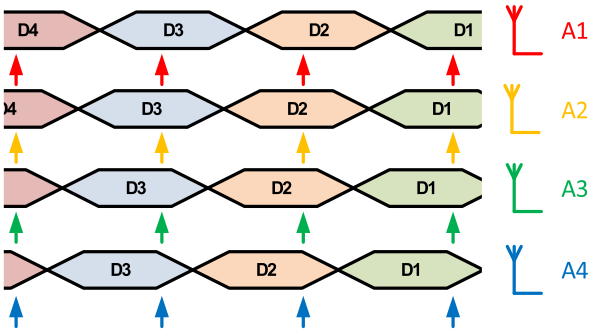


Fig. 4. Four-element uniform linear array without the array ISI.

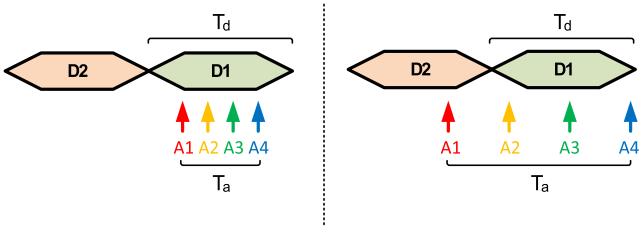


Fig. 5. Simplified diagram without (left) and with (right) array ISI.

array. However, emerging communication standards require high data rates and large arrays, making array ISI a serious limitation.

Fig. 4 gives an example of an array without the array ISI. In Fig. 5 (left), a simplified representation of Fig. 4 with a single-data stream is depicted. T_d is the symbol period, which is inversely proportional to the signal's bandwidth, and T_a is the maximum propagation delay difference across the array. In Fig. 5 (right), the array experiences array ISI as A1 receives D2, while A2–A4 receive D1. The array cannot avoid the array ISI when T_a is larger than T_d [2]. Therefore, the array needs to satisfy

$$T_d \gg T_a. \tag{9}$$

Based on (2), T_a can be expressed as follows for an array size of N and $\psi = 90°$

$$T_a = (N-1)\frac{1}{2f_c} \tag{10}$$

T_d, the symbol period, can be expressed as follows for a double-sideband signal such as quadratic-amplitude modulation (QAM)

$$T_d = \frac{2}{\mathrm{BW}} \tag{11}$$

where BW is the instantaneous bandwidth. With (10) and (11), (9) is equal to

$$\frac{2}{\mathrm{BW}} \gg (N-1)\frac{1}{2f_c}. \tag{12}$$

This can be re-written as

$$N \ll \frac{4f_c}{\mathrm{BW}} + 1. \tag{13}$$

With (13), a maximum array size without the array, ISI can be calculated. For example, the array size of a uniform linear array with a 1-GHz carrier frequency and 100-MHz bandwidth needs to be much smaller than 41 elements to avoid array ISI.

III. Baseband True-Time-Delay Beamformers

As discussed in Section II, phased arrays have limitations such as beam squinting and array ISI. Baseband true-time-delay beamforming not only addresses these challenges but also allows for digital beamforming, which is highly accurate, fast, and able to generate multiple beams. However, baseband true-time-delay beamforming is complicated because baseband time delay is not equivalent to RF time delay.

A. Problem With Using Baseband Time Delay Alone

To understand why baseband time delay alone does not give a true RF time delay, we must consider an array with baseband time delay alone in Fig. 6 (top). After downconversion, the array obtains a low-frequency sine wave signal (I_{bb}) described in the following equation:

$$I_{bb} = \sin(\omega_{bb} t) \tag{14}$$

where bb stands for baseband. If we time delay I_{bb} by τ_d

$$I'_{bb} = \sin(\omega_{bb}(t-\tau_d)) \tag{15}$$

$$= \sin(\omega_{bb} t - \omega_{bb}\tau_d). \tag{16}$$

Upconverting this signal by mixing with a local oscillator (LO) signal, we get

$$I_{rf} = \sin((\omega_{bb}+\omega_{LO})t - \omega_{bb}\tau_d) \tag{17}$$

$$= \sin\left((\omega_{bb}+\omega_{LO})\left(t - \frac{\omega_{bb}}{\omega_{bb}+\omega_{LO}}\tau_d\right)\right). \tag{18}$$

As a result, (18) shows that a baseband time delay τ_d corresponds to a RF time delay of $(\omega_{bb}/(\omega_{bb}+\omega_{LO}))\tau_d$, which is much smaller than the baseband time delay τ_d but is also dependent on the baseband frequency ω_{bb}. To illustrate the problem with baseband time delay, Fig. 6 (bottom) shows

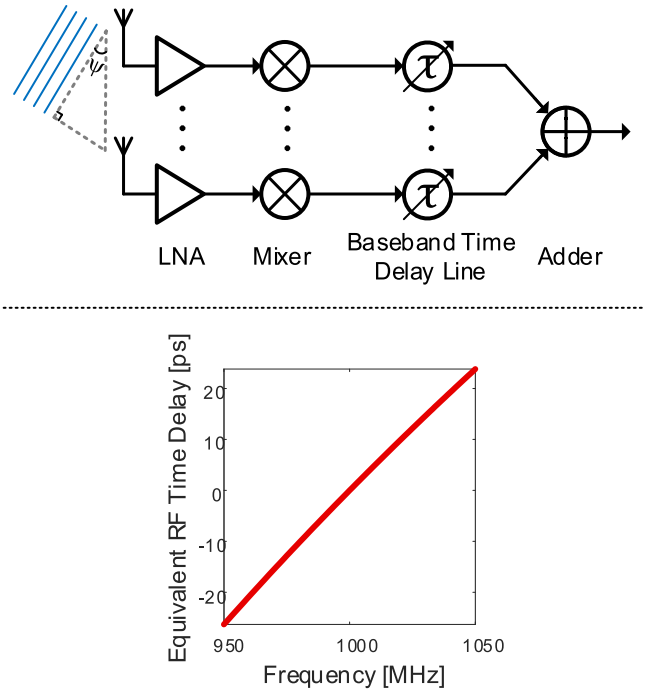


Fig. 6. System architecture of an array with baseband time delay alone (top) and equivalent RF time delay at 1 GHz for a baseband 500-ps time delay over ±50-MHz bandwidth (bottom).

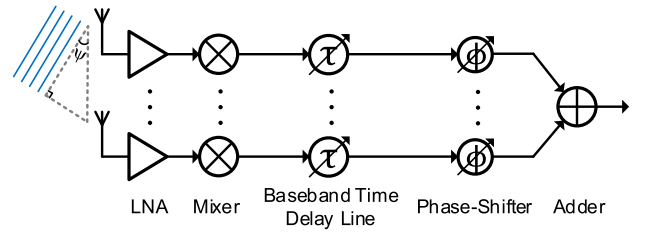


Fig. 7. System architecture of a baseband true-time-delay beamformer.

the equivalent RF time delay for a 500-ps baseband time delay over a ±50-MHz bandwidth centered at 1 GHz. In particular, for a dc signal ($\omega_{bb} = 0$), the equivalent RF time delay is always 0. A dc signal has a constant output voltage and does not change over time. Therefore, shifting or delaying a dc signal in the time domain does not result in a change in output value.

B. Combination of Baseband Time Delay and Phase Shifting

A baseband beamforming technique introduced in 1992 solves the squinting and array ISI problems for acoustic beamforming [12]. By combining phase shifting and time delay in the baseband (Fig. 7), we can eliminate squinting. To understand this, we reformulate (18) to obtain

$$I_{rf} = \sin\left((\omega_{bb}+\omega_{LO})(t-\tau_d+\frac{\omega_{LO}}{\omega_{bb}+\omega_{LO}}\tau_d)\right) \quad (19)$$

$$= \sin((\omega_{bb}+\omega_{LO})(t-\tau_d)+\omega_{LO}\tau_d). \quad (20)$$

By introducing a phase shift of $-\omega_{LO}\tau_d$ in (20), we get

$$I_{rf} = \sin((\omega_{bb}+\omega_{LO})(t-\tau_d)). \quad (21)$$

Equation (21) shows that an RF time delay of τ_d can be achieved by time delaying a baseband signal by τ_d and phase shifting the signal by $-\omega_{LO}\tau_d$, which is independent to the baseband signal frequency ω_{bb}. Regardless of the baseband frequency, an equivalent RF time delay τ_d is achieved.

As discussed in Section II, the kth element in an array has a propagation delay of τ_k. To compensate for this propagation delay, we need to apply an RF time delay of $-\tau_k$, which can be done by introducing a baseband phase shift of $\omega_{LO}\tau_k$ combined with a time delay of $-\tau_k$.

Next, let us consider a quadrature-amplitude-modulated signal $R(t)$ which is defined in the following equation:

$$R(t) = a(t)\cos(\omega_c t + \phi(t)) \quad (22)$$

where $a(t)$ and $\phi(t)$ are the amplitude and phase information. Upconversion from baseband $I(t)$ and $Q(t)$ to $R(t)$ can be expressed as

$$R(t) = [\cos(\omega_c t) \quad \sin(\omega_c t)]\begin{bmatrix} I(t) \\ Q(t) \end{bmatrix} \quad (23)$$

where

$$I(t) = a(t)\cos(\phi(t)) \quad (24)$$

$$Q(t) = -a(t)\sin(\phi(t)). \quad (25)$$

For beamforming, the kth element receives a signal $R_k(t)$ which is

$$R_k(t) = R(t-\tau_k) \quad (26)$$

$$= a(t-\tau_k)\cos(\omega_c(t-\tau_k)+\phi(t-\tau_k)). \quad (27)$$

Downconversion at element k gives the following relationship between the received baseband signals, $I_k(t)$ and $Q_k(t)$, at element k and $R_k(t)$:

$$R_k(t) = [\cos(\omega_c t) \quad \sin(\omega_c t)]\begin{bmatrix} I_k(t) \\ Q_k(t) \end{bmatrix} \quad (28)$$

where

$$I_k(t) = a(t-\tau_k)\cos(-\omega_c\tau_k+\phi(t-\tau_k)) \quad (29)$$

$$Q_k(t) = -a(t-\tau_k)\sin(-\omega_c\tau_k+\phi(t-\tau_k)). \quad (30)$$

This leads to the following relationship between $R(t)$ and the received baseband signals, $I_k(t)$ and $Q_k(t)$, at element k:

$$R(t) = \begin{bmatrix}\cos(\omega_c t) & \sin(\omega_c t)\end{bmatrix}\begin{bmatrix}\cos(\omega_c\tau_k) & -\sin(\omega_c\tau_k) \\ \sin(\omega_c\tau_k) & \cos(\omega_c\tau_k)\end{bmatrix} \times \begin{bmatrix} I_k(t+\tau_k) \\ Q_k(t+\tau_k)\end{bmatrix}. \quad (31)$$

This expression has the form

$$R = \text{Carrier} \times \text{Phase shift} \times \text{Delayed Baseband}. \quad (32)$$

Comparing with (23), we note that $I(t)$ and $Q(t)$ are recovered from $I_k(t)$ and $Q_k(t)$ by adding time delay $-\tau_k$ and phase shifting. We also note that for a narrowband signal, $-\tau_k$ is negligible and (31) becomes equivalent to conventional phased array beamforming.

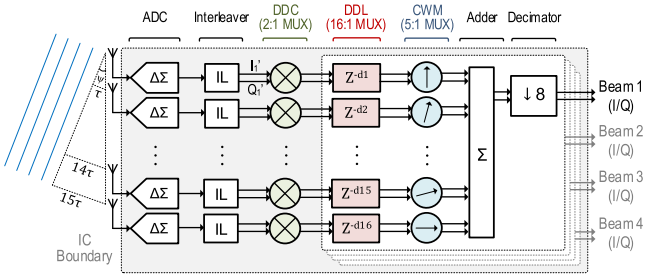


Fig. 8. System architecture of the prototype baseband true-time-delay DBF.

IV. Proposed Architecture

In this paper, we propose a true-time-delay DBF that consists of CTBPDSMs and a bit stream processing (BSP) DBF.

The system architecture of our prototype DBF is shown in Fig. 8. It consists of 16 bandpass ADCs, 16 interleavers, and 16 digital downconverters (DDCs). The bandpass ADCs are directly connected to antennas that receive IF signals centered at 1 GHz. The interleavers halve the data rate and the DDCs downconvert the digital IF signals to baseband. This is followed by four digital beamforming units, enabling the prototype DBF to generate four independent beams for multiple-input multiple-output (MIMO) [13] and other applications. Each beamforming unit has 16 digital delays lines (DDLs), 16 complex weight multipliers (CWMs), an adder, and a decimator. Digital beamforming simultaneously generates multiple beams without any SNR losses [7].

A. Introduction of Fine Phase Shifting

As we discussed, the data streams from each antenna are aligned by adding a delay of $-\tau_k$ to the kth element. However, in practice, time delay of $-\tau_k$ cannot be implemented because it is a negative time delay. To make the system causal, a constant time delay $(N-1)\tau$ is added to all the elements, where N is the array size. With the added time delay $(N-1)\tau$, the time delay of the kth element becomes $(N-k)\tau$, as τ_k is equal to $(k-1)\tau$ (see Section II-A).

Although our ADC samples the input signal at a high rate (4 GHz), the resolution of the digital time delay is still limited to 250 ps. Thus, instead of the ideal time delay $(N-k)\tau$, we actually delay the signal by the closest number of digital increments, which is denoted by $\lceil (N-k)\tau \rceil$ in Fig. 9. To compensate for this small missing delay, we introduce another fine phase shifter that shifts the phase by ϵ_k [Fig. 9 (top)], where

$$\epsilon_k = \omega_c k\tau - \omega_c \lceil k\tau \rceil. \tag{33}$$

We combine the two phase shifters into a single phase shifter to reduce both power and area usage [Fig. 9 (bottom)]. As we will demonstrate in Section V, the additional phase shifter does not introduce any observable beam squinting error for a step size of 1°.

B. Bit Stream Processing

We use BSP, which was first introduced in [14], to reduce both power and area usage. The basic idea of BSP is to replace

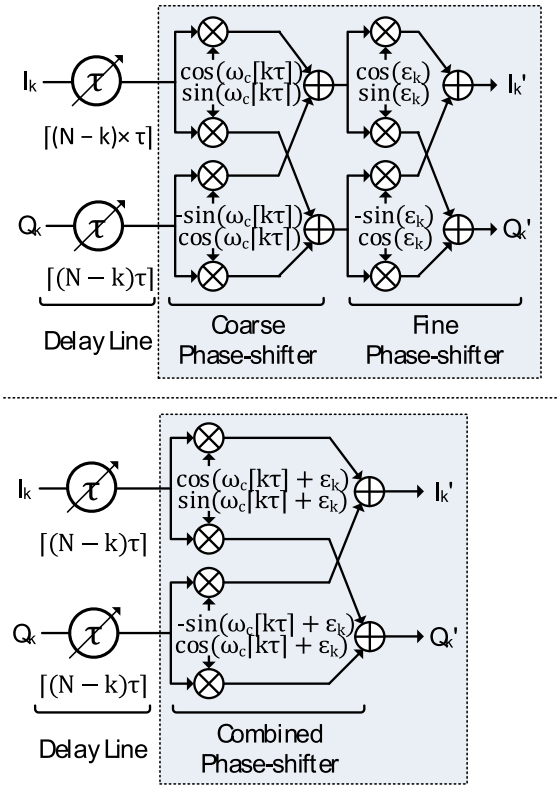


Fig. 9. System architecture of the baseband true-time-delay beamformer with an additional phase shifter to compensate the limited time delay resolution (top) and a simplified architecture implemented in this paper with a single combined phase shifter (bottom).

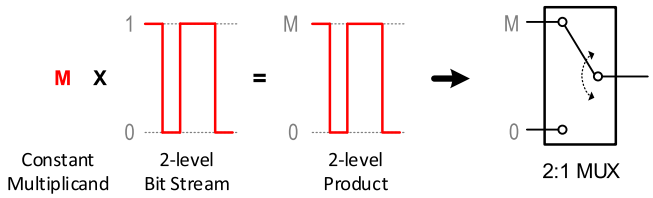


Fig. 10. Simplest example of multiplication in BSP.

bulky and power-hungry digital multipliers with digital multiplexers by performing multiplications directly on the high-speed, low-resolution bit stream generated by delta–sigma modulators.

Fig. 10 shows the multiplication in BSP of a constant multiplicand (M) and a two-level bit stream. As the product is still two-levels, a 2:1 multiplexer, which selects between 0 or M can perform this multiplication without any digital multipliers.

The implementation of the prototype DBF is detailed in Fig. 11. We increase the resolution of the bit stream to five levels[2] to achieve better modulator stability and a higher ADC SNR [15]. With the five-level bit stream, BSP is still used to perform multiplication. As we will discuss, a bit-stream resolution higher than five levels is not desirable because it necessitates multipliers or adders.

[2]The effective resolution of the ADC is much higher than five levels due to noise shaping and oversampling.

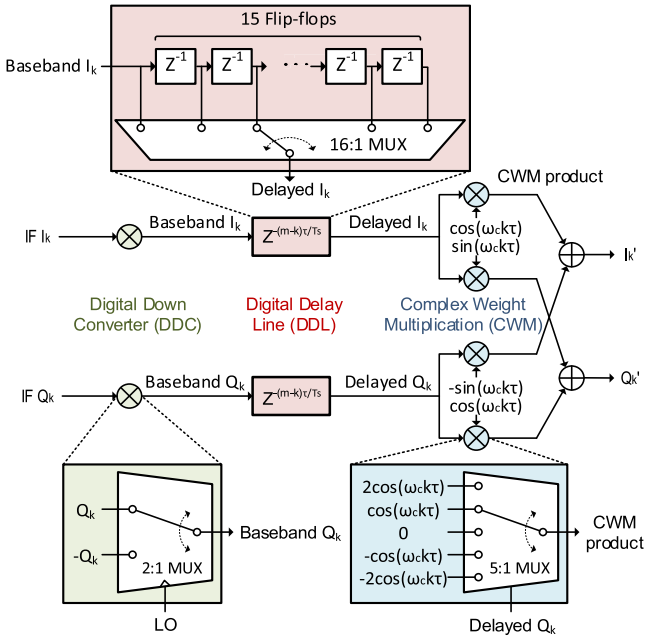


Fig. 11. Interleaved (IL)-BSP implementation of the prototype beamformer.

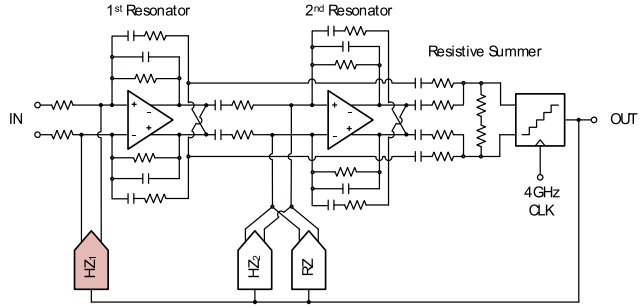


Fig. 12. System architecture of the fourth-order CTBPDSM.

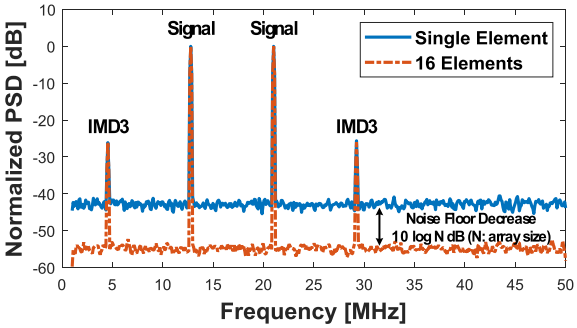


Fig. 13. Two-tone power spectral density plot for a single element and 16 elements when systematic nonlinearity is the dominant nonlinearity source.

The DDC downconverts the IF input signal to the baseband by multiplying the signal with a 1-GHz sinewave LO signal. By choosing a sampling rate four times higher than the carrier frequency, the sampled LO signal can be represented as a three-level digital signal with values of either 1, 0, or -1 [15]. As every other LO values are always 0, every other baseband I/Q values (output of the downconverter) are also 0. These zeros can be removed as they do not contain any useful information. Therefore, an interleaver is placed before the downconverter, and the zeros in the LO signal are removed. Due to the interleaver, the DBF operates at half speed without any performance loss [16]. Because the DDC performs multiplication between the two-level LO signal and a five-level bit stream (I_k/Q_k), it is implemented with a 2:1 MUX, which selects either I_k/Q_k or $-I_k/Q_k$ depending on the LO signal [16].

The DDL consists of a 15-tap shift register and a 16:1 MUX, which selects one of the outputs of the shift register. The phase shifter is implemented with a 5:1 MUX, which selects one of $2\cos\theta$, $\cos\theta$, 0, $-\cos\theta$, and $-2\cos\theta$, where θ is $\omega_c\tau_k$ in (6). As $\cos\theta$ is a digitized value, we get $2\cos\theta$ by shifting $\cos\theta$ by 1 bit, $-\cos\theta$ by flipping the sign bit, and $-2\cos\theta$ by shifting it by 1 bit and flipping the sign bit. Therefore, these five values do not need a multiplier. However, if we increase the resolution to seven-level, calculation of $3\cos\theta$ would either need a multiplier to perform $3 \times \cos\theta$ or an adder to sum $2\cos\theta + \cos\theta$. Therefore, five-level is ideal for BSP.

C. Continuous-Time Bandpass Delta–Sigma Modulator

It is well known that continuous-time bandpass modulators have inherent anti-alias filters and no flicker noise. Bandpass modulators also allow us to use digital down-mixing without I/Q mismatch. Besides these well-known advantages, bandpass modulators also have extra advantages when used for true-time-delay digital beamforming. Their high sampling rate allows us to have a fine digital time delay resolution, favoring their use in RF digital true-time-delay beamformers. In our work, 250-ps time delay resolution is achieved with a 4-GHz sampling rate. Delta–sigma modulators also enable BSP [14]. For digital beamforming with bandpass modulators, we need several digital multipliers for digital mixing and phase shifting. BSP achieves low power and small area usage by replacing the digital multipliers with multiplexers and reducing the number of decimators [15].

1) System Architecture: Fig. 12 shows the system architecture of the CTBPDSM in our work which is based on the ADC in [17]. It consists of two resonators, a resistive summer, a 4-GHz quantizer, and three feedback DACs. The modulator achieves 49-dB SNDR over a 100-MHz bandwidth centered at 1 GHz. It consumes 16 mW and occupies 0.01 mm^2.

2) Constant Output Impedance Feedback DAC: As discussed in Section I, systematic nonlinearity can limit array size. Fig. 13 shows an example of a power spectral density plot for both a single element and 16-element array when systematic nonlinearity is dominant. The power spectral density plot is normalized to the signal power to better visualize the array gain. Since the thermal noise is not correlated with the elements, we get 10 log N dB lower noise floor with N elements. However, IMD3 does not decrease because the third harmonics have the exact same phase over all elements just like the signal [7]. To understand how this correlated distortion limits the array size, let us consider the definition of SNDR

$$\text{SNDR} = \frac{P_{\text{signal}}}{P_{\text{noise}} + P_{\text{distortion}}}. \tag{34}$$

With an assumption that $P_{\text{noise}} \gg P_{\text{distortion}}$ for a single element, $P_{\text{distortion}}$ can be ignored for small arrays, and (34)

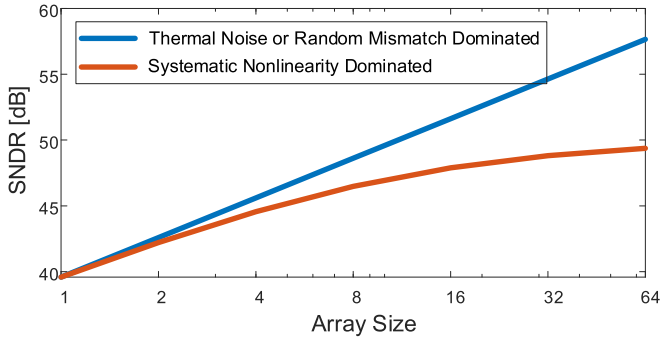


Fig. 14. Simulated example showing how systematic nonlinearity can limit the array size. The single ADC in this example has an SNR of 49 dB and an SFDR of 58 dB—This is similar to the ADCs in the prototype.

can be simplified as follows:

$$\text{SNDR} \approx \frac{P_{\text{signal}}}{P_{\text{noise}}}. \tag{35}$$

For an N-element array, P_{signal} increases by 20 log N dB, and P_{noise} increases by 10 log N dB. Therefore, for small arrays, the array gain improves SNDR by 10 log N dB.

In contrast, for large arrays whose linearity is systemically limited, $P_{\text{distortion}}$ becomes larger than P_{noise}, because the distortion increases by 20 log N dB. In this case, (34) can be simplified as follows:

$$\text{SNDR} \approx \frac{P_{\text{signal}}}{P_{\text{distortion}}}. \tag{36}$$

Thus, for large arrays, SNDR does not improve with increased array size because both the signal and distortion power increase by 20 log N dB, reducing the benefits of large arrays.

As an example, Fig. 14 shows the comparison of the simulated SNDR between beamformers with SNDR limited by thermal noise and by systematic nonlinearity. It also shows that the maximum SNDR is bounded by systematic nonlinearity. The example is based on an ADC with an SNR of 49 dB and SFDR of 58 dB, which are similar to the measurements of the prototype. In the thermal noise/random mismatch limited case, SNDR increases by 3 dB with every doubling of the array size. However, the maximum SNDR saturates at the SFDR value, limiting the benefit of large arrays.

For a single ADC, the random mismatch of the first feedback DAC is the dominant nonlinearity source [16] and dynamic element matching (DEM) is often used to mitigate the mismatch [18]. However, for arrays, DEM might not be required because random mismatch is averaged out by the addition of beamforming, which has a similar effect to DEM. Ideally, if the SFDR of an array is limited by the random mismatch, the array SFDR improves by 10 log N dB, which is the same as the SNR improvement. Therefore, for large arrays, random mismatch is not as critical as it would be for a single ADC and it is essential to manage systematic nonlinearity.

We apply a new technique to reduce the systematic nonlinearity of the feedback DAC in modulators, which is a dominant limitation in array SFDR. To understand the source of the systematic DAC nonlinearity, we consider the current steering

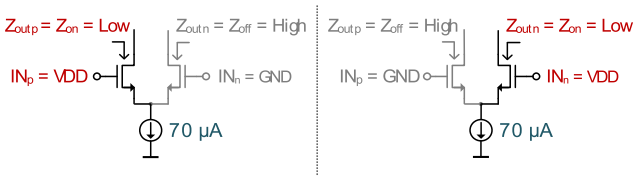


Fig. 15. 70-μA DAC cell with code-dependent output impedance.

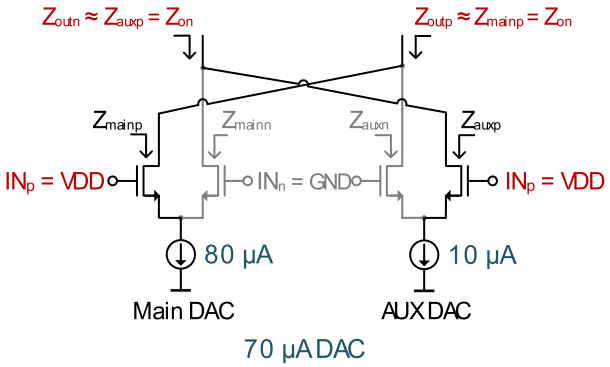


Fig. 16. Constant output impedance DAC cell.

DAC cell in Fig. 15. Ideally, a current steering DAC should have an infinite output impedance so that changes in the output voltage do not affect the output current. However, in reality, current DACs have finite output impedance. As shown in Fig. 15 (left), when input positive (IN_p) is high and input negative (IN_n) is low, the output impedance positive (Z_{outp}) is low (Z_{ON}), while the output impedance negative (Z_{outn}) is high (Z_{OFF}). In addition, if the input code changes, the output impedance also changes [Fig. 15 (right)]. Thus, the nonideal current output, due to finite output impedance, is dependent on the input code, causing systematic nonlinearity.

Fig. 16 shows how we eliminate the code dependency, by introducing an auxiliary DAC cell with the opposite digital input. As shown in Fig. 16, the auxiliary DAC cell sinks 10 μA and the main DAC sinks 80 μA in the opposite direction, making it effectively a 70-μA DAC cell. Since either the main or auxiliary DAC cell is always running for both outputs, the output impedance is always $Z_{\text{ON}}//Z_{\text{OFF}} \approx Z_{\text{ON}}$.

By including a constant output impedance that has no dependency on the input code, the ADC with a constant output impedance DAC achieves 7 dB higher SFDR than the ADC with a conventional variable output impedance DAC (Fig. 17).

V. Measurements

Fig. 18 shows a die micrograph of the prototype true-time-delay digital beamforming IC. Eight ADCs on the left and eight ADCs on the right surround the digital beamforming core at the center. Each ADC occupies 140 μm $\times$ 80 μm and the DBF occupies 360 μm $\times$ 360 μm.

The measurement setup is shown in Fig. 19. The 16 digital direct synthesizers (DDSs) generate the 1-GHz RF input signals for beam pattern measurements. A vector signal generator is used for QAM constellation measurements. No active front ends, such as low noise amplifiers (LNAs), are used.

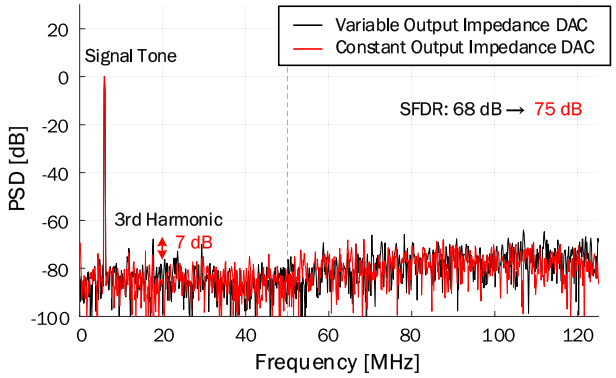


Fig. 17. (Simulation) SFDR comparison between delta–sigma modulators with a variable output impedance DAC and a constant output impedance DAC.

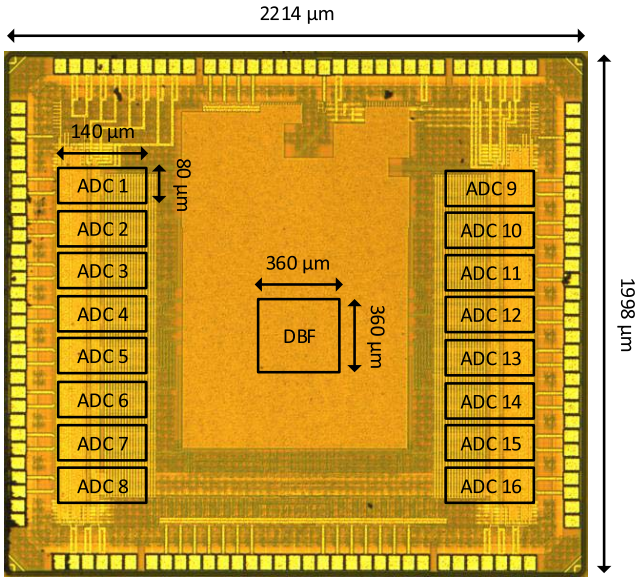


Fig. 18. Die micrograph in 40-nm CMOS (active area: 0.28 mm^2).

The vector signal generator produces a 1-GHz carrier 5-MBd QAM signal that is directly connected to the beamforming IC.

A. Beam Patterns

Fig. 20 plots measured beam patterns over a 100-MHz bandwidth for steered angles −90°, −30°, 0°, and 60°. These four beam measurement are for four simultaneous beams. For a measurement step size of 1°, the true-time-delay DBF shows no beam squinting error. This verifies the true-time-delay scheme and also demonstrates that the fine phase shifter (see Section IV) does not introduce any noticeable squinting errors.

Fig. 21 shows complete measured and ideal beam patterns for four different steered angles. The four simultaneous beam patterns are measured with different input frequencies and a step measurement size of 1°. Beam 3 and beam 4 demonstrate adaptive nulling and beam tapering, respectively. In all cases, the measured beam patterns are almost identical to simulated beam patterns. These tests demonstrate the ability of the prototype to simultaneously generate multiple beams with a range of sophisticated beamforming characteristics.

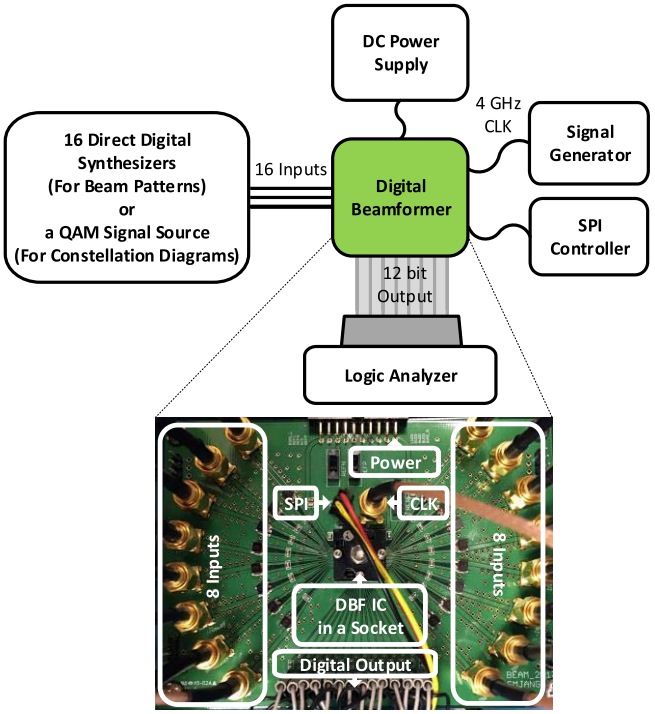


Fig. 19. Measurement setup.

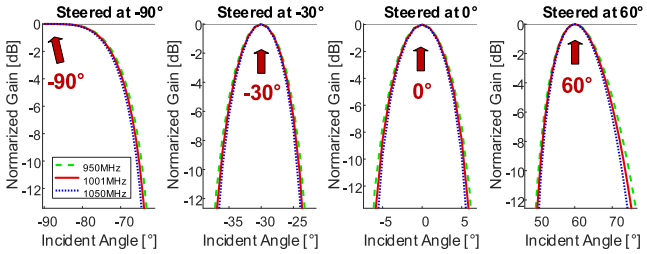


Fig. 20. Measured beam patterns for four simultaneous beams showing no beam squinting errors.

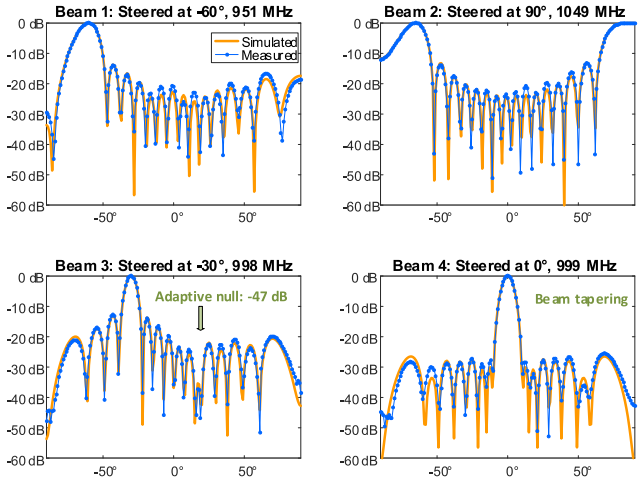


Fig. 21. Four measured simultaneous beam patterns superimposed on simulated beam patterns.

Digital beamforming facilitates sophisticated beamforming schemes. RF true-time-delay beamformers require additional gain control units such as variable gain amplifiers (VGAs) for

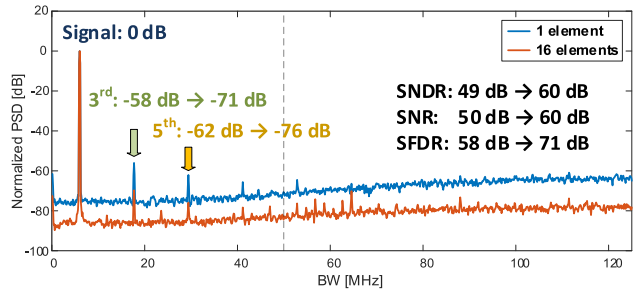


Fig. 22. Normalized power spectral density plot for a single element and 16 elements.

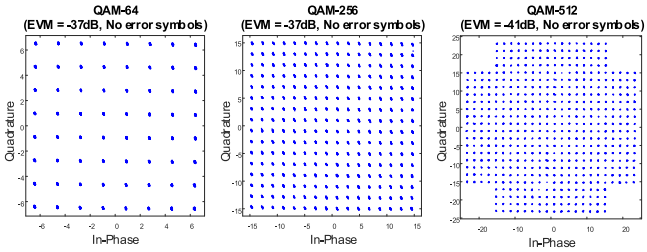


Fig. 23. QAM constellation diagrams for 5-MBd QAM-64, QAM-256, and QAM-512.

adaptive beamforming. In contrast, this digital true-time-delay beamformer can perform adaptive beamforming and tapering by tuning the gain of the phase shifters. The high-resolution 10-bit CWM in our prototype beamformer facilitates adaptive beamforming without any additional circuitry. Beam 3 is steered at $-30°$ with an adaptive null at 30°. The adaptive null attenuates interferer by -47 dB. Beam 4 is steered at 0° with a beam tapering technique. The measured tapered beam pattern has sidelobes lower than -25 dB.

B. Power Spectral Densities

Demonstrating the array gain, Fig. 22 shows the measured power spectral densities for a single element and 16 elements. To visualize the array gain, the two plots are normalized to the signal power. Therefore, the signal power is 0 dB in both plots to easily show how much the noise floor, third harmonic, and fifth harmonic are attenuated by the array. With 16 elements, the true-time-delay beamformer achieves an improvement of 11 dB in SNDR, 10 dB in SNR, and 13 dB in SFDR. Ideally, SNR should improve by 12 dB with 16 elements. However, in practice, the array gain is limited by correlated errors across the array such as shared clock jitter, supply noise, and quantization noise.

C. QAM Constellation Diagrams

Measured QAM constellation diagrams for various QAM signals are shown in Fig. 23. The beamformer achieves error vector magnitudes (EVMs) higher than -37 dB for 5-MBd[3] QAM-64, QAM-256, and QAM-512. No error symbols are observed amongst the 8000 symbols.

[3]This is the maximum modulation rate of the test signal source.

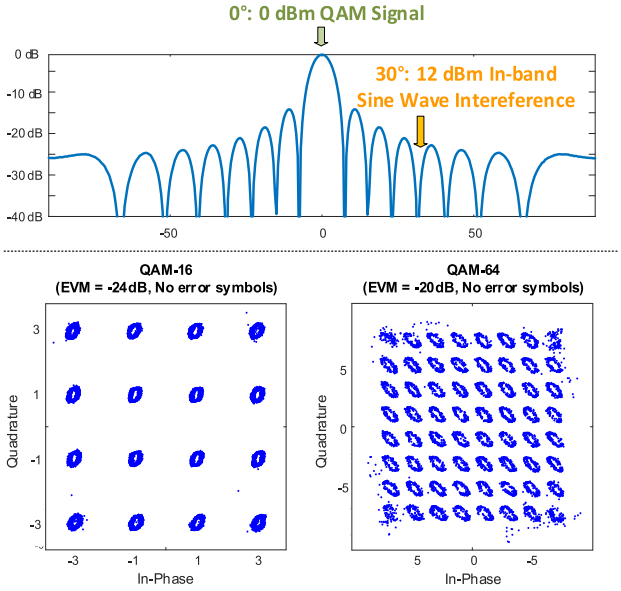


Fig. 24. Interference test setup (top) and measured QAM constellation diagrams with an in-band interference (bottom).

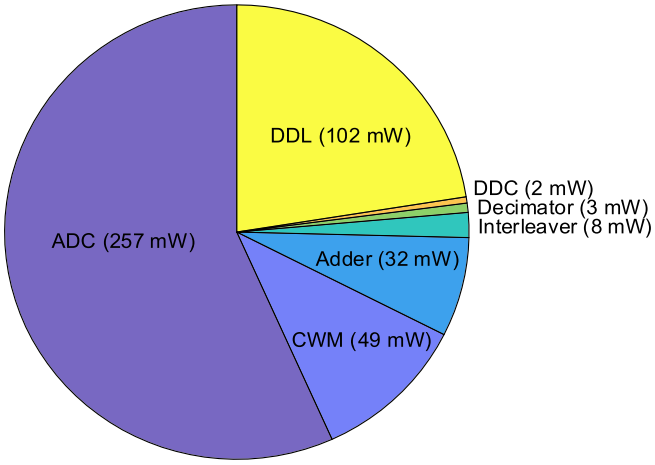


Fig. 25. Power break down of the true-time-delay digital beamforming including 16 bandpass delta–sigma modulators.

D. Interference Test

To test the performance in the presence of an in-band interference, a 0-dBm, 5-MBd QAM signal is applied to the main lobe and a 12-dBm, 1.01-GHz sine wave interference is applied to a null (Fig. 24). Although the in-band interference power is 12 dB higher than the desired signal, it is filtered out by the spatial filter of the array. As a result, the beamformer achieves an EVM better than -20 dB for QAM-16 and QAM-64, and no error symbols are found amongst the 8000 symbols.

E. Power Breakdown and Performance Scaling

Fig. 25 shows the power consumption breakdown of the prototype DBF. The 16 ADCs consume more than half of the total power (257 mW). The second most power-hungry block is the DDL block, which consumes 102 mW.

The power consumption of the CWM, DDC, and interleavers increases linearly with array size. The total power consumption of the DDLs is proportional to the square of the array size. For example, if we double the array size, the DDL power consumption quadruples. This is because both the number of DDLs and also the number of taps in each DDL increase with array size.[4] The power consumption of the adders and decimators increases because the number of inputs to the adder and the bitwidth of the input to the decimator increases. However, [16] shows that the total ADC power consumption remains the same for the same target EVM and the same modulation scheme. This is because the performance of each individual ADC can be relaxed as the array size increases.

Assuming a constant Schreier figure of merit (FoM) the ADC power consumption increases linearly with system bandwidth. As the power consumption of the digital blocks is proportional to clock frequency, the digital power consumption varies depending on the over sampling ratio (OSR) of the ADC. For example, for a constant OSR, doubling the clock rate doubles the bandwidth and also leads to a doubling of the power consumption of the DDC, CWM, and interleavers. In this scenario, the DDL power consumption quadruples because the number of DDL taps doubles due to the higher time-delay resolution. In a second scenario, if the OSR is halved to double bandwidth while maintaining the same clock frequency, then the power consumption of the DDL, CWM, DDC, and the interleavers remains the same. However, the second scenario (higher bandwidth with the same clock frequency) might not be practical because it may lead to a higher modulator order.

Increasing the number of beams increases digital power consumption but does not increase the ADC power consumption. The power consumption of the DDL, CWM, adder, and decimators increases linearly with the number of beams. However, the power consumption of ADCs, interleavers, and DDCs remains the same. The sharing of these blocks in processing multiple beams is a big advantage of digital beamforming.

The digital architecture is amenable to technology scaling. From [19], we expect that the digital power consumption reduces by 50% and 77% for 32- and 22-nm CMOS, respectively.

F. Performance Summary and Comparison

Table I summarizes the performance of our design and compares it with other state-of-the-art DBFs. This paper differs from the other two works in terms of delay implementation. This paper is the first true-time-delay digital beamforming IC, while the others are conventional phased arrays. The true-time-delay DBF in this paper has 16 elements, four independent simultaneous beams, a 100-MHz BW, 60 dB of array SNDR. It achieves baseband true-time-delay, which ranges from 0 to 7500 ps. The true-time-delay beamformer achieves no observable beam squinting error for a 1° measurement step size. In contrast, the beam squinting error fo phased arrays in [16] can be as large as 18° when steered at ±90°. Due to the high resolution (i.e., 10-bit) CWM, the difference between normalized measured beam patterns and normalized simulated beam patterns is less than 1 dB within the 3-dB beamwidth. The bandpass modulator consumes 16 mW, and the true-time-delay DBF consumes 196 mW. The total power consumption including the 16 ADCs and the DBF is 453 mW.

[4]Note that the maximum propagation delay in (10) is proportional to the array size.

TABLE I
PERFORMANCE SUMMARY AND COMPARISON

	This Work	[15]	[14]
Delay Implementation	True-Time-Delay	Phase-Shifting	Phase-Shifting
# of Elements	16	16	8
# of Beams	4	4	2
Bandwidth [MHz]	100	100	20
Array SNDR [dB]	60	59	63
Time Delay Range [ps]	0 - 7500	-	-
Beam Squinting Error [°]	< 1(a)	< 18(b)	< 16(b)
Phase-shifter Resolution [bit]	10	6	10
ADC Power [mW]	16	15	13
DBF Power [mW]	196	68	19
Total Power [mW]	453	312	124
Active Area [mm^2]	0.29	0.22	0.28
Technology	40 nm CMOS	40 nm CMOS	65 nm CMOS

(a) Measured for a -90º steered angle.
(b) Theoretical limitation for ±90º steered angles.

VI. CONCLUSION

This paper presents the first true-time-delay digital beamforming IC. The prototype beamformer has 16 elements, a 1-GHz carrier frequency, and a 100-MHz bandwidth. It achieves beam squinting errors smaller than 1° for various steered angles. Measured beam patterns, including adaptive beamforming, are almost identical to simulated beam patterns.

The CTBPDSMs in this paper enable IL-BSP which is high power and area efficient. The high-speed sampling of delta–sigma modulators is ideal for high-resolution digital true-time-delay. Furthermore, we introduce a constant output feedback DAC architecture, which improves the modulator's SFDR by 7 dB.

ACKNOWLEDGMENT

The authors would like to thank T. Olsson, K. Bunch, B. Epstein, and W. Chappell of Defense Advanced Research Projects Agency (DARPA) for their advice and support. They would like to thank J. Flynn at UCLA for his helpful comments and Linda Gong for proof reading. They would also like to thank Berkeley Design Automation for providing simulation software and Analog Devices for providing DDS devices.

REFERENCES

[1] R. Rotman, M. Tur, and L. Yaron, "True time delay in phased arrays," *Proc. IEEE*, vol. 104, no. 3, pp. 504–518, Mar. 2016.
[2] H. Hashemi, T. Chu, and J. Roderick, "Integrated true-time-delay-based ultra-wideband array processing," *IEEE Commun. Mag.*, vol. 46, no. no. 9, pp. 162–172, Sep. 2008.
[3] A. Gupta and R. K. Jha, "A survey of 5G network: Architecture and emerging technologies," *IEEE Access*, vol. 3, pp. 1206–1232, 2015.

[4] I. Mondal and N. Krishnapura, "A 2-GHz bandwidth, 0.25–1.7 ns true-time-delay element using a variable-order all-pass filter architecture in 0.13 μm CMOS," *IEEE J. Solid-State Circuits*, vol. 52, no. 8, pp. 2180–2193, Aug. 2017.

[5] S. K. Garakoui, E. A. M. Klumperink, B. Nauta, and F. E. van Vliet, "Compact cascadable gm-C all-pass true time delay cell with reduced delay variation over frequency," *IEEE J. Solid-State Circuits*, vol. 50, no. 3, pp. 693–703, Mar. 2015.

[6] T.-S. Chu and H. Hashemi, "True-time-delay-based multi-beam arrays," *IEEE Trans. Microw. Theory Techn.*, vol. 61, no. 8, pp. 3072–3082, Aug. 2013.

[7] S. H. Talisa, K. W. O'Haver, T. M. Comberiate, M. D. Sharp, and O. F. Somerlock, "Benefits of digital phased array radars," *Proc. IEEE*, vol. 104, no. 3, pp. 530–543, Mar. 2016.

[8] S. Jang, R. Lu, J. Jeong, and M. P. Flynn, "A true time delay 16-element 4-beam digital beamformer," in *Proc. IEEE Radio Freq. Integr. Circuits Symp.*, Philadelphia, PA, USA, Jun. 2018, pp. 12–15.

[9] K. Khalaf *et al.*, "A 60-GHz 8-way phased-array front-end with T/R switching and calibration-free beamsteering in 28-nm CMOS," *IEEE J. Solid-State Circuits*, vol. 53, no. 7, pp. 2001–2011, Jul. 2018.

[10] B. Sadhu *et al.*, "A 28-GHz 32-element TRX phased-array IC with concurrent dual-polarized operation and orthogonal phase and gain control for 5G communications," *IEEE J. Solid-State Circuits*, vol. 52, no. 12, pp. 3373–3391, Dec. 2017.

[11] S. K. Garakoui, E. A. Klumperink, B. Nauta, and F. E. V. Vilet, "Phased-array antenna beam squinting related to frequency dependency of delay circuits," in *Proc. Eur. Radar Conf. (EuRAD)*, Manchester, U.K., Oct. 2011, pp. 416–419.

[12] D. C. M. Horvat, J. S. Bird, and M. M. Goulding, "True time-delay bandpass beamforming," *IEEE J. Ocean. Eng.*, vol. 17, no. 2, pp. 185–192, Apr. 1992.

[13] F. W. Vook, A. Ghosh, and T. A. Thomas, "MIMO and beamforming solutions for 5G technology," in *IEEE MTT-S Int. Microw. Symp. Dig.*, Tampa, FL, USA, Jun. 2014, pp. 1–4.

[14] P. W. Wong and R. M. Gray, "FIR filters with sigma-delta modulation encoding," *IEEE Trans. Acoust., Speech, Signal Process.*, vol. 38, no. 6, pp. 979–990, Jun. 1990.

[15] J. Jeong, N. Collins, and M. P. Flynn, "A 260 MHz IF sampling bit-stream processing digital beamformer with an integrated array of continuous-time band-pass $\Delta\Sigma$ modulators," *IEEE J. Solid-State Circuits*, vol. 51, no. 5, pp. 1168–1176, May 2016.

[16] S. Jang, J. Jeong, R. Lu, and M. P. Flynn, "A 16-element 4-beam 1 GHz IF 100 MHz bandwidth interleaved bit stream digital beamformer in 40 nm CMOS," *IEEE J. Solid-State Circuits*, vol. 53, no. 5, pp. 1302–1312, May 2018.

[17] H. Chae, J. Jeong, G. Manganaro, and M. P. Flynn, "A 12 mW low-power continuous-time bandpass $\Delta\Sigma$ modulator with 58 dB SNDR and 24 MHz bandwidth at 200 MHz IF," *IEEE J. Solid-State Circuits*, vol. 49, no. 2, pp. 405–415, Feb. 2014.

[18] R. J. V. D. Plassche, "Dynamic element matching for high-accuracy monolithic D/A converters," *IEEE J. Solid-State Circuits*, vol. SSC-11, no. 6, pp. 795–800, Dec. 1976.

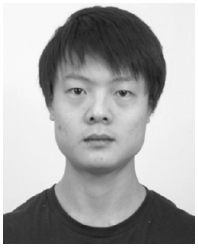
[19] A. Stillmaker, Z. Xiao, and B. Baas, "Toward more accurate scaling estimates of CMOS circuits from 180 nm to 22 nm," Dept. Elect. Comput. Eng., Univ. California, Davis, CA, USA, Tech. Rep. ECE-VCL-2011-4,

[20] R. H. Walden, "Analog-to-digital converter survey and analysis," *IEEE J. Sel. Areas Commun.*, vol. 17, no. 4, pp. 539–550, Apr. 1999.

Sunmin Jang (S'14) was born in Seoul, South Korea, in 1987. He received the B.S. degree in electrical engineering from Seoul National University, Seoul, in 2013, the M.S. degree in electrical engineering from the University of Michigan, Ann Arbor, MI, USA, in 2015, where he is currently pursuing the Ph.D. degree, with a focus on digital beamformers.

In 2018, he joined Apple Inc., Sunnyvale, CA, USA.

Mr. Jang received the Jeongsong Scholarship in 2013 and the Samsung Scholarship in 2015.



Rundao Lu (M'17) received the B.E. degree in electronic science and technology from Xi'an Jiaotong University, Xi'an, China, in 2013, and the M.E. degree in integrated circuit engineering from Shanghai Jiao Tong University, Shanghai, China, in 2016. He is currently pursuing the Ph.D. degree with the University of Michigan, Ann Arbor, MI, USA.

His research interests include RF and mixed-signal IC design.

Jaehun Jeong (M'11) received the B.S. degree in electrical engineering from Seoul National University, Seoul, South Korea, in 2006, and the M.S. and Ph.D. degrees in electrical engineering from the University of Michigan, Ann Arbor, MI, USA, in 2011 and 2015, respectively.

In 2015, he joined Broadcom Corporation, Irvine, CA, USA.

Dr. Jeong received the Scholarship from the Korea Foundation for Advanced Studies (KFAS) in 2009.

Michael P. Flynn (M'95–SM'98–F'15) received the Ph.D. degree from Carnegie Mellon University, Pittsburgh, PA, USA, in 1995.

From 1988 to 1991, he was with the National Microelectronics Research Centre, Cork, Ireland. From 1993 to 1995, he was with National Semiconductor, Santa Clara, CA, USA. From 1995 to 1997, he was a Technical Staff Member with Texas Instruments at Dallas, Dallas, TX, USA. From 1997 to 2001, he was with Parthus Technologies, Cork. In 2001, he joined the University of Michigan, Ann Arbor, MI, USA, where he is currently a Professor. His technical interests are in RF circuits, data conversion, serial transceivers, and biomedical systems.

Dr. Flynn is a 2008 Guggenheim Fellow. He was a recipient of the 2016 University of Michigan Faculty Achievement Award, the 2011 Education Excellence Award, the 2010 College of Engineering Ted Kennedy Family Team Excellence Award from the College from Engineering at the University of Michigan, the 2005–2006 Outstanding Achievement Award from the Department of Electrical Engineering and Computer Science at the University of Michigan, the NSF Early Career Award in 2004, and the 1992–1993 IEEE Solid-State Circuits Pre-Doctoral Fellowship. He was an Editor-in-Chief of the IEEE JOURNAL OF SOLID STATE CIRCUITS from 2013 to 2016. He is a former Distinguished Lecturer of the IEEE SOLID-STATE CIRCUITS SOCIETY. He served as an Associate Editor for the IEEE JOURNAL OF SOLID STATE CIRCUITS (JSSC) and the IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS. He serves on the Technical Program Committees for the International Solid State Circuits Conference (ISSCC) and the European Solid State Circuits Conference (ESSCIRC). He formerly served on the Technical Program Committees the Asian Solid-State Circuits Conference (ASSCC) and the Symposium on VLSI Circuits.