A 9b 2GS/s 45mW 2X-Interleaved ADC

Jorge Pernillo and Michael P. Flynn
Dept. of EECS, University of Michigan, Ann Arbor MI 48109, USA

***Abstract*— A 9b 2GS/s ADC architecture interleaves a pair of two-stage pipeline ADCs to achieve high performance with a shared low-gain op-amp and a shared low-accuracy 2nd stage sub-ADC. This technique reduces area and eliminates the need to correct for gain and offset mismatch between channels. The ADC achieves a measured ENOB of 7.07b for a 1GHz signal input sampled at 2GS/s and consumes 45mW from a 1.0V supply, yielding an FOM of 167fJ/conversion-step.**

I. INTRODUCTION

Multi-Giga-sample per second (GS/s+), moderate resolution ADCs enable direct sampling receivers for cable modems [1] and are key components of software radios and 60GHz wireless links [2]. Time interleaving is extensively employed to achieve GS/s+ moderate resolution, conversion. Recent architectures leverage the power efficiency of SAR ADCs either through extensive parallelization [3] or with hierarchical structures [1]. However, these approaches require large area, require gain and offset calibration, and consume hundreds of milli-Watts of power. Pipelining reduces the number of T/Hs [4], because pipelining increases the throughput of each individual, interleaved ADC. However, the high op-amp gain required for moderate-resolution pipeline ADCs is challenging in 45nm CMOS and below, as the transistor self-gain is ~10. In [5], both high gain and high bandwidth are achieved in an MDAC op-amp implemented in 40nm CMOS. However, [5] relies on thick-oxide devices and gain boosting along with a 2.5V supply to increase the op-amp gain and the signal swing.

We introduce a new, twice-interleaved ADC architecture that leverages the single-channel two-stage redundant flash-based pipeline ADC architecture proposed in [6]. The new architecture incorporates a combination of op-amp and sub-ADC sharing to double the bandwidth, reduce power and area, and eliminate the need to correct errors due to gain and offset mismatch between channels.

This combination of an interleaved first stage and shared second stage is very attractive for a 45nm SOI CMOS process. For moderate resolution, the speed of the 1st stage MDAC is limited by the op-amp's self-parasitics which dominate the output load capacitance. On the other hand, the speed of the 2nd stage flash sub-ADC tracks the speed (i.e. f_T) of the technology which improves with CMOS scaling. In our design, a single 2nd stage flash sub-ADC is shared between two time-interleaved 1st stage MDACs to enable optimal 2nd stage performance and at the same time reduce area. Furthermore, sharing a single 2nd stage sub-ADC eliminates channel mismatch due to gain and offsets that arise when there are separate 2nd stage sub-ADCs for each interleaved channel.

A simple clock-skew correction circuit reduces timing mismatch between the two interleaved channels. The 9bit, 2GS/s 45nm SOI-CMOS prototype achieves a peak ENOB of 7.6b, and no missing codes at 9b resolution. It consumes only 45mW at 2GS/s from a 1V supply. This 2X-interleaved 9bit ADC occupies only 0.22mm^2 and achieves a figure of merit (FOM) of 167fJ/conversion-step at Nyquist.

II. ARCHITECTURE AND SUB-BLOCKS

A. Overview

Fig. 1 shows a block diagram of the proposed 2X interleaved architecture. Two interleaved boot-strapped switches sample the differential input signal (single-ended shown) on opposite phases of a 1GHz clock. The sampled signals are subsequently processed by two 4b MDACs that are pipelined with a single, shared 2GS/s 6b flash ADC sub-converter. The two 4b MDACs also share an op-amp for power efficiency and further area reduction.

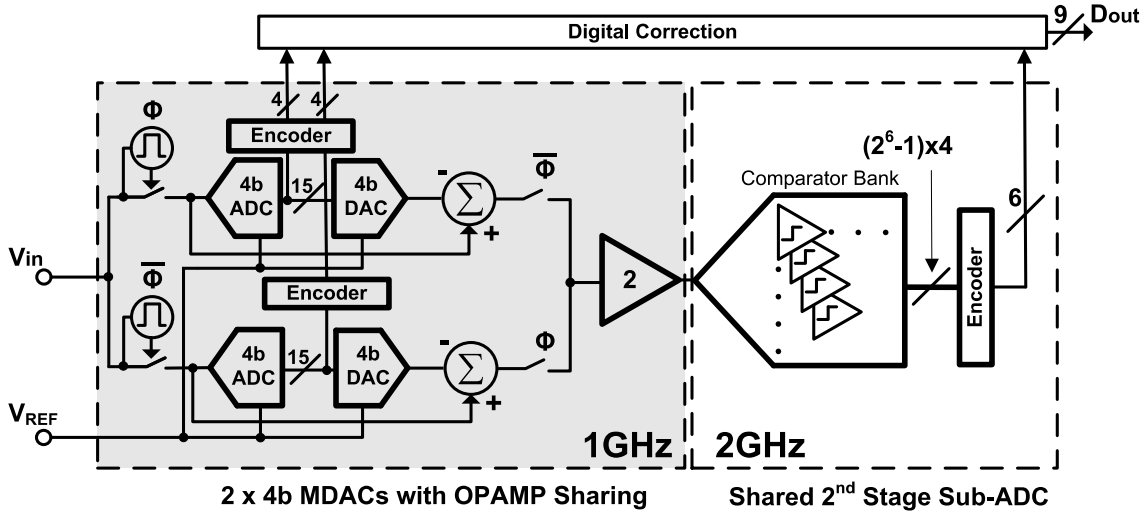

Fig. 1 Simplified single-ended representation of ADC architecture

The time-interleaved 4b MDACs use a high feedback factor of 1/3 to relax the op-amp gain and bandwidth requirements. The high feedback factor scheme reduces the required gain and bandwidth by 5.7X, allowing a single-stage op-amp design [7]. The shared 2nd stage 6b flash sub-ADC employs comparator redundancy and reassignment to correct for DNL errors [8]. Furthermore, deliberate and random mismatch set the desired comparator trip-points and eliminates the need for a high-precision, low-impedance resistor reference ladder [9]. A 1b over-range in the 2nd stage reduces the accuracy required for the 1st stage comparators.

B. 2X-Interleaved 1st stage 4b MDACs

Fig. 2 shows a simplified schematic of the two time-interleaved 1st stage MDACs and their sub-ADCs. Each channel is similar in architecture to [6]. For each channel, an array of thermometer-encoded unit capacitors C_U serves as the input sampling capacitance for the 4b MDAC. A second array of capacitors C_S serves as the input sampling capacitors for the comparators that make up the 4b flash sub-ADC. A 15-tap resistor reference ladder sets the 1st stage comparator thresholds. For power efficiency and area reduction, the 2X-interleaved architecture shares an op-amp between the two MDACs. Op-amp sharing also eliminates channel gain and offset mismatch that arise when there are separate op-amps for each interleaved channel. Therefore calibration to mitigate gain and offset mismatch between channels is not required. The front-end switch in each channel is bootstrapped for improved linearity. Each channel is clocked on opposite phases of a 1GHz input clock (i.e. 1GHz, 0° and 1GHz, 180° in Fig. 2) and interleaving doubles the throughput to 2GS/s.

The timing waveforms for one channel (i.e. MDAC[0] in Fig. 2) are shown in Fig. 3. The clock waveforms for the two channels are similar but are phase shifted 180°. When V_{clk} and V_{clk1} are both high, the sampling capacitors in the sub-ADC and MDAC track the input signal. The signal is then sampled on the falling edge of V_{clk}. A short delay (τ_{delay} in Fig. 3) between the falling edges of V_{clk} and V_{clk1} reduces the effects of timing mismatch between the 1st stage MDAC and its sub-ADC.

On the rising edge of V_{clk2} the flash sub-ADC reference voltages are connected to the comparator sampling capacitors, C_S. This causes the difference between the comparator reference voltages and sampled input signal to appear at the comparator inputs. Comparator decisions are made on the falling edge of V_{comp1}. A short delay between the rising edge of V_{clk2} and the falling edge of V_{comp1} allows adequate settling before the sub-ADC comparison. The sub-ADC comparator outputs then drive the MDAC reference switches to produce the residue V_{RES} at the MDAC output.

The time between the falling edge of V_{clk1} and the 1st stage sub-ADC decision is used to reset the MDAC output during pulse V_{Reset} as shown in Fig. 3. This reduces cross-talk between the two interleaved MDACs. The switched capacitor CMFB also operates during this period. The reset also reduces SOI related memory effects in the 2nd stage sub-ADC.

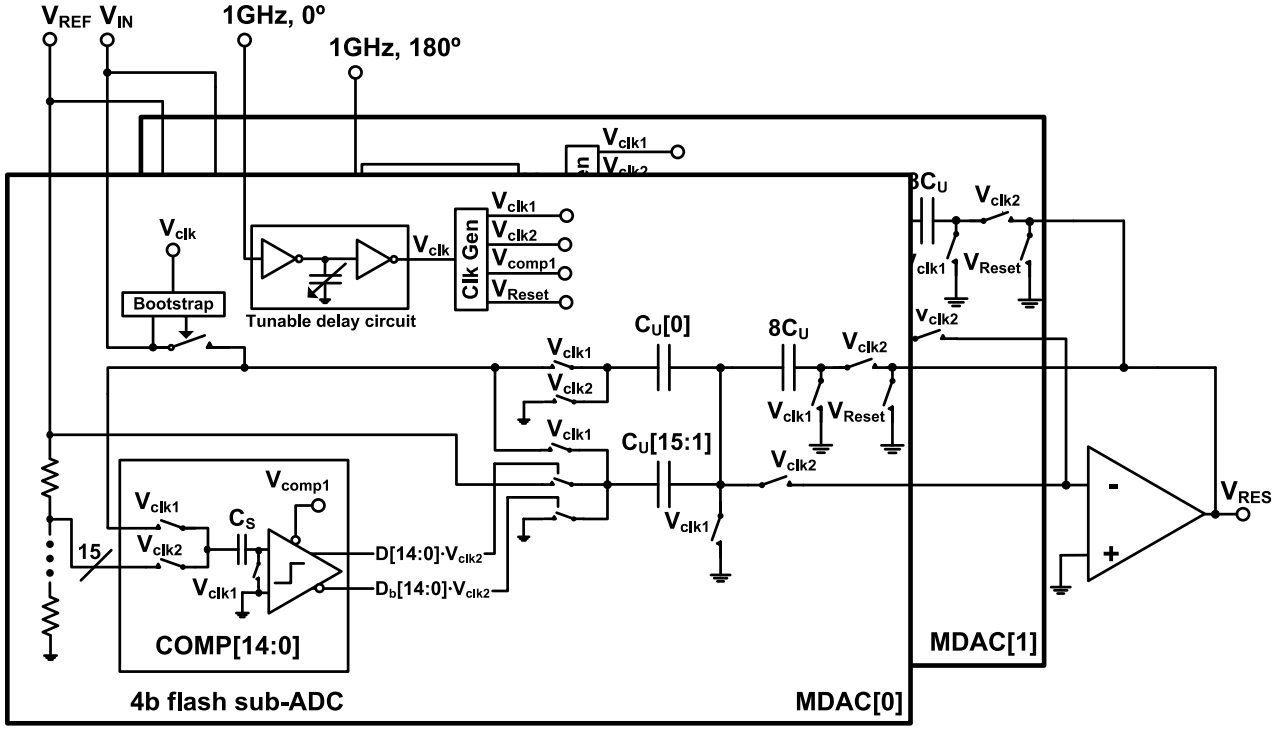

Fig. 2 Simplified single-ended representation of two time interleaved 4-bit MDACs with op-amp sharing.

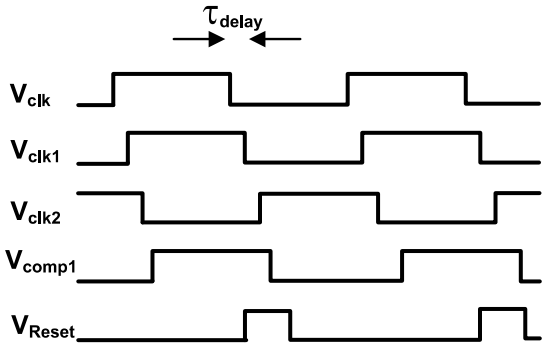

Fig. 3 Timing waveforms for one of two time-interleaved 1st stage 4-bit MDACs.

The shared op-amp is implemented as an NMOS-input, telescopic, triple-cascode amplifier. The op-amp has a minimum gain of 42dB, a unity gain frequency of 7.5GHz and supports a pk-pk output swing of 150mV with only a1V supply [6].

Simple digital trimming of a tunable delay circuit in the input clock path of each MDAC (i.e. 1GHz, 0° and 1GHz, 180° in Fig. 2) correct for timing mismatch between channels. 5b control and a 200fs delay increment provides sufficient granularity within a 1.5ps window to limit SNR degradation due to sampling mismatch to less than 3dB for a 1GHz input signal. Furthermore, the 180° phase shift between channels ensures that only a single channel loads the ADC input during tracking.

III. Shared 2ND Stage Sub-ADC

Fig. 4 shows a simplified single-ended block diagram of the shared 2nd stage 6b flash sub-ADC and its timing waveforms. The sub-ADC is similar to that in [6]. The residues from the 2X-interleaved 1st stage MDACs are digitized in alternating order on the falling edge of V_{COMP2} as shown in Fig. 4. A single 2GS/s 2nd stage is simpler and more area efficient than two separate 2nd stages operating at 1GS/s. Furthermore, sharing a single 2nd stage sub-ADC eliminates channel mismatch due to gain and offsets that arise when there are separate 2nd stage sub-ADCs for each interleaved channel. Therefore, offset calibration schemes to mitigate this effect are not required. A 1σ comparator random offset of 17 ADC-LSBs and a comparator redundancy of four-per-code provide sufficient spread so that only twelve deliberate offsets are implemented in the 6 bit sub-ADC [6]. A startup calibration routine finds the comparators closest to the desired trip-points and an encoder block comprised of full adders resolves the comparator outputs to the 6-bit sub-ADC output code.

IV. Measurement Results

The prototype, fabricated in a 45nm SOI-CMOS process, occupies a core area of 0.22mm^2. A die micrograph is shown in Fig. 5. The prototype ADC has a differential input signal range of 900mVpp and input capacitance of 500fF.

The measured DNL and INL for each channel is within -0.85/+1.3LSB and -1.75/+1.58LSB, respectively, and is shown in Fig. 6. With interleaving, the overall ADC DNL and INL improve to -0.69/+1.11 and -1.58/+1.37 respectively.

Fig. 7 shows the output spectrum for a 1000.98MHz input signal, sampled at 2GS/s. The output data is decimated by 9X for reliable transmission off-chip. Fig. 8 shows the measured SNDR and SFDR versus input frequency at 2GS/s. Simple calibration corrects for MSB-dependent DC offsets in the MDAC residue due to insufficient decoupling on the reference lines.

The prototype ADC achieves an ENOB and SFDR of 7.6 bits and 66dB, respectively, at low frequency and 7.07 bits and 56 dB at Nyquist. The ADC consumes a total of 45mW from a 1V/1V analog/digital supply and achieves an FOM of 167fJ/conversion-step. Table I compares recently published ADCs with Fs > 1GS/s and Nyquist ENOB > 7b. The prototype 9b 2GS/s ADC architecture achieves one of the best energy efficiencies in its class with far less interleaving and simpler calibration than other designs.

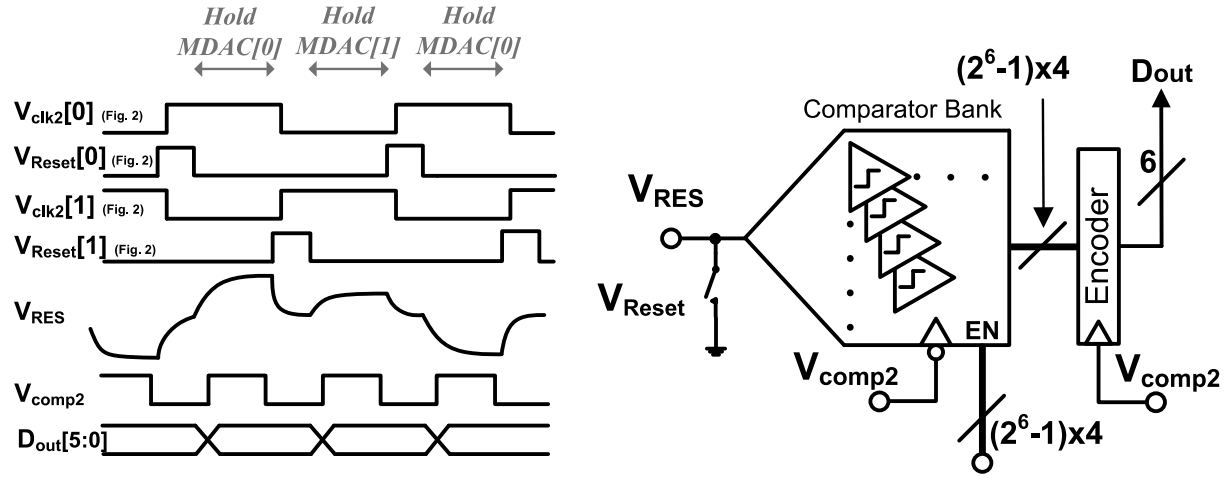

Fig. 4 Simplified single-ended representation and timing waveforms for the shared 2nd stage 6b sub-ADC with redundancy of four comparators per code.

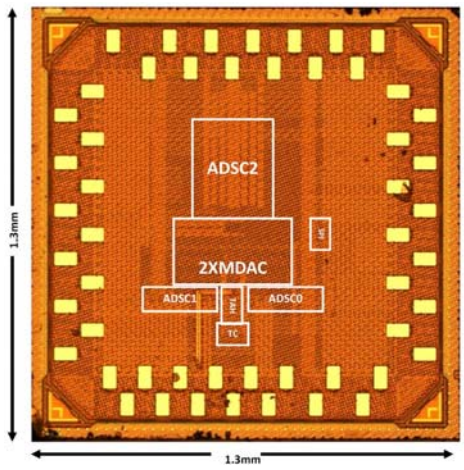

Fig. 5 Die micrograph of 45nm SOI-CMOS ADC.

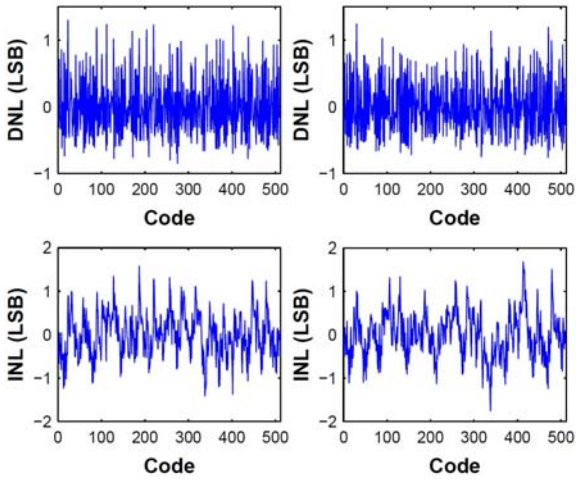

Fig. 6 DNL and INL of channel 1 (right) and channel 2 (left).

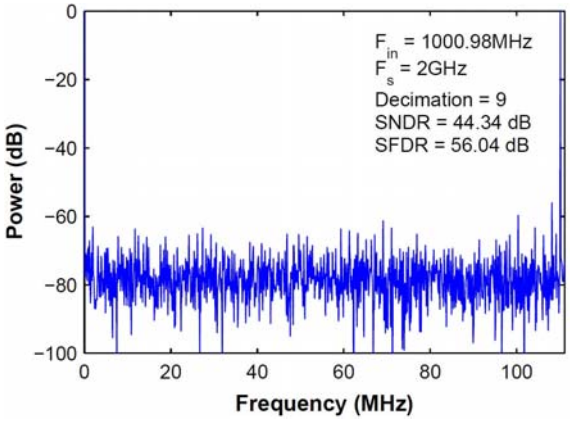

Fig. 7 Output spectrums for a 1000.98MHz input and 9X decimation.

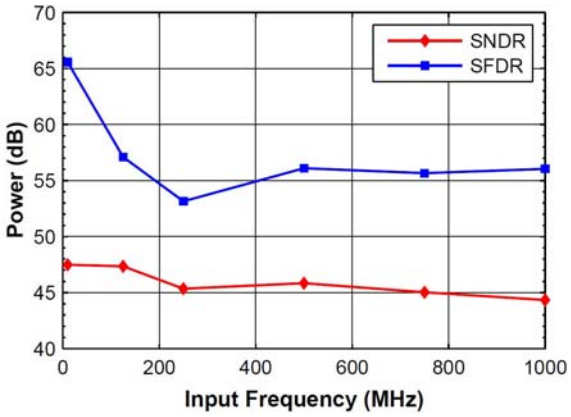

Fig. 8 Measured SNDR & SFDR vs. Fin (Fs = 2.0GS/s).

Table I
ADC Performance Comparison
(Fs > 1GS/s, Nyquist ENOB > 7b)

Reference	[3]	[5]	[1]	[10]	This work
Technology	0.13um CMOS	40nm CMOS	65nm CMOS	65nm CMOS	45nm SOI-CMOS
Fs (GS/s)	1.35	3	2.6	2.8	2
Channels	16	2	64	24	2
PWR (mW)	175	500	480	45	45
Area (mm^2)	1.6	0.4	5.1	0.18	0.22
Nyquist ENOB	7.4	7.85	7.76	7.71	7.07
FOM (fJ/conv-step)	768	722	852	76	167

ACKNOWLEDGMENT

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