Global Signaling over Lossy Transmission Lines

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Abstract

We describe an interconnect scheme based on lossy transmission lines, compare this scheme with traditional bus based links, and present performance data. Unlike some other schemes there is no requirement for up-conversion, equalization, or special metal processing. In preliminary work, we have measured data rates of 14 Gbps (limited by test equipment) over a 7.2 mm interconnection, implemented in 0.18 µm CMOS. For active links signaling over a single serial link, is more power efficient than over traditional parallel buses, does not require repeaters and is less affected by noise and coupling.

Keywords: serial interconnection, global wiring, transmission line

1. Introduction

High-speed serial signaling over transmission lines is a robust, power-efficient alternative to global parallel buses with repeaters. The parallel bus is replaced with a single high speed differential link. We present and analyze a practical serial interconnect scheme for a 130 nm digital CMOS process and 0.18 µm CMOS. A 15 mm link achieves a bandwidth in excess of 40 Gbps, yet does not require repeaters or buffers. We show that the energy per bit is less than that of an optimally designed parallel bus. In contrast to other serial schemes, this scheme does not incorporate up-conversion to a high frequency carrier, or require special metal processing. Furthermore, very wide lines are not required. We present a termination scheme that minimizes dispersion, making very large bandwidths feasible even with narrow lossy on-chip transmission lines. In addition, differential signaling is largely immune to the problems of skew, and crosstalk that afflict long, high speed, parallel buses.

Global signaling is responsible for an ever increasing portion of the total power consumption. On 180 nm microprocessors (e.g., McKinley) global repeaters consume 3% of the total power dissipation, while repeater power consumption is predicted to increase towards 25-30 % by the 65 nm technology node [2]. In addition there are reliability problems due to timing errors, skew, and crosstalk. Noise, coupling, and inductive effects have become significant for both intermediate and global routing. Buses are taking too much area, yet interconnect is reverse scaling [1] while the required communication bandwidth on an IC is growing exponentially. Even today, the energy required to transfer 32 bits over a distance of 15 mm in a microprocessor is 20 times larger than the energy consumed by a 32 bit arithmetic operation [3].

Repeaters are commonly used to improve long distance signaling by breaking up long lines into shorter sections. Although this technique is very effective, the optimum number of repeaters can be large. The repeaters have an adverse effect on power consumption and chip area, and also generate significant supply noise. The performance of repeaters is sensitive to edge rates. Furthermore, repeaters are not always optimally located, for example, it may not be possible to optimally place repeaters when routing over a critical logic block.

As data rates increase, digital designers see inductance as a one of the major impediments to performance. Inductance affects delay [4], yet is difficult to estimate from layout [5], and the much larger netlist makes simulation expensive. Inductance can cause ringing and overshoot. Inductive coupling [4] can be a significant problem, especially since this coupling has a longer range than capacitive coupling [5].

2. Serial Communication on Chip

Over the last decade, serial links have all but replaced parallel buses for high speed chip-to-chip and backplane communication. Serial signaling removes the requirement to match multiple bus lines. Properly designed PCB traces form low loss transmission lines, and offer propagation speeds close to the speed of light. Serial links based on transmission lines allow higher data rates, yet generate less noise and are less prone to interference than parallel buses. Off the IC, CMOS based serial transceivers communicate across feet of PCB interconnect at rates of more than 3 Gbps (e.g. XAUI, Infiniband, Fiberchannel).

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Serial links can be combined in parallel to achieve even higher data rates.

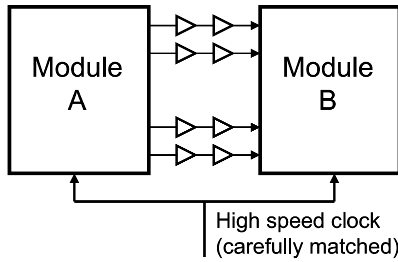

Figure 1. Conventional parallel bus with repeaters.

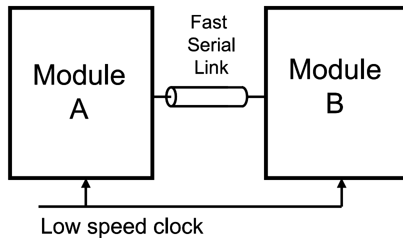

Figure 2. Serial link with plesiochronous clocking.

Fig. 1 shows a conventional bus link between two modules on an IC. Care is taken to match clock delays to both blocks. A parallel bus can include repeaters to improve data rate, however the time of flight must be less that a clock period. We now consider two possible clocking scenarios that can be used for serial links between modules on an IC.

In a *mesochronous* [7] link [8] (Fig. 2), the same reference clock is routed to the transmitter and receiver modules, but without consideration of delay. (To save power, the reference clock need only run at a fraction of the clock speed of the modules.) Since the receiver's internal clock and the transmitter clock are derived from the same reference clock, the receiver needs only to determine the phase, not the frequency, of the received signal. Based on the phase information, the receiver optimally samples the arriving signal and transfers the sample data to a parallel format. Depending on the system clock frequency, for a long link (e.g., 15 mm), the time of flight can be comparable to (or longer than) the system clock period. There is no requirement to match or control clock and signal delays.

Since the system clock runs at a fraction of the serial data rate, the transmit block must derive the high speed clocking for data transmission from the system clock. This can be accomplished using a phase locked loop (PLL) or a delay locked loop (DLL) [9]. There are no repeaters or buffers, although equalization can be used to extend the effective bandwidth of the link.

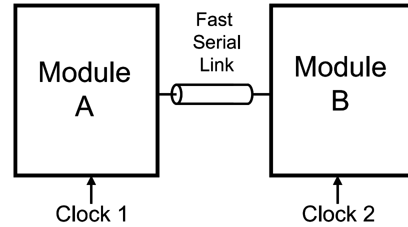

Figure 3. Serial link with mesochronous clocking.

A *plesiochronous* [7] configuration allows more flexibility in clocking, but this comes at the expense of increased complexity and power consumption. In this case (Fig. 3) the reference clocks to the transmit and receive ends are derived from different clock reference sources (e.g. separate crystals) and each may vary or drift independently from its nominal value. (For example, in backplane applications (e.g., Fiberchannel) reference frequency error is usually limited to 100 ppm.) The receiver must now track the phase and frequency of the received signal. This data in turn must be transferred to the local clock domain. Because a plesiochronous link can fail in the presence of long sequences of zeroes or ones, the transmitted data is scrambled (e.g. 8B-10B coding [10]). The extra flexibility of a plesiochronous link comes at the expense of a much more complex and power hungry receiver, as well as the coding overhead and power consumption associated with scrambling.

3. Lossy On-Chip Transmission Lines

3.1. Background: Transmission lines

On-chip transmission lines have application in both on chip serial signaling and in bus based signaling. However on-chip transmission lines formed with standard metal layers are very lossy, causing dispersion which greatly limits the effective bandwidth of on-chip serial links. Nevertheless, transmission lines offer the potential of close to speed of light communication. [11] Furthermore, since the return path is well defined, transmission lines have well controlled inductance and are less prone to coupling than RC lines.[1]

Some of the most successful demonstrations of on-chip serial signaling have involved additional process steps or frequency up-conversion. In [6], a 50 GHz bandwidth was achieved over 20 mm link implemented as

[1] The idea of increasing inductance to help signaling in over a lossy line is not a new one. The present situation is similar to in telephony in the 1880s, when engineers struggled with signaling on long telephone lines. Oliver Heaviside proposed that the addition of inductance would reduce distortion in long distance telephony.

a coplanar transmission line, formed with a very thick (5 μm) non-standard metal layer. The use of thick, wide metal helps to minimize resistive loss. In [11], 1 Gbps data is up-converted to 7.5 GHz carrier, in an approach inspired by RF communication techniques. Significant dispersion is avoided by utilizing only a narrow band at high frequency; however, this approach adds significant complexity to the link and utilizes a small fraction of the potential bandwidth. CDMA modulation is used for re-configurability, multiple access and increased bandwidth [12]. In [13] a measured data rate of 4 Gbps is achieved over a 2.5 mm transmission line, constructed with a pair of diagonally offset wires on different layers.

A transmission line is formed by a signal wire coupled to a ground line or ground plane. The coplanar (Fig. 4(a) and microstrip transmission line structures Fig. 4(b) are best suited to integrated circuit implementation.

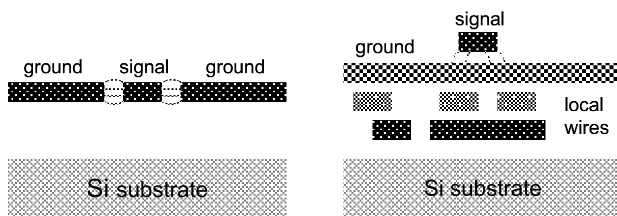

Figure 4. (a) Co-planar and (b) strip-line transmission lines.

Ideally, a transmission line should have well-defined ground to reduce EM coupling to the substrate and other lines and to reduce di/dt noise to clock and local wires. The coplanar structure incorporates ground and signal paths on the same metal layer. A microstrip incorporates a ground line below the signal line. Since this ground functions as a shield, the placement of local circuitry and routing on the lower layers is not restricted.

Since capacitance between the signal line and the ground sets the characteristic impedance, the characteristic impedance of a co-planar transmission line, can be altered by changing the spacing of wires [6]. An advantage of the coplanar configuration is that the characteristic impedance can be relatively high. However, a significant disadvantage of the structure is that local wiring can not be routed below the transmission line without interference since field lines extend down towards the substrate. Furthermore coplanar lines are also prone to substrate loss [14].

The interaction of the inductance and capacitance in a lossless transmission line allow wave propagation of a signal. The wave travels at the speed of light in the dielectric. The phase velocity is $1/\sqrt{\varepsilon\mu}$ and the ratio $\sqrt{L/C}$ is the characteristic impedance, Z_0, of the line. A transmission line is usually terminated with a resistance equal to the characteristic impedance to avoid reflection.

3.2. Dispersion and inter symbol interference

Practical on-chip transmission lines have significant series resistance, causing attenuation and dispersion. As an example, a 15 mm long, 10 μm wide line might have a series resistance on the order of 100 Ω. This significant series resistance has two detrimental effects. Since a pulse traveling down the line loses energy through resistive loss it becomes attenuated. A more serious problem is that the resistance leads to dispersion. The high frequency components of the signal travel more quickly than the low frequency content, since the low frequency content now becomes RC limited. This results in inter-symbol interference, where successive symbol (i.e. bits in the simplest case) may collide and interfere with each other, making detection difficult.[2]

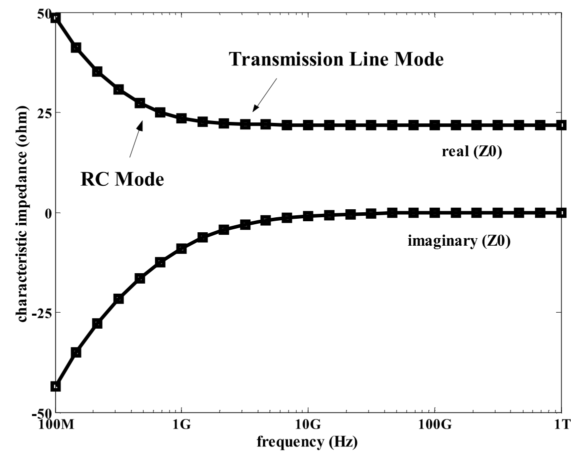

Figure 5. Characteristic impedance vs frequency for a lossy line.

Fig. 5 indicates the two regions of propagation of a lossy transmission line. The graph shows the real and imaginary components of the characteristic impedance. The real and imaginary impedance vary with frequency in the RC mode but remain constant and real for wave propagation. Transmission line effects dominate when the frequency is large enough so that the following condition is true [16].

$$R_{unit} << \omega L_{unit} \quad (1)$$

[2] Dispersion in PCB traces is mostly caused by the skin effect [15]. We can ignore the skin effect if the skin depth is greater that half the thickness or width of the conductor. Skin effect does not limit frequency dependant resistance of a thin film copper layer in a modern CMOS processes for frequencies below 100 GHz; Film thickness typically ranges from 0.30 μm to 0.55 μm, while the skin depth in copper is 0.208 μm at 100 GHz.

ω is the frequency in radians and R_{unit} and L_{unit} are the series resistance and the inductance of a unit length of interconnect, respectively. On the other hand, when the spectral content of the signal spans both regions, there can be inter symbol interference.

We now consider in more detail how a short pulse (i.e. dominated by high frequency components) travels down a lossy transmission, first considering an infinite line. The amplitude of the pulse decays exponentially as the pulse travels down the line with wave velocity equal to the speed of light in the dielectric. The amplitude at a distance l from the transmitter can be described with (2).

$$V(l) = V_S \cdot e^{-\alpha \cdot l}. \qquad (2)$$

Here, V_S is the transmit amplitude, and the attenuation constant α is determined by the resistive loss in the line and characteristic impedance Z_0.

$$\alpha \approx \frac{R_{line,unitlength}}{2 \cdot Z_O} \; (m^{-1}). \qquad (3)$$

We now consider the more practical and complicated situation of sending a step of amplitude V_S down a line of finite length l, terminated with a small capacitance. Usually, on-chip, digital lines are terminated with capacitance, since the inverter or flip-flop at the receive-end presents a capacitive load. We know from Fourier analysis that the step is comprised of a series of spectral components. The high frequency components decay exponentially as they travel along the lossy line. On the other hand, for low frequency components, the line appears as a distributed RC circuit, not a transmission line. Because the low and high frequency components propagate at different speeds, the step is distorted when at arrives the receive end.

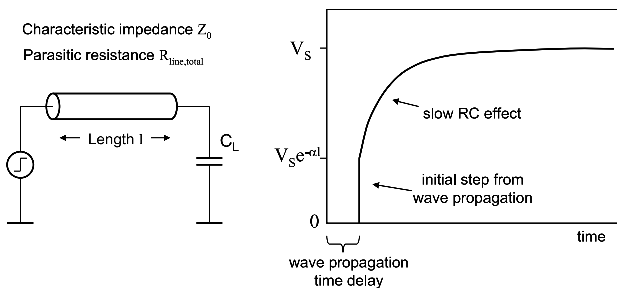

Figure 6. Step response for lossy line terminated in capacitance.

This response to the step is depicted in Fig. 6. An initial attenuated step of amplitude $V_S\, e^{-\alpha l}$, at the output is due to the high frequency components propagating down the transmission line at near the speed of light, and later the slower RC effect charges the entire line to the unit voltage. Because of the RC effect the voltage at the receive end may take a long time to reach the final value (i.e. V_S), there may be inter-symbol interference, limiting the maximum bit rate on the line.

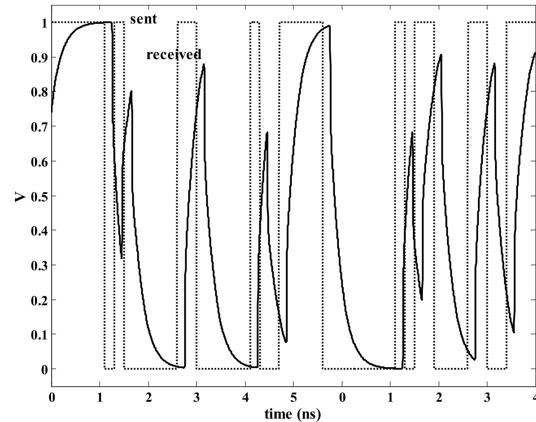

Figure 7. Response to data pattern for line terminated with capacitance showing significant ISI.

Fig. 7 shows the response to a series of pulses representing a data pattern that begins at time 0. In this example inter symbol interference (ISI) corrupts the duration and height of the received bits.

3.3. Termination Resistance

If we terminate the line appropriately, then we can achieve extremely large bandwidths and avoid inter-symbol interference. RF circuit designers terminate transmission lines with a resistance equal to the characteristic impedance of the line, (i.e. $R_L = Z_0$) to prevent some the received signal reflecting back into the line. Reflection is less important in digital signaling and since our lines are very lossy, the energy of any reflected signal is dissipated by resistive loss. We will see that the optimum termination for digital communication over a lossy transmission line is not necessarily equal to the characteristic impedance [17].

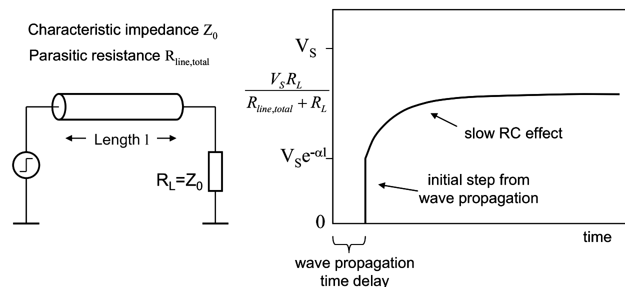

Figure 8. Step response for lossy line terminated in resistance.

We first considered the step response of a lossy line of length l terminated by a real resistance $R_L = Z_0$ (Fig. 8). As before, for a finite length, lossy transmission line, terminated with a real resistor, the high frequency components arrive at the receiver with amplitude of:

$$V_H = V_s \cdot e^{-\alpha \cdot l} . \tag{4}$$

The slower low frequency component charges up the line to a voltage determined by a voltage divider formed by the total parasitic series resistance of the line, $R_{line,total}$ and termination resistance R_L.

$$V_H = V_s \cdot \frac{R_L}{R_{line,total} + R_L} \tag{5}$$

As discussed earlier, we see a step component that propagates quickly down the line, followed by a slow RC component that approaches a final value given by (5).

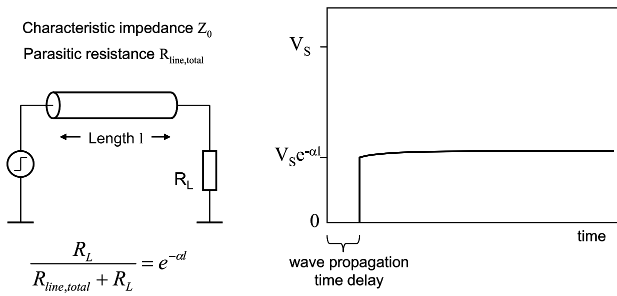

Figure 9. Step response for optimally terminated, lossy line.

If we choose an optimum value of R_L (Fig. 9), we can mask the effect of the slow component and minimize inter-symbol interference [13]. If we compare the resistor terminated example above, with the earlier capacitor terminated case, we note that the RC component is far less significant in the resistor terminated case. This is because the final voltage is closer to the amplitude of the initial high frequency component. This suggests that the optimum performance without any RC settling is achieved by matching the high frequency and low frequency (resistive divider) components. This is achieved by satisfying the following equality:

$$\frac{R_L}{R_{line,total} + R_L} = e^{-\alpha \cdot l} \quad . \tag{6}$$

This places some restrictions on line length however in principle, the transmission link and termination can be optimized for any link length.

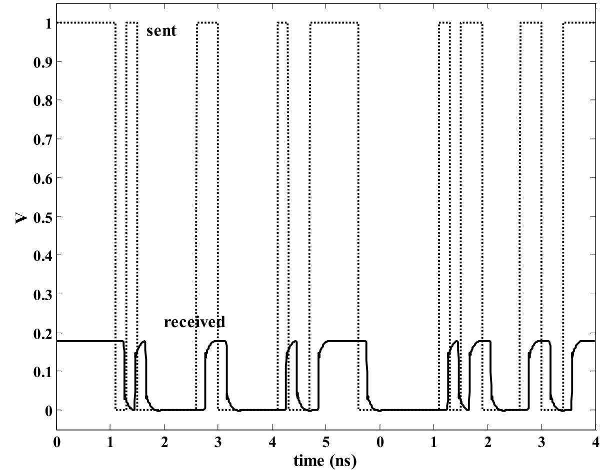

Figure 10. Response to data pattern for line terminated with optimum resistance.

Fig. 10 shows the response to the same digital pattern as in Fig. 7, but now the line is optimally terminated. The receive amplitude is reduced, to that of the high frequency components, sacrificing receive amplitude for bandwidth. The inter-symbol interference is greatly reduced and the received bits can easily be identified.

4. Case Studies

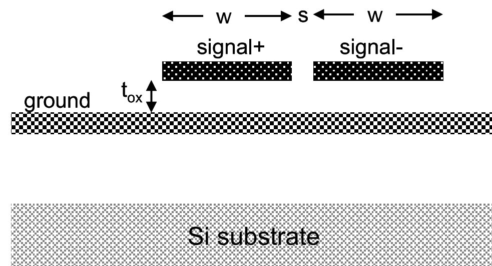

Figure 11. Differential strip line.

We now present measured data from a prototype 7.2 mm transmission line fabricated in 180 nm CMOS, and present simulated data from a 15 mm long line in a 130 nm CMOS process. We employ a differential microstrip structure, with two signal lines over a single ground (Fig. 11). Differential signaling gives increased immunity to noise and coupling, and simplifies the receiver. Higher metal layers are used for the signal and ground. Since the ground functions as a shield, the placement of local circuitry and routing on the lower layers is not restricted. We compare the transmission line with a 16 bit wide, parallel bus. To make the comparison meaningful we choose a transmission line width narrower than that of the parallel bus.

4.1. Prototype link in 0.18μm CMOS

A 7.2 mm differential lossy line is implemented as two 9 μm wide, 2.34 μm thick, M6 signal lines, separated by 1 μm, over a single ground (M2). EM simulation indicates a high frequency, characteristic impedance of 28.6 Ω. Applying (6), the optimal termination resistance for a 7.2 mm line is R_L = 40 Ω.

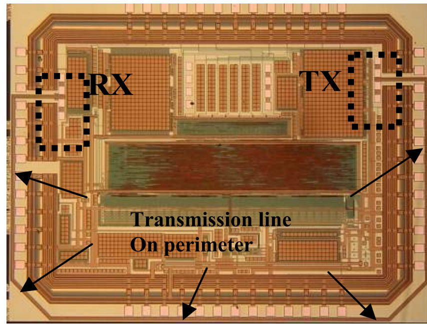

Figure 12. Die photo of prototype link in 0.18 μm CMOS.

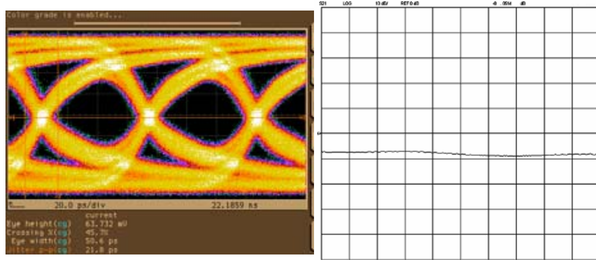

Figure 13. (a) Measured eye diagram at 14 Gbps, and (b) measured S21 from 30 kHz to 6 GHz.

Fig. 12 shows a die photo of a prototype transmission line implemented in a 180 nm CMOS IC. Fig. 13(a) shows the measured eye diagram for a 14 Gb/s 32 bit PRBS signal. Fig. 13(b) shows that the measured S21 (transmission) of the structure is constant to -8 dB within 2 dB, from 30 KHz to 6 GHz. Fig. 13(b) shows the measured eye diagram for a 14 Gb/s 32 bit PRBS signal. The flat transmission and the open eye indicate minimal dispersion and inter-symbol interference.

4.2. 130nm CMOS lossy transmission line

We now study a 15 mm transmission line in 130 nm CMOS that achieves 40 Gbs+. To make our analysis realistic, we design the transmission line to be significantly narrower than a 16 bit wide, 40 Gb/s parallel bus (i.e. <16 * (0.6 μm + 0.6 μm) = 18.6 μm). Higher metal layers, separated by 3.05 μm, on M8 and M4, are used to implement the signal and ground traces. Two 6 μm wide signal wires on M8 are separated by 1 μm. EM simulation indicates that the characteristic impedance of this structure at high frequency is 29.9 Ω.

A termination resistance, R_L is chosen according to (6). The copper metal series resistivity is 68.9 Ω/cm. The high frequency attenuation constant, α, extracted by the EM solver is 115.4 m^{-1}. Applying (6), the optimal termination resistance for a 15 mm line is R_L = 22.2 Ω.

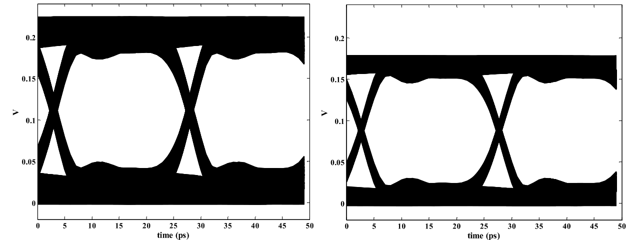

Figure 14. Eye diagram at 40 Gbps, (a) termination with Z_0 and (b) optimum termination.

To evaluate the performance of the serial link, a 192 segment model of the transmission line is simulated with Spectre. The response to a 1 Vp-p, 40 Gbps 2^{31}-1 pseudo random binary data sequence (PRBS) is simulated and its received signal is shown in the form of an eye diagram, for a line terminated with the characteristic impedance Z_0 (Fig. 14(a)), and a line terminated with the optimum R_L (Fig. 14(b)).

4.3. Power comparison with parallel bus

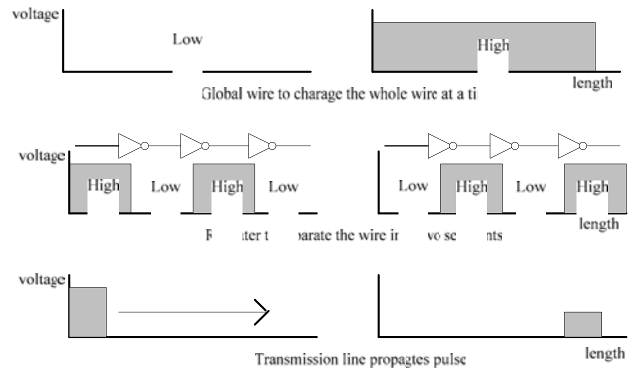

Figure 15. Data transmission over a long link (a) without repeaters (b) with repeaters and (c) transmission line scheme.

The energy advantage of a transmission line structure, for active data, can be seen by comparing signaling over a transmission line with signaling over traditional buses. Fig. 15 shows three examples of propagation. The simplest case is a bus line without repeaters. To signal a logic '1' the entire line is charged up to the 'high' voltage. Long bus lines are usually broken up into shorter lengths,

separated by repeaters, to reduce the time to charge the line (Fig. 15(b)). In this case, in order to signal a logic '1' repeaters charge and discharge alternate sections of the link. In contrast, when a logic 1 value is launched on a transmission line (Fig. 15(c)), only part of the line is charged, and this energy propagates down to line to the receive end. On the other hand since the transmission line is terminated, energy is consumed, when the link is not active.

We now compare a transmission line signaling with an equivalent data rate parallel bus. A 9 mm long 16 bit wide parallel bus, implemented with the M5 layer (0.6 µm line spacing and 0.6 µm line width) is used for this comparison. Five sets of large repeaters (NMOS width: 40 µm, PMOS width: 100 µm) are inserted to give a delay of 400 ps. With a 2.5 GHz bus speed, giving a total data rate of 40 Gbps, and assuming an activation rate of 0.5, the 16 bit bus consumes 73.5 mW.

Spice simulation of the transmission line indicates an average signaling power per line of 8.2 mW for a 40 Gb/s 2^{31}-1 pseudo random bit sequence[3]. The total power for the differential transmission line is twice this value, or 15.2 mW. This result can be verified by simple analysis. If we assume the data sequence is dominated by high frequency content, then the impedance presented by the transmission line is approximately equal to the high-frequency characteristic impedance. This leads to an upper limit on the power delivered to the line. In this case, using a characteristic impedance of 29.9 Ω and 1 V signaling, the power delivered to each half line is given by:

$$P_{in} = \frac{1}{2}\mathrm{Re}\{V_{in} I_{in}^*\} = \frac{1}{2}\frac{V_{S,rms}^2}{Z_o} = \frac{1}{2}\frac{0.707^2}{29.9} = 8.36\ mW \quad (7)$$

At the other extreme, if the data rate is low, the impedance presented to the transmitter is the sum of the line parasitic series resistance and termination resistance and the power delivered to each of the differential line is given by:

$$P_{in} = \frac{1}{2}\frac{V_{S,rms}^2}{R_{line,total} + R_L} = \frac{1}{2}\frac{0.707^2}{103.4 + 22.2} = 1.99\ mW \quad (8)$$

The power delivered to the line derived from simulation lies between these two boundary values.

[3] Note that driver power consumption is higher than the power delivered to the line.

Table 1. Power comparison.

Metal technology with standard CMOS	130 nm 6 thin 2 thick copper	
Link length	9 mm repeater, 15 mm serial	
Repeater design (50% activation rate)	73.50 mW	
Power to Transmission line	**Single ended**	**Differential**
Upper limit of power	8.36 mW	16.72 mW
Lower limit of power	1.99 mW	3.98 mW
Simulated PRBS power	8.20 mW	16.40 mW

5. CAD and Design Automation

Although it is likely that transmission lines will replace traditional buses for some global on-chip links, the decision of where and when to use such links is a complex one. (Some have begun to consider this problem from a CAD perspective [18].) The decision involves not only interconnect area and signaling power, but also issues such as latency and link activity. Unlike the case of a bus incorporating repeaters, for given signaling amplitude, the signaling power for a transmission line is largely independent of line length. However, because of attenuation in a lossy line, the amplitude of the signal at the receiver decreases exponentially with line length. The receive signal is not a CMOS amplitude one, and for a small receive amplitude, more power may be required to overcome thermal noise and offset in the receive circuitry. The power comparison must also consider the activity of the link, since a terminated line consumes static power. At a system level, energy can be saved by powering up and down the link as required.

Design of transmission line interconnect itself is also a complex problem. There are tradeoffs involving both the type of transmission line and the layers chosen. A co-planar structure allows better control of characteristic impedance, but a microstrip provides better isolation from other interconnect and from the substrate. Not only should the choice of layers accommodate power distribution and local interconnect, but the material type and thickness should also be considered. Thick lines offer less attenuation, but are more sensitive to the skin effect, since the skin depth becomes less than half the line thickness at a lower frequency than is the case for thin lines. Paradoxically, thinner, lossier lines may be a better choice for higher frequencies. Line width has a direct effect on area, but also affects characteristic impedance and loss. Bends, bridges, terminations, and interconnect process variation also require careful analysis, optimization and simulation.

Simulation and modeling of interconnect is time consuming and difficult. (The prototype links were simulated with EM simulator Maxwell 2D to produce a 192 segment LC model for spice simulation). Accurate prediction of inductance is less difficult than with

traditional interconnect since the return path is well defined in a transmission line, nevertheless netlists incorporating inductance can become large [5]. Much progress has been made in modeling the skin effect and other high frequency effects such as substrate loss [5], [19].

6. Conclusion

With appropriately terminated transmission lines, serial signaling is an attractive alternative to parallel buses for global, on-chip communication. For high speed signaling, these links are more power efficient than traditional parallel buses with repeaters. Lossy transmission lines provide enormous on-chip signaling bandwidth. The challenges are develop circuit techniques to effectively utilize this bandwidth, and to efficiently model these interconnect structures.

7. Acknowledgements

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