A 90-MS/s 11-MHz-Bandwidth 62-dB SNDR Noise-Shaping SAR ADC

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***Abstract*—Although charge-redistribution successive approximation (SAR) ADCs are highly efficient, comparator noise and other effects limit the most efficient operation to below 10-b ENOB. This work introduces an oversampling, noise-shaping SAR ADC architecture that achieves 10-b ENOB with an 8-b SAR DAC array. A noise-shaping scheme shapes both comparator noise and quantization noise, thereby decoupling comparator noise from ADC performance. The loop filter is comprised of a cascade of a two-tap charge-domain FIR filter and an integrator to achieve good noise shaping even with a low-quality integrator. The prototype ADC is fabricated in 65-nm CMOS and occupies a core area of 0.03 mm^2. Operating at 90 MS/s, it consumes 806 μW from a 1.2-V supply.**

***Index Terms*—Analog-to-digital, CMOS, converter.**

I. Introduction

In recent years, charge-redistribution successive approximation (SAR) ADCs have exhibited the highest conversion efficiencies for ADCs with moderate resolution and bandwidth [1]–[3]. For effective resolutions beyond 10 b or so, however, the accuracy of the SAR circuit blocks limits the overall energy efficiency of the converter. At high resolutions, for instance, the DAC voltages become small compared with the input-referred noise of a dynamic comparator, necessitating an additional power-hungry, low-noise preamplifier to drive the comparator. To improve the effective resolution of SAR ADCs, this work introduces a technique that decouples the accuracy of the comparator from the resolution of the ADC.

In this paper, we introduce a low oversampling ratio (OSR) noise-shaping SAR ADC that leverages noise shaping to increase the resolution of a conventional SAR ADC. The prototype converter uses an 8-bit capacitor DAC and achieves an ENOB of 10.0 b over a signal bandwidth of 11 MHz, with an OSR of 4. Through noise shaping and oversampling, we mitigate some of the losses from mismatch, kT/C noise, and comparator noise by trading bandwidth for accuracy, which allows us to achieve higher resolutions using lower resolution and lower accuracy circuit blocks. Significantly, the input-referred noise of the comparator is noise-shaped along with the quantization noise so the comparator no longer requires the full accuracy of the converter. The noise-shaping technique presented in this paper provides a means to enhance the resolution of SAR ADCs without a significant modification to the basic SAR ADC structure.

While SAR ADCs are very efficient for moderate resolutions, fundamental and related second-order effects significantly reduce the efficiency of SAR ADCs at higher effective resolutions. As with all ADCs, kT/C noise limits sampling accuracy. For moderate resolution ADCs, the minimum capacitance to achieve adequate sampling noise is greater that the required capacitance needed to achieve adequate matching. In addition, a large DAC array capacitance leads to second-order effects that also limit performance. These include the signal-dependent resistance of the input switch and slow settling due to parasitic capacitances. Although techniques such as switch gate boosting [5] and redundancy [6], [7] can alleviate these second-order effects, these techniques invariably lead to higher power consumption. A significant advantage of oversampling is that it attenuates kT/C noise, but without noise shaping, oversampling is usually unattractive and until this work, noise shaping has not been efficiently demonstrated in SAR ADCs. [8] describes a noise-shaping system for a SAR ADC and presents simulated data, but a practical implementation of [8] requires a power-hungry opamp to drive the entire DAC array of the SAR ADC. Although noise-shaping ADCs have previously employed SAR ADC structures as a multi-bit quanitzer in sigma-delta ADCs [13], this work embeds noise shaping into the SAR ADC topology while maintaining the power-efficient operation of the SAR ADC.

The input-referred noise of the comparator in a SAR ADC is a fundamental limitation to performance, which we alleviate by noise shaping. In a straight, binary SAR ADC, all trial comparisons must be made at the full accuracy of the overall converter. This requirement determines the maximum input noise of the comparator and in turn the power consumption of the comparator [14]. Moreover, a preamp is often required at higher resolutions due to noise constraints. The large input devices, needed for low-noise comparator operation, increase the parasitic capacitance on the critical top-plate SAR residue nodes. Redundancy schemes can reduce the accuracy needed for the earlier trials, but as noted earlier, redundancy substantially increases the complexity of the ADC. In any case, the later bit trials must still be made to the full ADC accuracy. In this work, a noise-shaping scheme shapes both quantization noise and comparator noise so that comparator noise is decoupled from the ADC resolution.

Noise shaping reduces the number of capacitors in the DAC array, simplifying the practical implementation of the DAC array. It is clear that the number of capacitors in a binary-weighted capacitor DAC array grows exponentially with resolution. While

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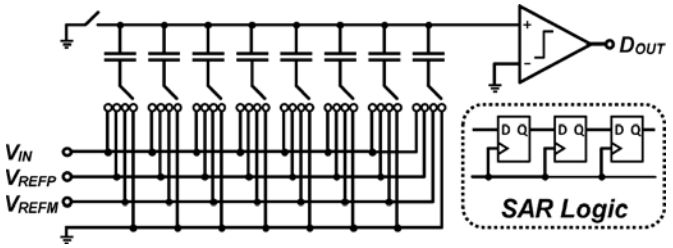

Fig. 1. Basic operation of the SAR ADC.

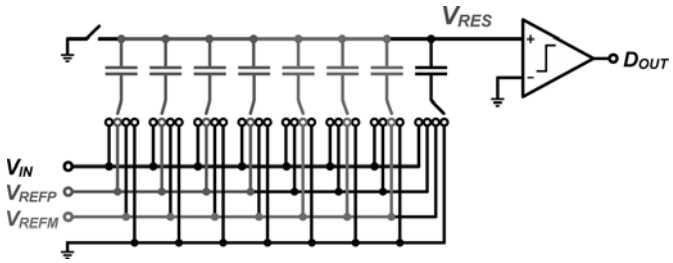

Fig. 2. Residue voltage produced on the DAC after conversion by an 8-b SAR ADC is the difference between the sampled input and a 7-b digital estimate.

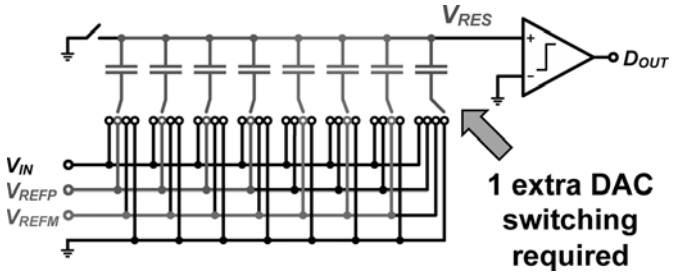

Fig. 3. One extra switching of the DAC array based on the final comparator decision.

by itself this is not a fundamental limit to performance, it does present practical impediments to performance. Routing is necessarily complicated in high-resolution SAR ADCs. Furthermore, the very large ratio between the smallest and largest capacitances can become problematic since the finite minimum value of capacitance can lead to a large total capacitance at high resolutions. The use of a sub-DAC alleviates this problem [11] but the use of a sub-DAC often requires careful calibration of the coupling capacitor [12] Noise shaping reduces the DAC resolution and, therefore, substantially reduces the number of capacitors in the DAC array.

II. SAR ADC Review

Here, we review the basic operation of the SAR ADC architecture used in this work (see Fig. 1). During the first phase of operation, an input voltage is bottom-plate sampled onto a binary weighted capacitor array through a bootstrapped switch. Following this sampling operation, each of the capacitor array bottom plates is initialized to a common-mode voltage, and then the ADC performs a binary search under control of the SAR logic.

In this design, the SAR algorithm performs sign-magnitude encoding of the sampled input voltage, and the capacitor DAC uses bipolar reference voltages during the binary search. Therefore, after the DAC references are initialized to the common-mode reference voltage, the comparator tests the sign of the sampled voltage, and this sign decision is fed back to the bottom plate switches of the MSB capacitor in the DAC. When the subtraction of voltage is required, only the MSB switches move from the common mode reference voltage to a lower reference voltage, and when addition of voltage is required, only the MSB switches move from the common-mode reference voltage to a higher reference voltage. The switches for the rest of array are left at the common-mode reference voltage after this first decision. Throughout the rest of the conversion algorithm, the comparator is enabled, and the decision is fed to the appropriate binary-weighted caps in the array.

III. Noise Shaping in a SAR ADC

A. Residue Generation

We first introduce an efficient and almost seamless technique for measurement of the quantization error. Efficient capture of the quantization error is vital for efficient noise shaping. The quantization error Q is simply defined by this equation:

$$D_{\mathrm{OUT}} = V_{\mathrm{IN}} + Q. \tag{1}$$

In a conventional SAR ADC, the final residue information produced by the SAR DAC at the end of the conversion is discarded when a new input voltage is sampled onto the array for the next analog-to-digital conversion. As discussed in Section II, after each bit trial, the DAC references V_{REFM} and V_{REFP} are connected to capacitor bottom plates so that the comparator input represents the undigitized residue. However, since the analog-to-digital conversion is complete when the comparator determines the least significant bit, the last decision is not fed back to the DAC array. In other words, when the SAR ADC conversion is complete for an N-bit ADC, the magnitude of the residue voltage produced at the top plate of the DAC represents the difference between the sampled input and a digital estimate constructed from the first $N-1$th decision. This is shown in the example of an 8-b ADC in Fig. 2. The residue voltage produced on the DAC after completing the digital conversion by the 8-b SAR ADC is the difference between the sampled input and a 7-b digital estimate. Therefore, the final residue is not based on the full resolution of the digital estimate, and

$$V_{\mathrm{RES}} \neq D_{\mathrm{OUT}} - V_{\mathrm{IN}}. \tag{2}$$

In Fig. 3, we make one extra switching of the DAC array based on the final comparator decision so that the final residue is

$$V_{\mathrm{RES}} = D_{\mathrm{OUT}} - V_{\mathrm{IN}}. \tag{3}$$

Significantly, this final residue voltage also contains information about the input-referred comparator noise, $V_{N,\mathrm{COMP}}$. As indicated in Fig. 4, this final residue also captures the comparator noise for the Nth comparison, so that

$$V_{\mathrm{RES}} = D_{\mathrm{OUT}} - V_{\mathrm{IN}} + V_{N,\mathrm{COMP}}. \tag{4}$$

B. Simple Noise Shaping

For clarity of explanation, we begin with the simple SAR ADC noise shaping technique introduced in Fig. 5. In this technique, the residue $V_{\rm RES}(k-1)$ from the conversion of the previous ADC sample $k-1$ is applied to the negative input of the comparator during the conversion of current sample k. Including comparator noise, $V_{N,\rm COMP}(k)$, $D_{\rm OUT}$ is expressed as

$$D_{\rm OUT}(k) = V_{\rm IN}(k) + Q(k) + V_{N,\rm COMP}(k) - V_{\rm RES}(k-1). \quad (5)$$

Considering that the residue voltage generated by the DAC represents the difference between $D_{\rm OUT}$ and $V_{\rm IN}$, $V_{\rm RES}$ can be expressed as follows:

$$V_{\rm RES}(k) = D_{\rm OUT}(k) - V_{\rm IN}(k). \quad (6)$$

Substituting (6) into (5) and performing a z-transform, we obtain the following system transfer function:

$$D_{\rm OUT}(z) = V_{\rm IN}(z) + \frac{1}{1+z^{-1}}[Q(z) + V_{N,\rm COMP}(z)]. \quad (7)$$

This equation indicates an all-pass signal transfer function (STF) and a high-pass noise transfer function (NTF), which shapes both the quantization noise and comparator noise, thereby attenuating both the quantization noise and comparator noise at lower frequencies.

In practice, the battery that applies $V_{\rm RES}(k-1)$ to the negative input of the comparator can be implemented as a capacitor, $C_{\rm COMP}$. At the end a the SAR conversion, and after the last comparator decision is fed back into the array, the battery capacitor $C_{\rm COMP}$ is charged-shared with the DAC top-plate voltage. Since $C_{\rm COMP}$ is much smaller than the total DAC capacitance, the residue voltage that is sampled onto $C_{\rm COMP}$ is almost identical to the actual residue voltage. Because $C_{\rm COMP}$ is small compared with the DAC, memory effects can also be ignored.

With a small $C_{\rm COMP}$ capacitance, sampling of the SAR ADC residue on $C_{\rm COMP}$ introduces an additional kT/C noise contribution in the ADC operation, which depends on the capacitance of $C_{\rm COMP}$. This kT/C noise, however, presents itself to the comparator in series with the input-referred comparator noise, and, thus, this additional kT/C noise contribution experiences the same noise transfer function as the quantization noise and the input-referred comparator noise. Therefore, noise shaping and oversampling and the eventual digital filtering of the overall ADC output greatly reduce the effective contribution of kT/C noise associated with sampling onto $C_{\rm COMP}$ for this simple noise-shaping technique.

Fig. 6 shows a functional representation and the equivalent signal flow diagram of this simple noise shaping SAR ADC. Thanks to the additional DAC switching, the DAC array generates the quantization residue. Effectively, this ADC architecture feeds forward the ADC input to the quantizer, where a delayed version of this residue is summed with the input and is then fed to the quantizer.

Through this simplified noise shaping implementation, both the quantization noise and the input-referred comparator noise of the ADC can be reduced at the expense of bandwidth. The noise transfer function that is associated with this simple noise shaping is shown in Fig. 7. Although the architecture has the advantage of shaping both quantization noise and the comparator noise, the NTF indicates only a flat 6 dB of attenuation of low frequency. For this reason, the effective improvement in resolution offered by this technique is small. The resolution improvement from this simplified implementation does not trade resolution and bandwidth equally, so, in terms of figure of merit, the resolution improvement is not an energy-efficient design tradeoff.

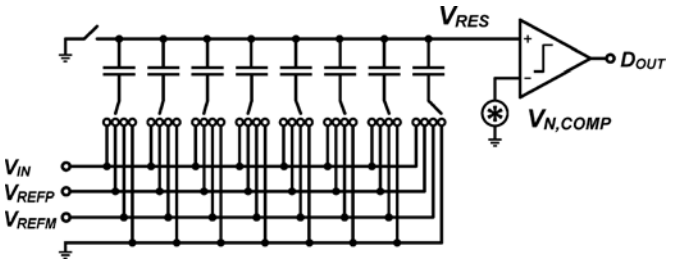

Fig. 4. Final residue also captures the comparator noise for the Nth comparison.

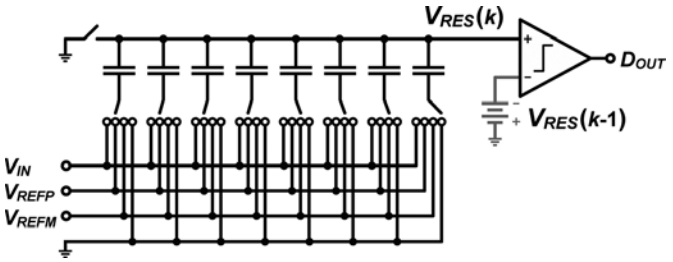

Fig. 5. Simple SAR ADC noise-shaping technique.

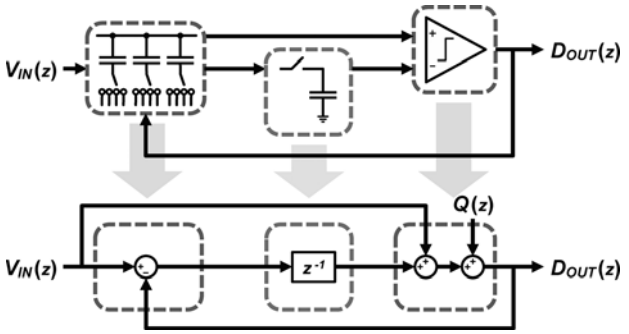

Fig. 6. Functional representation and the equivalent signal flow diagram of the simple noise-shaping SAR ADC.

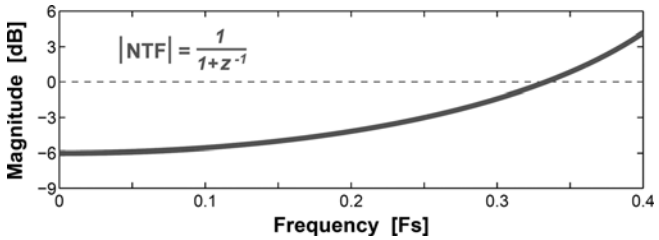

Fig. 7. Noise transfer function that is associated with this simple noise shaping.

C. Improved Noise Shaping

The simplified noise-shaping system described in Section III-B provides an implementation that uses the DAC residue voltage produced at the end of the SAR conversion to

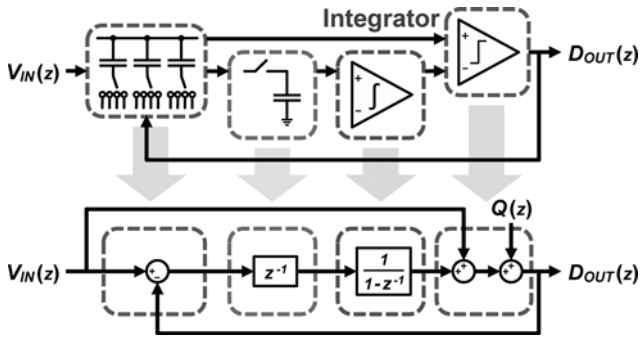

Fig. 8. Functional representation and the equivalent signal flow diagram of the improved noise-shaping SAR ADC.

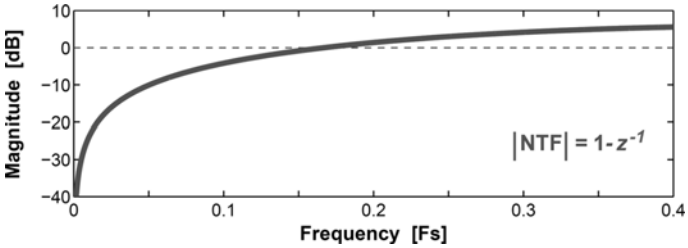

Fig. 9. Plot of noise transfer function for the improved noise shaping SAR ADC.

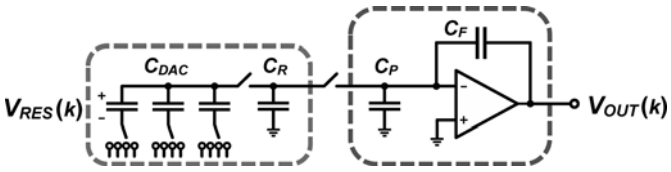

Fig. 10. Simplified depiction of improved noise-shaping SAR ADC.

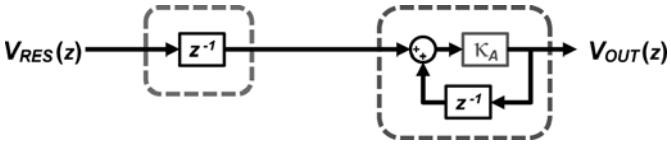

Fig. 11. Model of the residue processing in the improved noise-shaping SAR ADC.

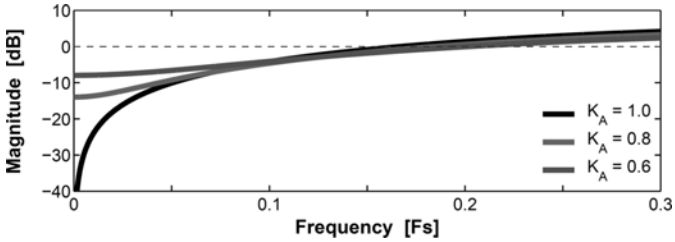

Fig. 12. Noise transfer function for three values of κ_A .

perform noise shaping. We improve the resolution gain of the simplified implementation described in the previous section by inserting an integrator between the passive sampling network and the inverting terminal of the comparator. With ideal sampling of the DAC residue voltage and an ideal integrator, this system behaves exactly like a first order sigma delta modulator.

Fig. 8 shows a functional representation and the equivalent signal flow diagram of the improved noise-shaping SAR ADC, which now includes integration after the sampling of the final DAC residue. As shown in the signal flow diagram, the sum of the fed-forward input and the integrated residue is fed to the quantizer. The transfer function for this improved noise-shaping system is

$$D_{\mathrm{OUT}}(z) = V_{\mathrm{IN}}(z) + \left(1 - z^{-1}\right) Q(z). \tag{8}$$

As before, the STF is all-pass. However, the NTF $1-z^{-1}$ is now identical to the NTF of a first-order $\Sigma\Delta$ modulator. As expected, a plot of noise transfer function, shown in Fig. 9, indicates significant attention of quantization noise at lower frequencies.

To understand the limitations of this improved architecture, we consider the simplified depiction of this system shown in Fig. 10. The DAC residue is sampled by residue-sampling capacitor, C_R, and this sampled charge is then transferred to an integrator, formed by an OTA with a feedback capacitor, C_F. C_P represents parasitic capacitance and includes contributions from the switches and the OTA input. As with the simple noise-shaping scheme in Section III-B, C_R introduces an additional kT/C noise contribution. Unlike the simple noise-shaping scheme, however, this kT/C noise contribution from C_R is not noise-shaped, but is still digitally filtered. Practically speaking, the inclusion of the integrator prevents noise-shaping of this kT/C noise. Therefore, C_R must be sized in accordance with the desired resolution of the ADC in order to keep the kT/C noise negligible. At high resolutions, charge sharing with a large C_R can set the minimum size of the DAC array.

We now consider the effect of finite amplifier gain as well as errors related to the parasitic capacitance C_P. For this purpose, we model the residue processing with the signal flow diagram shown in Fig. 11. In this figure, we introduce a quality factor κ_A for the integrator. A κ_A value of 1.0 indicates an ideal integrator, and, in practice, κ_A is smaller than unity. This quality factor represents losses due to both finite amplifier gain and the attenuation due to charge sharing between C_R and C_P. Fig. 12 plots the noise transfer function for three values of κ_A ranging from 0.6 to ideal. We see that even with a very poor integrator (i.e., κ_A of 0.6), reasonable noise shaping is still obtained. Nevertheless, a higher value of κ_A is typically desired to achieve an attractive tradeoff between bandwidth and resolution. However, a high value of κ_A requires a high-gain amplifier and accurate handling of charge. This extra complexity is undesirable since it is at odds with the scaling friendly nature of the basic switched capacitor SAR architecture.

D. Practical Noise Shaping

We introduce a cascaded FIR-IIR filter as a loop filter to achieve practical noise shaping. To reconcile the design tradeoff between bandwidth and resolution, an additional switched capacitor FIR filter replaces the passive sampling network described in Sections III-B and III-C. Fig. 13 shows the signal flow diagram for the noise-shaping scheme that incorporates this new loop filter. The residue voltage $V_{\mathrm{RES}}(z)$ is processed by the cascade of the FIR and IIR filters to form $Y(z)$. $Y(z)$ is then summed with the fed-forward input and fed to the quantizer. The FIR filter is a two-tap filter with coefficients α_1 and

α_2. If the IIR filter formed with the integrator has a quality factor κ_A, then the overall transfer function is

$$D_{\mathrm{OUT}}(z) = V_{\mathrm{IN}}(z) + \frac{1-\kappa_A z^{-1}}{1-\kappa_A(\alpha_1-1)z^{-1}+\kappa_A\alpha_2 z^{-2}} Q(z). \quad (9)$$

Again, the signal transfer function is all-pass, but now thanks to coefficients α_1 and α_2 there is flexibility in the form of the noise transfer function. In this design, α_1 is set at 3.0 and α_2 is set at 1.0 for a simple integrator with κ_A of 0.64.[1]

The circuit implementation of the cascaded FIR-IIR filter is shown in Fig. 14. The FIR filter is a two-tap filter constructed as a pair of two-capacitor banks. Alternate DAC residue voltages are alternately sampled onto bank 1 and bank 2 at the end of each ADC conversion cycle. As shown in Fig. 15, bank 1 is formed with capacitor C_{A1} and C_{B1} while bank 2 is formed with C_{A2} and C_{B2}. The FIR tap coefficients α_1 and α_2 are set by the size of capacitors (i.e., capacitor designated A and B) within the capacitor banks.

As shown in Fig. 16, the residue voltage, $V_{\mathrm{RES}}(k-1)$, is passively sampled onto C_{B2} and C_{A2}. Later, residue, $V_{\mathrm{RES}}(k)$, is passively sampled onto C_{B1} and C_{A1}. The charges on C_{B2} and C_{A1} are combined to form the FIR filtered charge $Q_{\mathrm{OUT}}(k)$. Next, C_{B2} and C_{A2} are reused to sample the next residue, $V_{\mathrm{RES}}(k+1)$, and after this, the charges on C_{B1} and C_{A2} are combined to form the FIR filtered charge $Q_{\mathrm{OUT}}(k+1)$. We see that interleaved capacitors are required because each residue value must contribute to two FIR filtered outputs and the sampled charge stored on a capacitor is destroyed after a single charge sharing.

Returning to the simplified schematic representation, shown in Fig. 14, the IIR filter is implemented with a simple, single-stage opamp along with feedback capacitor C_F, which sums and integrates the FIR filter tap charges onto a feedback capacitor. The FIR filter taps are summed and integrated during the relatively long signal-sampling period of the SAR ADC to ensure that there is sufficient time for the filter outputs to settle before the start of the next ADC conversion cycle. The overall filtered residue is given as

$$V_{\mathrm{OUT}}(z) = \left[\frac{C_A}{C_F}z^{-1} + \frac{C_B}{C_F}z^{-2}\right] \frac{\kappa_A}{1-\kappa_A z^{-1}} V_{\mathrm{RES}}(z). \quad (10)$$

Fig. 17 compares the noise transfer function for the IIR filter alone (Section III-C) and that of this combined IIR with FIR filter, both with a low κ_A value of 0.6. Even with the low value κ_A, it is clear that the noise attenuation is much improved with the combined IIR/FIR structure. Furthermore the attenuation bandwidth is wide, facilitating a low OSR. Fig. 18 compares the NTF of this noise-shaping SAR ADC and the NTF of an ideal sigma-delta ADCs. As shown in Fig. 18, the NTF for this noise-shaping SAR ADC with FIR-IIR loop filter indicates resolution gains equivalent to a third-order sigma-delta modulator at an OSR of 4.[2]

[1]The tap coefficients chosen for FIR filter produce an unstable filter, but when combined with losses from the integrator, the noise transfer function is stabilized.

[2]Mismatch and noise are not included in the comparison.

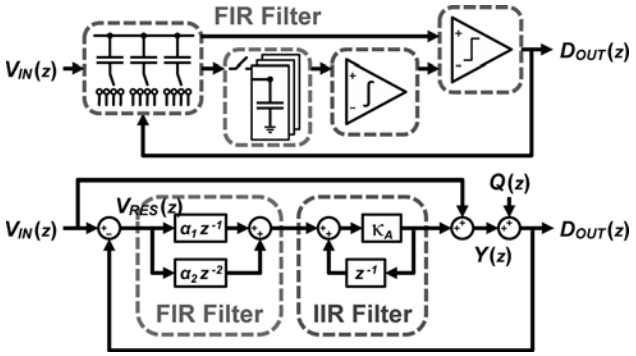

Fig. 13. Noise shaping with cascaded FIR/IIR filter .

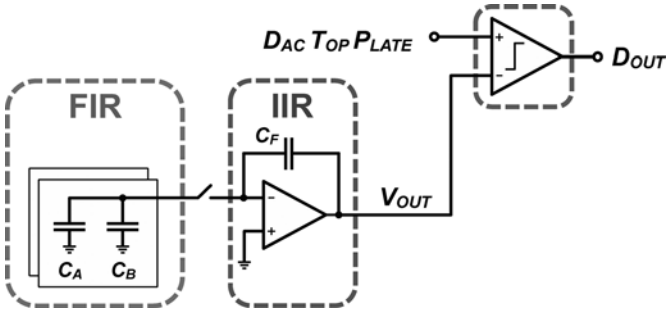

Fig. 14. Circuit implementation of the cascaded FIR-IIR filter.

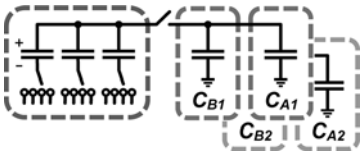

Fig. 15. Capacitor banks in FIR filter.

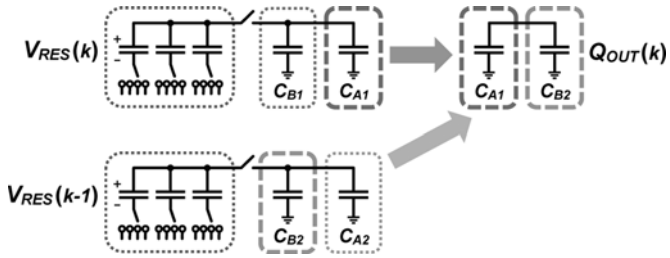

Fig. 16. Interleaved FIR operation.

IV. Circuit Details

The SAR ADC is a fully differential implementation of the architecture shown in Fig. 1, along with a differential realization of the noise shaping circuitry shown in Fig. 13. The loop filter opamp is a simple single-stage low-gain amplifier. The comparator is shown in Fig. 19. The comparator compares the differential residue voltage with the differential filtered residue signal. A simple dynamic structure is employed for energy efficiency. The comparator is double differential version of the double tail latch comparator [4].

To save power and to eliminate the need for a very fast reference clock, the timing for this SAR ADC is generated using an asynchronous clocking scheme. A 90-MHz master clock controls the sampling instance, and a single delay element is

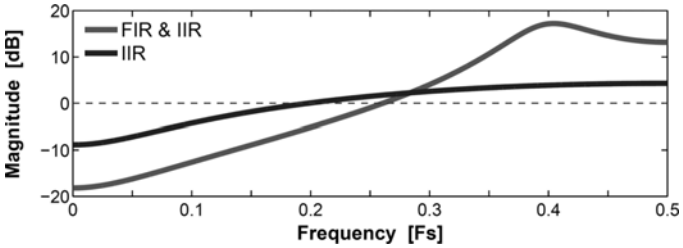

Fig. 17. Noise transfer function for the IIR filter alone (Section III-C) compared to that of combined IIR with FIR filter.

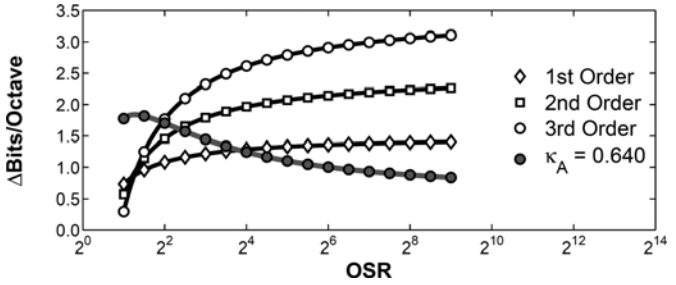

Fig. 18. Comparison in resolution gains between a noise-shaping SAR ADC using a FIR-IIR loop filter and ideal sigma-delta ADCs. Noise and mismatch are not considered. At a low OSR of 4, the FIR-IIR filter provides resolution gains comparable to a third-order modulator.

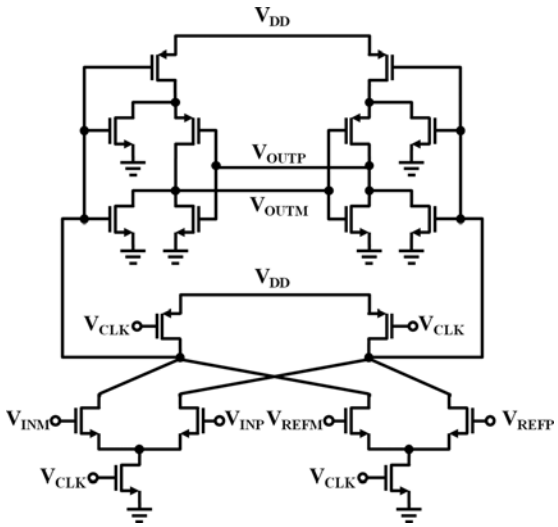

Fig. 19. Comparator.

used to time each of the DAC settling events. The delay element (Fig. 20) consists of a ring-oscillator-type structure with one inversion produced by a flip-flop, which when triggered by the comparator-ready signal, immediately resets the comparator and initiates the inverter delays to time the DAC. By recycling this single delay element, the delays of all DAC settling events match without the use of calibration.

V. Prototype and Measurements

The prototype ADC (Fig. 21) is fabricated in 65 nm CMOS. The ADC occupies an area of 0.03 mm^2 (231 μm by 140 μm) and more than half of this area shown is taken up by decoupling capacitance. The DAC is an 8 bit, binary-weighted capacitor array. Each half of the array has a total capacitance of 640 fF. The unit capacitors are implemented as stacked, finger

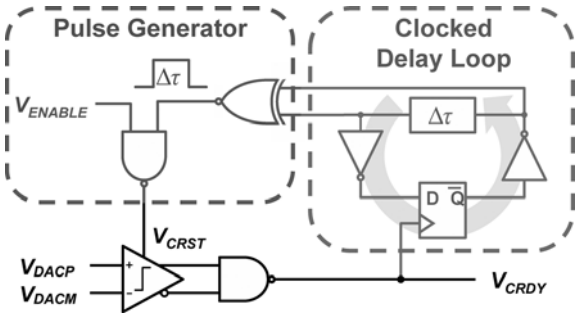

Fig. 20. Clock generation.

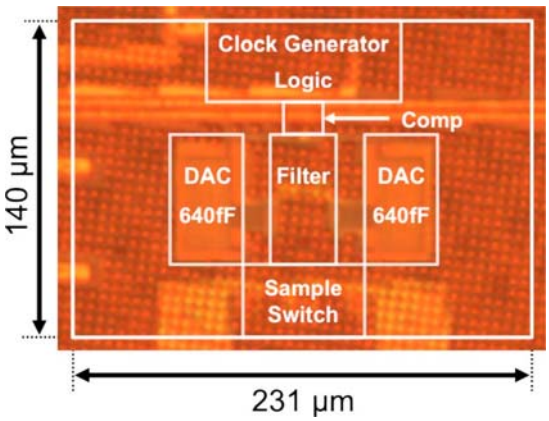

Fig. 21. Die photograph.

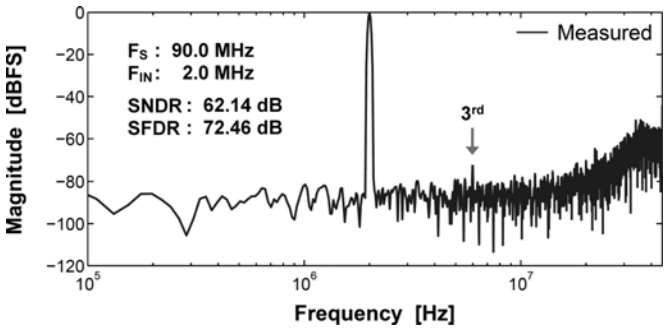

Fig. 22. Measured spectral density of the converter for a 2-MHz input signal sampled at 90 MS/s.

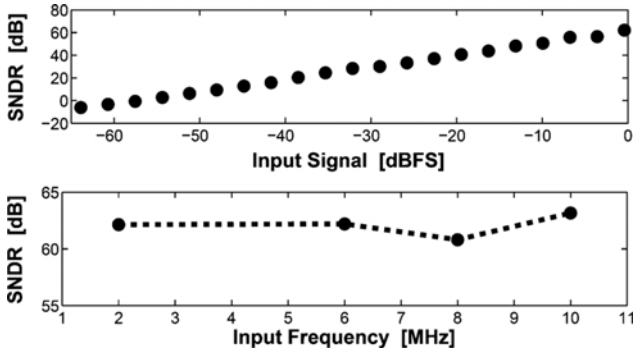

Fig. 23. Measured SNDR versus input frequency and input amplitude.

capacitors. The measured spectral density of the converter for a 2 MHz input signal sampled at 90 MS/s is shown in Fig. 22. With an OSR of 4, the signal bandwidth is 11 MHz and the

TABLE I
COMPARISON TABLE

Specifications	JSSCC'10 [1]	VLSI'10 [3]	ISSCC'11 [4]	ISSCC'10 [14]	ISSCC'10 [15]	This Work
Architechture	SAR	SAR	SAR	SAR	SAR	NS-SAR
Technology (nm)	65	180	65	65	90	65
Resolution (bit)	10	10	10	10	10	---
Bandwidth (MHz)	0.5	5	0.01	25	50	11
Power (μW)	1.9	98	0.206	820	1130	806
ENOB (bit)	8.75	9.83	8.84	9.16	9.51	10
FOM (fJ/conv)	4.42	11	22.4	30	15.5	35.8

ADC achieves a measured ENOB of 10.0 bits with a 2-MHz input signal. The measured SFDR is 72 dB. With a resolution gain of 2-bits above the 8-bit DAC resolution and a reduction of the signal bandwidth by 4, this noise-shaping SAR ADC trades bandwidth and resolution equally in terms of FOM.

The measured SNDR versus input frequency and versus input amplitude are shown in Fig. 23. At 90 MS/s the total power consumption is 806 μW. Of this, the digital power consumption is 608 μW, and the analog power consumption is 198 μW. The analog power consumption includes 30 μW for the comparator, 45 μW for the sampling circuit, 44 μW for the DAC reference voltages, and 79 μW for the FIR-IIR filter. For a 2-MHz input the measured FOM for this converter is 35.8 fJ/conversion-step. Table I provides a comparison with previously published work.

VI. CONCLUSION

This work introduces a new noise-shaping SAR ADC architecture. An OSR noise-shaping architecture allows 10-b ENOB to be achieved with a compact 8-b DAC array. Noise shaping shapes both comparator noise and quantization noise, helping to decouple comparator noise from ADC performance. A loop filter comprised of a cascade of a two-tap charge domain FIR filters and an integrator achieves good noise shaping even with a low-quality integrator. A wide attenuation bandwidth in the noise transfer function facilitates a low OSR of 4.

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