A Fully Self-Contained Logarithmic Closed-Loop Deep Brain Stimulation SoC With Wireless Telemetry and Wireless Power Management

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***Abstract*—Although closed-loop deep brain stimulation (DBS) promises treatment of many neurological disorders, an implantable system-on-chip (SoC) implementing an effective closed-loop DBS algorithm has not been demonstrated. This work introduces a logarithmic, closed-loop DBS system that detects and processes low-frequency brain field signals to control and adapt stimulation currents. The system records and processes neural signals with four low-noise neural amplifier (LNA) channels, a multiplexed logarithmic ADC, and two high-pass and two low-pass digital logarithmic filters. Logarithmic processing saves power and achieves high dynamic range. A logarithmic domain digital signal processor (DSP) and PI-controller controls eight current stimulator channels and enables closed-loop stimulation. An RF transceiver, a clock generator, and a power harvester are also included in the system to achieve a complete implantable SoC. The 4 mm^2 180 nm CMOS prototype consumes a total of 468 μW for recording and processing neural signals, for stimulation, and for two-way wireless communication.**

***Index Terms*—Closed-loop deep brain stimulation (DBS), local field potential (LFP), log-domain DSP, logarithmic ADC, PI controller.**

I. Introduction

DEEP-BRAIN stimulation (DBS) has provided remarkable therapeutic benefits for neurological disorders such as essential tremor and Parkinson's disease [1], [2] . However, despite the long history of DBS and more than a decade of research, the underlying principles of DBS and a mechanism for optimizing stimulation parameters remain elusive. Currently, visual symptoms are the most effective feedback indicator for the optimal selection of stimulation parameters, such as amplitude, pulse-width, and repetition rate. For each patient, there is a unique set of signal amplitudes, pulse-widths and repetition rates that are effective for treatment. With open-loop DBS systems, a post-surgery process called *programming* is necessary for the best results [3]. Initial programming takes 2–3 hours and thereafter the patient is observed for at least 1–2 hours to make fine adjustments. Programming is repeated frequently during the first 6 months and patients must visit a neurologist or a trained technician periodically to ensure the best treatment of symptoms as patient's condition changes over time.

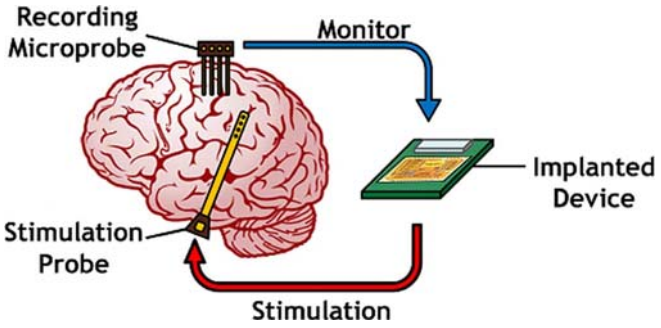

Fig. 1. Conceptual diagram of closed-loop DBS.

Closed-loop DBS promises much simpler programming and also an easier and better patient experience. The principle of closed-loop DBS is shown in Fig. 1. It is believed that the best candidates for the closed-loop feedback signal are abnormal pattern changes in spike signals or changes in the local field potential (LFP) signals. Neural spike signals, also known as action potentials, have bandwidths ranging from 100 Hz to 10 kHz and amplitudes up to 500 μV [4], while LFP signals have bandwidths from 1 Hz to 100 Hz and amplitudes up to 5 mV [5]. Among these, neural spike signals have been considered as a possible candidate for the feedback indicator. To this end, a biomedical multiprocessor system-on-chip (SoC) for closed-loop neuroprosthetic applications has been proposed [6]. This biomedical multiprocessor performs real-time spike-sorting through principal component analysis (PCA). Other work on a closed-loop biomedical system has developed an activity-dependent intracortical microstimulation SoC [7]. This SoC embeds a digital spike discrimination processor that triggers stimulation every time it captures a neural spike signal stronger than a preset threshold. Although the combination of spike sorting and PCA can disentangle spikes, this approach has some drawbacks such as the large power consumption

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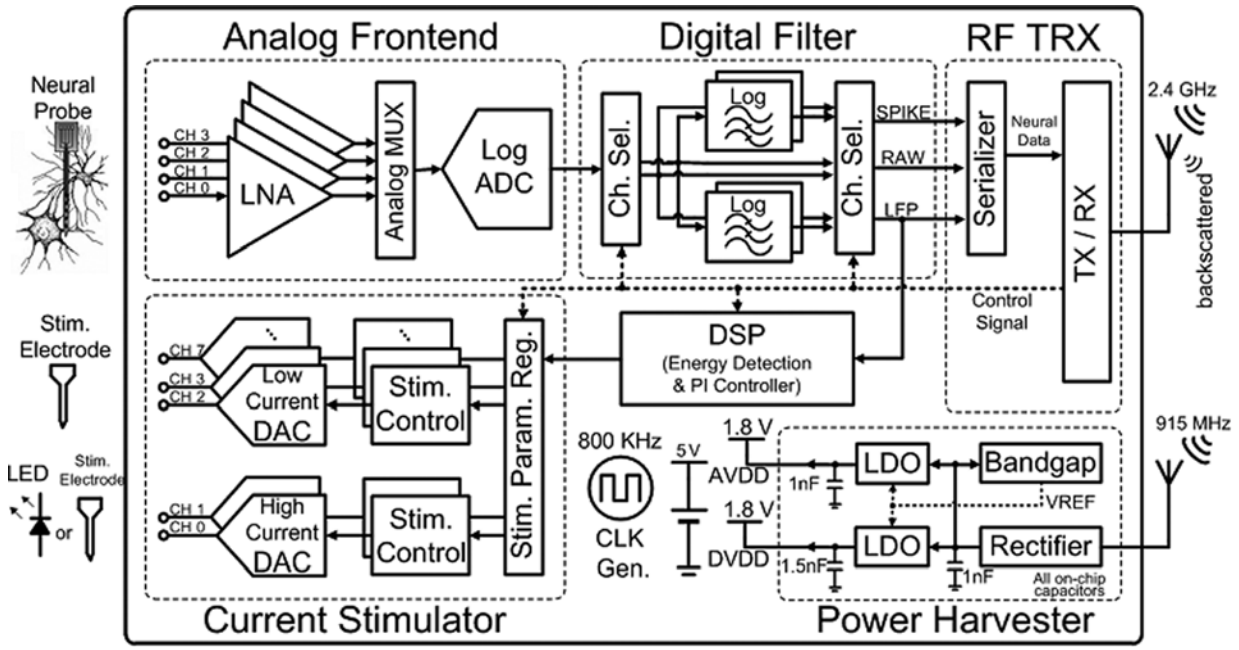

Fig. 2. Overall system block diagram of the proposed log-based closed-loop DBS system.

required for real-time computation [6] and a high sensitivity to stimulation artifacts [7]. Moreover, spike sorting and PCA require significant on-chip computation making wireless powered or long-term battery powered operation difficult.

Recently, features of the LFP signals, and in particular the energy of LFPs, have emerged as a more effective feedback indicator for setting and tuning DBS [8]. An implantable closed-loop microstimulator targeted for DBS therapy uses analog spectral analysis to extract features of the LFP signals [9]. The system incorporates a custom IC for recording and spectral analysis, an auxiliary microprocessor for extracting key bioelectrical signals, and an existing neurostimulator device. However, this system consists of several different ICs, and consumes a lot of power.

In this paper, we describe the first wirelessly-powered closed-loop DBS system-on-chip (SoC) with two-way wireless telemetry. A new closed-loop neural stimulation architecture exploits the logarithmic characteristic of neural signals, so that efficient log-domain digital signal processing extracts information for closed-loop feedback, allowing long-duration battery-powered operation or operation from harvested RF power. The 180 nm CMOS prototype incorporates low-noise neural amplifiers and a log-ADC to efficiently record both low-frequency LFP signals and high-frequency spike signals. A log-based DSP block determines the energy of the LFP signals digitized by the log-ADC. Based on analysis of LFP energy, as proposed in recent brain research [8], an on-chip closed-loop feedback path controls the stimulation channels. The prototype device is fully self-contained and in addition to the recording and stimulation functions it also incorporates energy recovery, voltage regulation and on-chip clock generation to enable a true single-chip solution. To broaden the utility of this system for research, the prototype IC also incorporates two-way telemetry as well as support for optical stimulation for optogenetic research.

II. System Architecture Overview

The overall system architecture is shown in Fig. 2. We significantly improve energy efficiency by introducing a complete logarithmic domain neural recording and processing chain. We take advantage of the fact that neural signals, like many other natural signals, can be elegantly expressed in a logarithmic scale to reduce the bit resolution dictated by the dynamic range. Four band-pass low-noise neural amplifiers (LNAs) filter and amplify neural signals before these signals are multiplexed to a single 100kSample/s 8b logarithmic pipeline ADC [10]. Each LNA has a nominal pass-band gain of 54dB and a passband transition region slope of -40 dB/decade. The logarithmic DSP simultaneously processes the logarithmic-scale digital outputs of two recording channels. Logarithmic domain digital filtering saves power by replacing digital multiplication with simple addition. Similarly, the logarithmic DSP calculates LFP energy by performing simple 1 bit left-shifting instead of squaring. Uniquely, the on-chip DSP in this work also includes a programmable PI-controller that evaluates the LFP energy information to set the optimal stimulation amplitude. An advantage is that the closed-loop feedback is based on low-pass-filtered LFP signals, making the closed-loop DBS operation robust to high-frequency stimulation artifacts.

There are two different types of neurostimulation: voltage stimulation and current stimulation. Since the clinical efficacy of voltage stimulation can gradually decrease as the impedance of the implanted electrodes increases due to reactive tissue response [11], we employ current stimulation in this work because with current stimulation the injected charge is independent of the load impedance. Biphasic stimulation avoids tissue damage

caused by residual charge. Stimulation parameters include the amplitude, the pulse width and the frequency (repetition rate) of stimulation current. Each parameter value is set with 6 bit resolution. As shown in Fig. 2, the stimulator consists of six 6b general-purpose (amplitude up to 116 μA) channels and two 6b high-current (amplitude up to 4.2 mA) stimulation channels. The high current driving capability of the current stimulator allows a LED to be powered and this extends the potential use of this DBS system to optogenetic applications.

The prototype device is wirelessly powered or can run from a battery if high current stimulation is required. Many biomedical systems are powered through low-frequency inductive coupling [12]–[14]. However, considering tissue absorption and antenna performance, recently, much higher frequencies (i.e., GHz) have been used to optimize power transmission [15]. We exploit higher frequency coupling to implement efficient power delivery and to reduce antenna size. The power management block recovers energy from a 915MHz carrier to power the entire system. The power management block is comprised of an RF-DC converter and two on-chip LDOs.

The self-contained single-chip system also incorporates a bandgap reference, bias circuitry and a low jitter clock generator. The jitter of the relaxation clock generator is low enough to support the ADC precision. The stimulation parameters can be directly set via a 2.4 GHz wireless downlink. In addition to the receiver, the device includes a power-efficient 800kbps backscatter RF transmitter that wirelessly communicates recorded LFP, spike or raw data to an external receiver.

III. Logarithmic Signal Recording and Processing

A. Logarithmic Analog-to-Digital Conversion

If we assume an N bit logarithmic ADC with an input voltage, $\mathrm{V_{IN}}$, a full scale input range, $\mathrm{V_{RANGE}}$, a log base, B, and output digital bits $(\mathrm{b_{N-1}}, \mathrm{b_{N-2}}, \ldots, \mathrm{b_0})$, then the transfer function of the ADC is given by [16]:

$$\left[2^N \cdot \log_B\left(B \cdot \frac{V_{in}}{V_{range}}\right)\right] = b_{N-1}2^{N-1} + \cdots + b_0 \quad (1)$$

where [x] denotes the largest integer which is not larger than x. As the input amplitude increases, the quantization becomes coarser. LSB size is given by:

$$LSB = V_{range} \cdot \frac{B^{1/2^N} - 1}{B}. \quad (2)$$

The dynamic range (DR) is defined as the ratio of the input range to the smallest resolvable signal, and can be expressed as:

$$DR = \frac{V_{range}}{LSB} = \frac{B}{B^{1/2^N} - 1}. \quad (3)$$

From this equation, we see that DR increases as the base of logarithmic function, B, and the resolution, N, increase. A logarithmic ADC has a higher DR than a conventional linear ADC of the same bit resolution. We chose $\mathrm{B} = 10$ and $\mathrm{N} = 7$ for this work. An additional bit represents the sign of input, so that the overall ADC resolution is 8bits with one sign bit and seven magnitude bits. From (3) we see that a dynamic range of 54 dB is achieved. This dynamic range is high enough to capture all the information needed, considering the background noise of around 5 $\mu\mathrm{V_{RMS}}$ and practical maximum neural input amplitude of 1.2 mV.[1]

B. Logarithmic Digital Signal Processing

The logarithmic DSP directly processes the logarithmic ADC output. Logarithmic arithmetic used in a digital filter in [17] consumes less power than a linear counterpart, while maintaining a high DR. Recently, a 32 bit processor core based on logarithmic arithmetic was developed for a low-power 3-D graphics system [18]. A logarithmic number system with an additional sign was proposed in early research [19] and this number system is adopted in this work. For a given DR requirement, fewer bits are needed for a logarithmic number system compared to a conventional linear number system. Furthermore, multiplication in linear-domain is equivalent to addition in logarithmic domain, so simple adders can replace power consuming multipliers. The elimination of multipliers and the reduction of number of required bits lead to lower total power consumption.

Addition in the log-domain is less straightforward than multiplication. The most popular way to implement addition in log-domain is a lookup table method that requires an adder and a ROM [20]. The ROM stores the values of $\log(1+10^X)$ for different values of X. We use the look-up table method in our work because of its simplicity. The method is explained with the following equation:

$$\begin{aligned}\log(A+B) &= \log\left(A\left(1+\frac{B}{A}\right)\right) \\ &= \log A + \log\left(1+10^{\log B - \log A}\right) \end{aligned} \quad (4)$$

where A and B are positive numbers. First, $\log B - \log A$ is calculated and the value of $\log(1+10^{\mathrm{logB-logA}})$ is found from the ROM. Finally we get the value of $\log(A+B)$ by adding $\log A$ and $\log(1+10^{\log B - \log A})$.

Addition can be further simplified when either A or B is much larger than the other. When $\log B - \log A$ exceeds a certain value, $1+10^{\log B - \log A}$ approximates to $10^{\log B - \log A}$ and, as a result, $\log A + \log(1+10^{\log B - \log A})$ approximates to $\log B$. The threshold for which this approximation is valid depends on the bit resolution of the digital number system. Fig. 3 visually explains the selective lookup table method. In the case where $\log B - \log A$ is not larger than the threshold, the lookup table is needed to find the exact value of $\log(1+10^{\log B - \log A})$. In the case where B is much larger than A, $\log(A+B)$ approximates to $\log B$. Thus, in the practical implementation, the difference, $\log B - \log A$, is calculated and compared to the threshold value to decide whether to use the lookup table or not.

[1]The neural signals we recorded from a rat's brain rarely exceed 1.2 mV, so we chose 1.2 mV as the maximum input amplitude for our system.

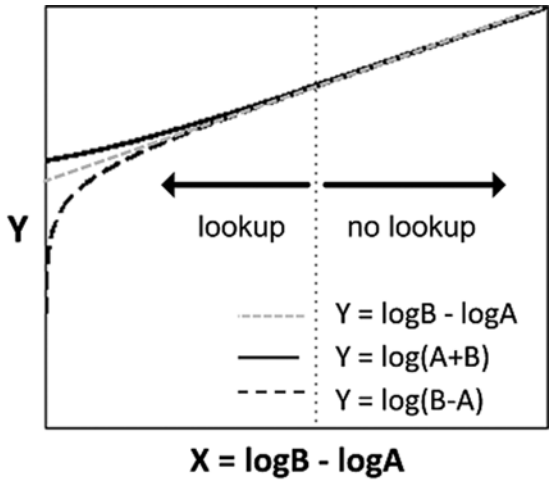

Fig. 3. Lookup table usage decision. $(\mathrm{B} > \mathrm{A} > 0)$.

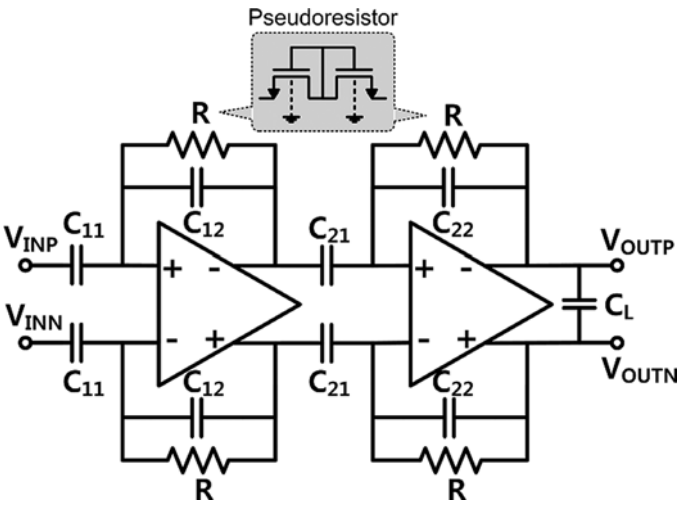

Fig. 4. Schematic of two-stage cascade band-pass LNA.

IV. Circuit Implementation

A. Recording Front-end

Both the spikes and LFP signals carry useful information about the state of the brain [21]. Since the bandwidth and amplitude of these signals differ, few IC systems can simultaneously record both signals. Due to the very different amplitude ranges of spikes and LFPs, the LNAs must simultaneously exhibit a high dynamic range, good noise performance, and wide bandwidth. Given that the full scale input range of the ADC is 600 mV, as explained in Section III-B, and that the input amplitude of LFP signals is around 1 mV and rarely higher than 1.2 mV in our pre-recorded neural data, a pass-band gain of 500 ($=54$ dB) is appropriate for the front-end LNA.

To achieve such a large closed-loop gain, a two-stage cascade structure is chosen for the LNA (Fig. 4). The two-stage structure consumes much less power for the same bandwidth compared to a conventional single stage amplifier. Also, since each stage in the two-stage LNA is a band-pass filter, the two-stage structure suppresses out-of-band signals with a twice-steeper transition region slope compared to a single stage amplifier. Moreover, instead of implementing a feedback capacitance 500 times larger than input capacitance, the two-stage amplifier has a much smaller total capacitance. The first stage has a pass-band gain of 50, and the second stage has a gain of 10. This gain distribution means $\mathrm{C}_{12} = 50 \cdot \mathrm{C}_{11}$ and $\mathrm{C}_{22} = 10 \cdot \mathrm{C}_{21}$, and, assuming $\mathrm{C}_{11} = \mathrm{C}_{21}$, the total feedback capacitance is $60 \cdot \mathrm{C}_{11}$ instead of $500 \cdot \mathrm{C}_{11}$ in the case of a single-stage amplifier. The larger gain of the first stage reduces the input-referred noise of the entire LNA due the second stage.

The first and second stage amplifiers are NMOS input folded cascode amplifiers. As shown in Fig. 4, a pseudoresistor comprised of two back-to-back diode-connected NMOS transistors emulates a high resistance, as large as $10^{11}\ \Omega$. Compared to the configuration in [22], this configuration reduces the parasitic capacitance at both the input and output nodes of the amplifier because the gates of NMOS transistors are connected within the pseudoresistor. The simulated input-referred noise of the front-end LNA is 6.0 $\mu\mathrm{V}_{\mathrm{RMS}}$, which is comparable to the microelectrode noise and background cortical activity noise $(5\ \mu\mathrm{V})$ [23]. The nominal high-pass cutoff and low-pass cutoff frequencies are 1.4 Hz and 6 kHz, respectively, which ensures a wide enough pass-band to simultaneously record both LFP and spike signals.

A simplified block diagram of the 8b pipeline log-ADC is shown in Fig. 5. First, the sign of input is determined. The input is inverted if negative because log functions can only operate on positive inputs. After sign detection, the input is processed through a SHA, five 1.5b $\log$ stages, and a 2b flash final stage. A digital correction block collects the digital bits and assembles an 8b output. A direct logarithmic implementation of the 1.5 bit per stage pipeline requires squaring to replace the multiplication-by-2 operation in a linear domain pipeline and conditional multiplication to replace the conditional addition or subtraction. Fig. 6 explains the conditional multiplication scheme and shows the scaling of the reference voltages and the multiplication gains for the different stages. To avoid analog squaring, the reference voltages for the comparators and the gain settings are scaled in order to achieve the same result as squaring the output of each 1.5 bit stage [24].

Fig. 7 shows one of the fully differential 1.5 bit stages of the logarithmic ADC. Three clock signals φ_1, $\varphi_1{}'$, and φ_2 control the operation of the 1.5 bit stages and implement bottom-plate sampling. When $\varphi 1$ is high, the stage input is sampled and the output is reset. When φ_2 is high, the two comparators decide the output bits and the residue is amplified with a gain that depends on the bit decision. The clock $\varphi_1{}'$ is used for bottom plate sampling. A two-stage regenerative comparator is used for the 1.5 bit sub-ADCs. The size of the input pairs of the comparators is increased for progressive stages in the pipeline, as the mismatch requirement becomes stricter because the signal range decreases along the pipeline. Table I gives the reference voltage values and the gains for each stage.

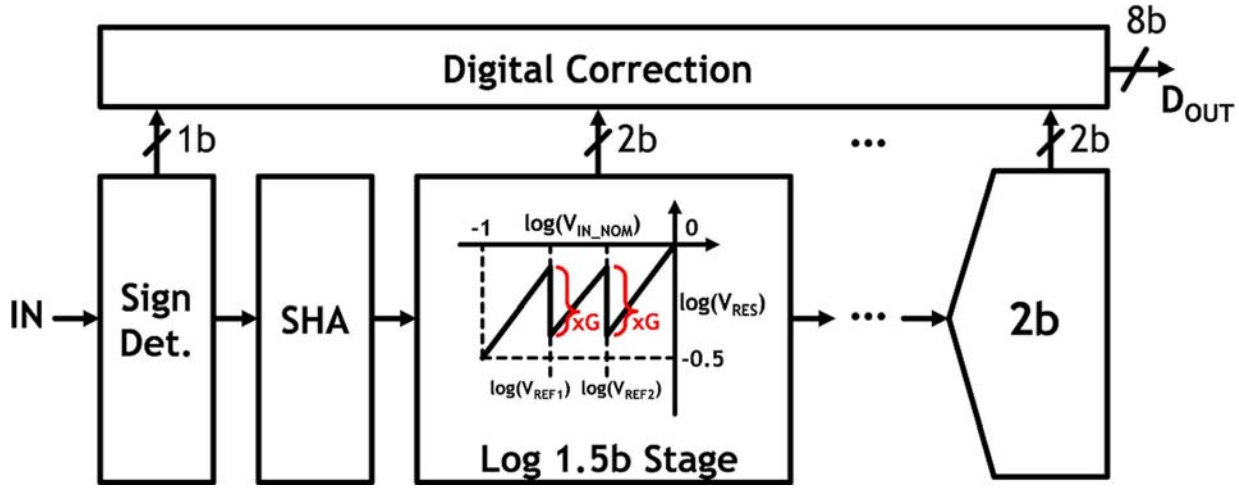

Fig. 5. Block diagram of 8b logarithmic pipeline ADC.

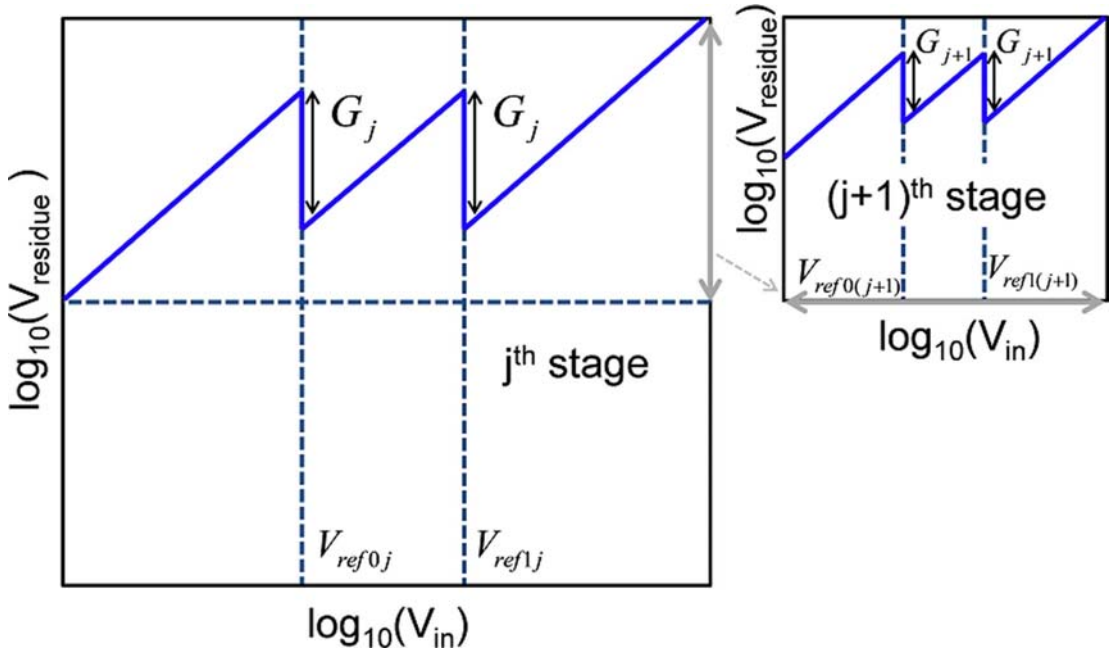

Fig. 6. Scaling of reference voltages and conditional gains from j^{th} stage to $(\mathrm{j}+1)^{\mathrm{th}}$ stage.

B. Logarithmic Digital Filters and Closed-Loop Stimulation Controller

Log-domain digital filtering is introduced in this work to take advantage of the logarithmically encoded signals, and to directly process the log-scale digital output of the ADC. In the prototype system, two sets of high-pass and low-pass 15th order log-domain digital FIR filters separate spikes and LFPs in two channels (Fig. 2). The LPFs and HPFs have the same 3 dB cutoff frequency of 700 Hz. A block diagram of the 15th order digital log-filters is shown in Fig. 8. The digital log-filters receive a sign bit and the log-domain absolute value for each input signal. A ROM stores 16 filter coefficients. The high-pass and the low-pass filters are implemented in the same way but with different stored coefficients.

The digital circuitry reuses key blocks to minimize the area of the 15th order digital log-filters. A 400 kHz clock signal is derived from the 800 kHz system clock. Since the 400 kHz clock is 16 times faster than 25 kS/s data rate for each channel a single linear adder and a single logarithmic accumulator are reused 16 times for each 25 kS/s input. Compared to a conventional cascade FIR filter structure that has as many delay cells, multipliers, and adders as the order of the filter, this hardware reuse significantly reduces silicon area. A linear adder multiplies the absolute values of logarithmic input with the filter coefficients, while an XOR gate multiplies the sign with the sign coefficient. A log accumulator accumulates 16 filter products at 400 kHz and produces the final 25 kS/s filtered output. As illustrated in Fig. 9, the digital log-filters consume 48% less power than equivalent linear-filters thanks to the substitution of power-hungry multi-

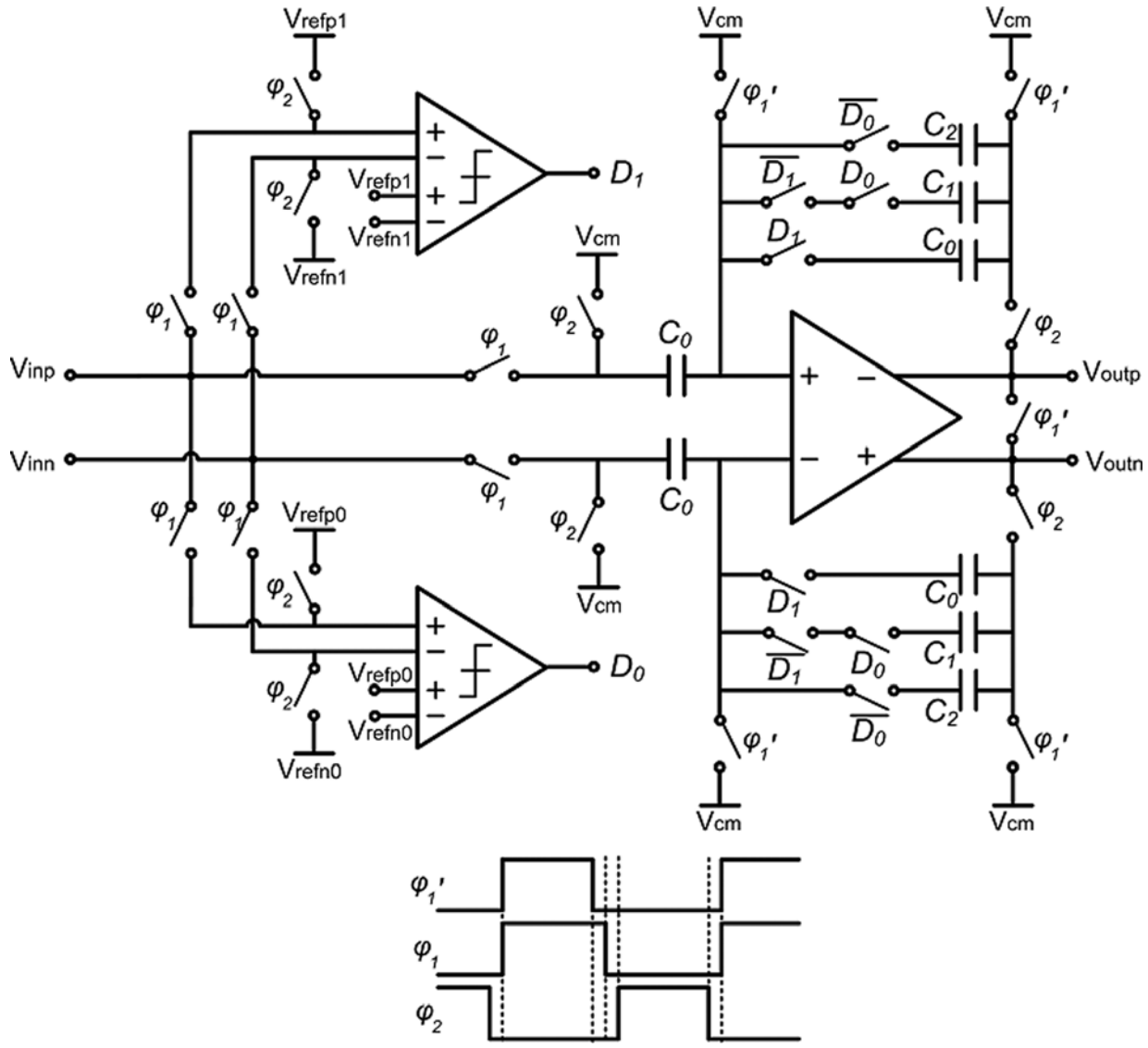

Fig. 7. Simplified schematic of a logarithmic 1.5 bit stage.

TABLE I
VOLTAGE REFERENCE AND GAIN SETTINGS IN THE LOGARITHMIC 8-BIT ADC WITH B = 10. * VREF2 IS NEEDED FOR THE 6TH STAGE BECAUSE A 2-BIT FLASH ADC NEEDS THREE COMPARATORS

Stage (j)	1st	2nd	3rd	4th	5th	6th (2-bit Flash)
V_{ref0j}	142 mV	292 mV	419 mV	501 mV	548 mV	568 mV
V_{ref1j}	253 mV	389 mV	484 mV	539 mV	568 mV	579 mV
V_{ref2j}*	-	-	-	-	-	589 mV
G_{0j}	3.162	1.778	1.334	1.155	1.075	-
G_{1j}	1.778	1.334	1.155	1.075	1.037	-
G_{2j}	1	1	1	1	1	-

pliers with adders and the aforementioned selective look-up table method.

In this work, we introduce a closed-loop stimulation controller that includes a generic P.I. controller that optimizes the stimulation current in real-time. The P.I. controller adjusts the stimulation parameters based on the calculated LFP energy in order to optimally suppress abnormal activity in the brain. A simplified signal flow diagram of the proposed closed-loop DBS is shown in Fig. 10. The log approach simplifies the calculation of LFP energy in the PI-controller. Instead of using squaring, the log-DSP determines the energy of the log-domain LFP signals with simple logical 1 bit left-shifting. The product of controller

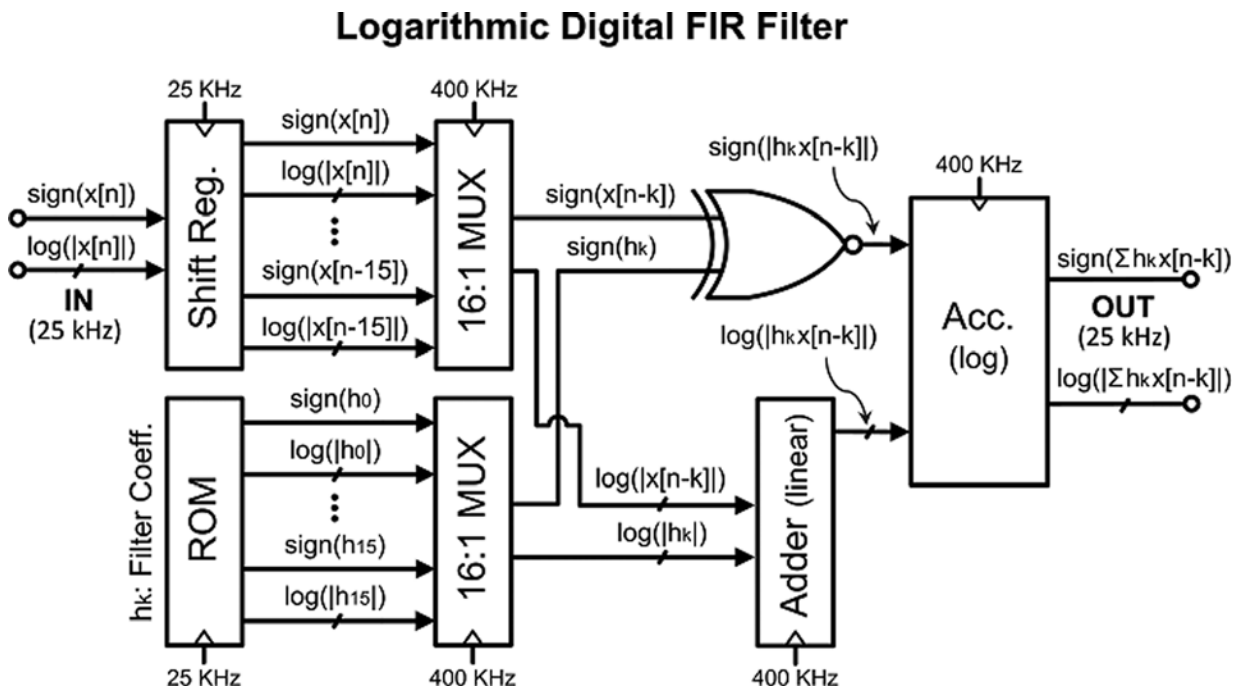

Fig. 8. Block diagram of digital logarithmic low-pass and high-pass filters.

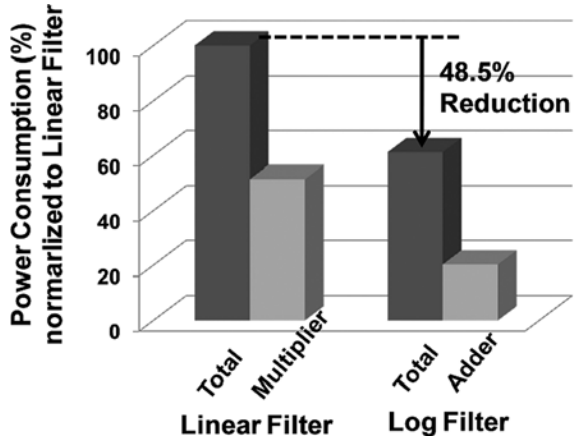

Fig. 9. Simulated power consumption of a linear-domain filter and log-domain 10 bit FIR digital filters.

constants (K_P and K_I) and the present input and integrated input are calculated in the log-domain through simple addition. The difference between input LFP energy and a reference energy value is calculated by the lookup table method. Using an accumulator and a logarithmic adder, the P.I. controller generates a final output and this output sets the current amplitude in real time.

C. Current Stimulator

Current stimulation is selected for this work because a good current mode stimulator injects a constant charge into tissue, irrespective of fluctuations of load impedance. Biphasic stimulation is implemented to avoid tissue damage caused by residual charge. Programmable stimulation parameters include amplitude, pulse width and stimulating frequency (repetition rate or period) of stimulation current. The amplitude value is stored to 6 bit precision.

Fig. 11 shows a block diagram of the prototype 8-channel current stimulator. The current stimulator is comprised of three parts: eight 6 bit current steering DACs, dedicated DAC controllers for each DAC, and stimulation parameter registers. Stimulation parameters are either determined by the closed-loop stimulation controller in closed-loop operation or set directly by the user in open-loop mode through an SPI interface or through the RF receiver. The DAC controllers configure the current DACs to generate biphasic current stimulation with the amplitude, pulse-width and repetition rate stored in the registers. To support a variety of stimulation probes, six DACs are designed to drive currents up to 116 μA, while the two other DACs can drive up to 4.2 mA. The high current channels can drive miniature LEDs for optogenetic applications as well as low impedance DBS probes. Because of the high current drive capability, the high current DACs are designed to run from a 5 V supply while the other DACs are powered from the main power management block. Operating from a 5 V supply, a current up to 3.3 mA can be supplied to a DBS probe (impedance range of $473 \pm 159\ \Omega$ [25]). Since the DAC controller operates from a 1.8 V supply voltage, level shifter circuits interface between the controller and the high current DACs. A triple-cascode current-steering DAC structure enhances the output impedance of both the general and the high current DACs to improve linearity. The ranges of stimulation parameters are summarized in Table II.

D. RF Telemetry

In this work, a low-power backscatter based RF transceiver communicates to an external device. The power-efficient backscatter RF transmitter communicates recorded LFP, spike or raw data wirelessly to an external receiver at a data rate of 800 kbps. The RF transceiver consumes only 5 μW from a

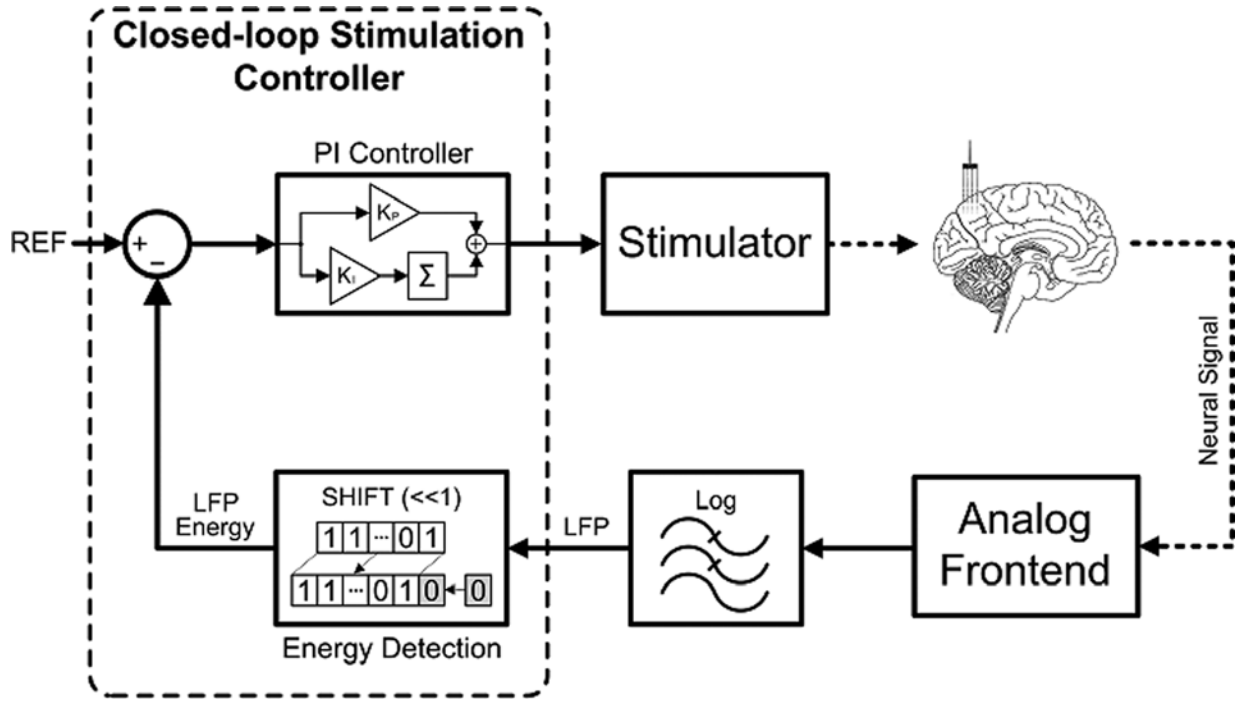

Fig. 10. Block diagram of the proposed closed-loop stimulation that uses LFP energy information as a feedback indicator.

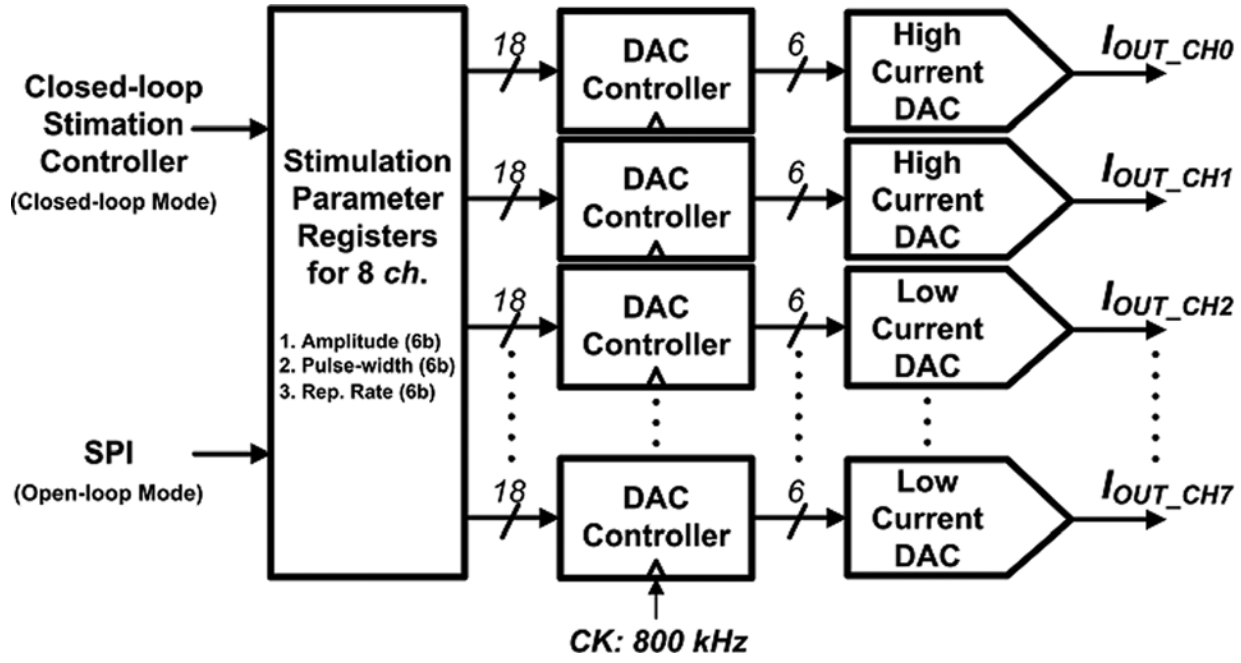

Fig. 11. Block diagram of 8-channel current stimulator.

TABLE II
SUMMARY OF RANGES OF STIMULATION PARAMETERS

	Amplitude	Pulse-width	Period
High-current DAC	0 – 4.2 *mA*	1 *ms*	65 *ms*
General-purpose DAC	0 – 116 μA	1 *ms*	65 *ms*

1.8 V supply in transmit mode. Recently, backscatter communication has been used for implanted systems [26], [27]. In RFID applications where there is no dedicated power source, backscatter communication is attractive because of its

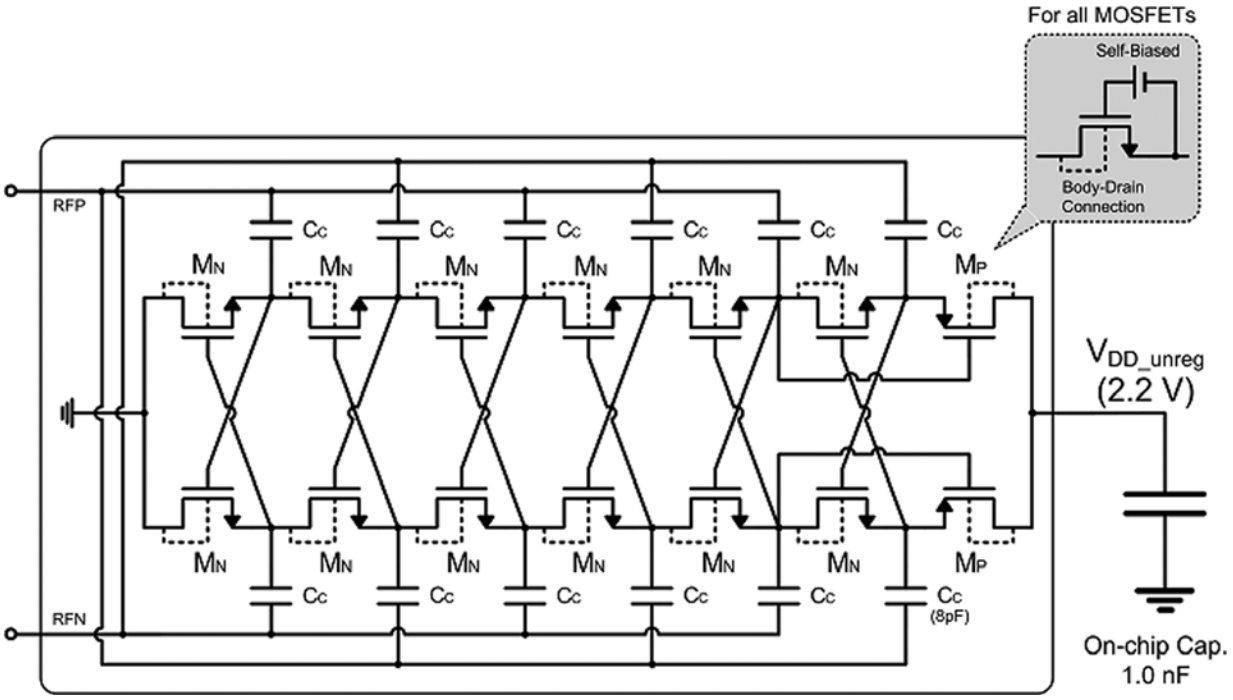

Fig. 12. Schematic of full-wave rectifier that generates unregulated V_{DD} of 2.2 V from a 915 MHz carrier.

TABLE III
PASS TRANSISTOR DIMENSION AND LOAD CAPACITANCE OF LDOS

	Pass transistor dimension (*W/L*)	**Load capacitance (C_L)**
LDO for Digital	$40\mu m$ / $180nm$	1.5 *nF*
LDO for Analog	$20\mu m$ / $200nm$	1.0 *nF*

extremely low power consumption and the simplicity of the transmitter design [28]. The backscatter transmitter consists simply of buffers and a switched transistor for impedance modulation. The impedance connected to the antenna changes depending on the transmitter input because the switched transistor changes the load.

E. Power Management

Wireless power delivery has many advantages for implantable devices including the elimination of a battery inside a human body. In this work, we implement a power management block comprised of a highly efficient RF-DC converter, two LDOs, and a bandgap reference circuit. The power management block generates 1.8 V from a 915 MHz carrier to power the entire DBS system. The high-current DACs require a 5 V battery.

A schematic of the RF-DC converter is illustrated in Fig. 12. A full-wave, self-threshold-compensated rectifier is chosen for its high power conversion efficiency [29]. At every phase, one half of the rectifier delivers charge to the on-chip capacitor. However, in an improvement over [29], here the body of each FET is tied to the drain for both lower on-resistance and less reverse-bias leakage. The rectifier generates an unregulated V_{DD} of 2.2 V and charges a 1 nF on-chip capacitor. The prototype RF-DC converter exhibits a power conversion efficiency of 52% when the load current is 350 μA.

TABLE IV
POWER BREAKDOWN OF THE PROTOTYPE SYSTEM

Part	**Power Consumption**	**Condition**
LNA	$16\mu W$/ch.	-
Log-ADC	$180\mu W$	-
High-Current Stimulation Ch.	$62\mu A$/ch.	4.2 *mA* amplitude, 1 *ms* pulsewidth, 15.4 *Hz* repetition rate.
Low-Current Stimulation Ch.	$3\mu A$/ch.	116 μA amplitude, 1 *ms* pulsewidth, 15.4 *Hz* repetition rate.
Digital (Filters+Stim. Controller)	$138\mu W$	All four filters (two LPFs and two HPFs) are active.
RF Transceiver (TX/RX)	$5\mu W$ / $4.6\mu W$	One of TX and RX active at a time.
Clock Generator	$60\mu W$	800 *kHz* clock output.
Total	**$468\mu W$**	All 6 general-purpose stimulators are active with 116 µA amplitude.

A schematic of the LDO that generates the supplies for the analog and the digital domains is shown in Fig. 13. The LDO consists of a folded cascode amplifier as an error amplifier, a

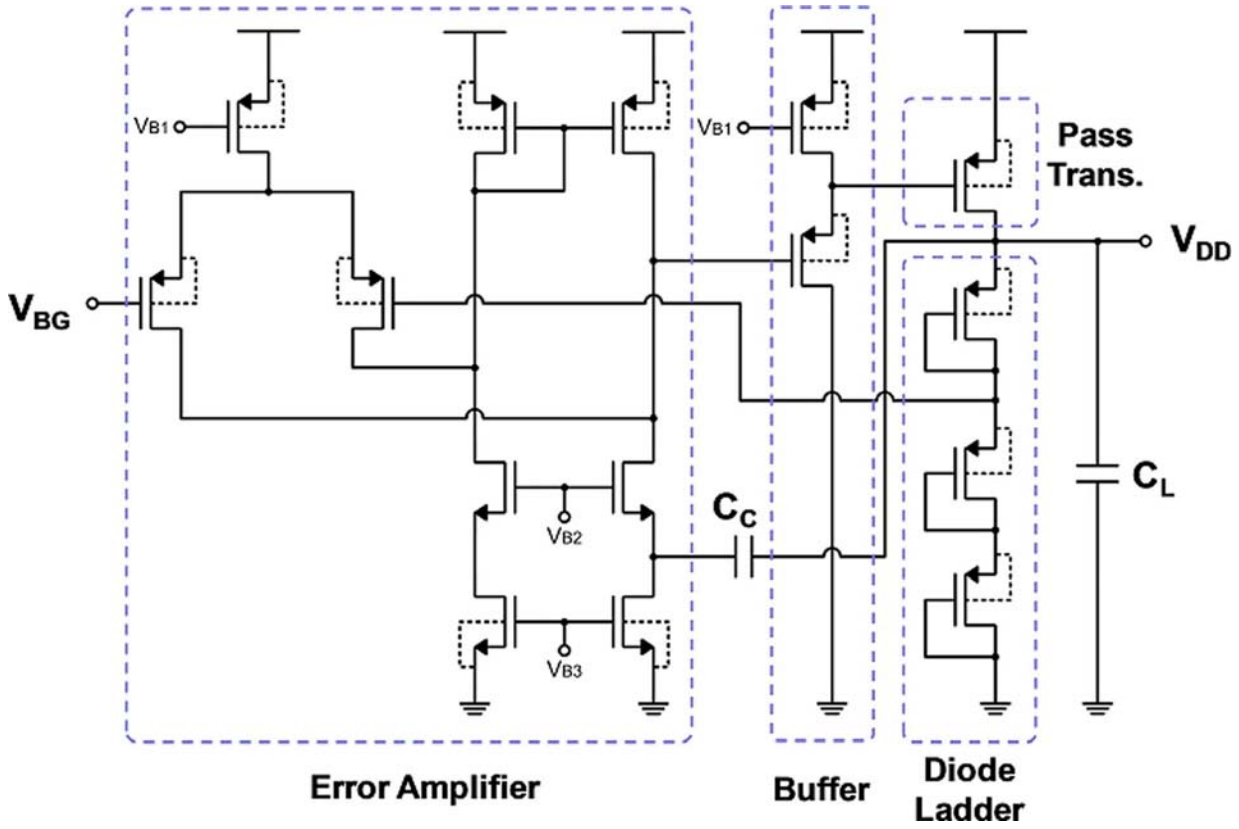

Fig. 13. An LDO generates a supply voltage for analog and digital domains.

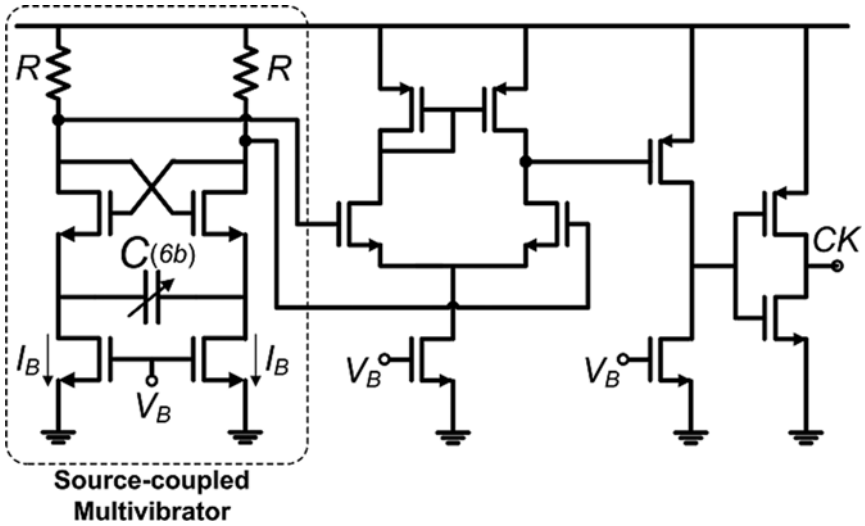

Fig. 14. Clock generator.

buffer, and a pass transistor with a diode ladder and a load capacitor. To minimize power consumption a diode ladder instead of a resistor ladder sets the supply voltage values. The LDO loop is closed by connecting the output node in the diode divider ladder to the negative input node of the error amplifier. A bandgap reference voltage, V_{BG}, functions as the reference input to the opamp. The pass transistor dimensions and the load capacitance values for the LDOs are given in Table III. A stack of MOSCAP, MOMCAP, and MiMCAP is used in the empty areas in the system to maximize the capacitor density. Also, MOMCAP and MiMCAP are stacked on top of the digital circuitry for the same purpose. The pass transistor of the digital domain LDO is larger than that of the analog domain LDO for better transient performance required to handle digital supply spikes. The LDOs are fully implemented on-chip and require no external passive components.

F. Clock Generator

For stand-alone operation, the system needs a low-power on-chip generated clock signal. In this work, a source-coupled

TABLE V
PROTOTYPE PERFORMANCES SUMMARY

Analog Front-end	
LNA Gain	54 *dB*
LNA 3dB Passband	0.64 *Hz* – 6 *kHz*
Input Referred RMS Noise	6.3 μV_{RMS}
Noise Efficiency Factor (NEF)	3.76
Logarithmic ADC Sampling Rate	100 kSample/s
Analog Front-end Max DNL/INL	0.82 *LSB* / 0.89 *LSB*
Analog Front-end SNDR	35.5 *dB* @ 170 *Hz*
Analog Front-end Power Consumption	245 μW
Current Stimulator	
Maximum Current of High/Low Current DAC	± 4.18 *mA* / ± 116 μA
Charge Unbalance of High/Low Current DAC	< 9% / < 0.1%
Amplitude Resolution	6-bit
Repetition Rate	15.4 *Hz*
Pulse Width	1 *ms*
Digital Filters + Stimulator Controller	
Clock Frequency	400 *kHz*
3*dB* Cutoff Frequency of LPF / HPF	700 *Hz* / 700 *Hz*
Power Consumption	138 μW
RF-DC Converter	
Carrier Frequency for Power Harvesting	915 MHz
Simulated Rectifier Power Conversion Efficiency	52% @ I_{Load} = 350 µA
RF Transceiver	
Communication Scheme of TX / RX	Backscatter / PWM
Carrier Frequency for RF Communication	2.4 *GHz*
Data Rate TX / RX	800 *kbps* / 100 *kbps*
Power Consumption TX / RX	5 μW / 4.6 μW
Clock Generator	
Output Frequency	800 *kHz*
Simulated Cycle Jitter	176 *ps*
Power Consumption	60 μW
Total Power Consumption	**468μW**
Technology	**180*nm* 1P6M CMOS**
Die Size (excluding pads)	**2 x 2 mm^2**

multivibrator generates an 800 kHz on-chip clock signal for the entire system. Fig. 14 shows a schematic of the clock generator. To maintain an ideal ADC effective resolution considering jitter above 10 bits, the clock generator is designed to achieve a cycle jitter of 176 ps while consuming only 60 μW from 1.8 V supply and occupying only 20×20 μm^2. In normal operation, the capacitor C is always being charged by one of the source-coupled NMOSs. As the V_{GS} of the switch becomes smaller than the threshold voltage because of the accumulated charge on C, the closed switch turns off and the open switch turns on. The current flow path is changed and the direction of charge accumulation on the capacitor is reversed. This process repeats and generates a periodically alternating output. The jitter performance of the multivibrator improves inversely to the bias current as the uncertainty of switching instant becomes smaller with larger current. An open-loop two-stage amplifier and an inverter follow the source-coupled multivibrator to generate a rail-to-rail square wave from the small amplitude output of the source-coupled multivibrator. In addition, a 6 bit digitally controlled capacitor array allows an accurate 800 kHz output even with significant process variation.

V. PROTOTYPE AND MEASUREMENTS

The prototype logarithmic closed-loop DBS SoC is fabricated in 180 nm CMOS. Fig. 15 shows a die micrograph of the

TABLE VI
PERFORMANCE COMPARISON WITH OTHER RECENT WORKS

	This work	[26]	[13]	[7]
Recording Front-End	Yes	Yes	No	Yes
Number of channels	4	1		8
AC Gain [dB]	54	49		60
Low cutoff freq [Hz]	0.64	100		1.1 - 525
High cutoff freq [KHz]	6	2.5 - 6.2		5.1 - 12
ADC type	Pipeline (log)	SAR		SAR
ADC resolution [bit]	8	8		10
Sample rate [KS/s]	100	80		35.7
DNL / INL [LSB]	< 0.82 / 0.84			< 0.8 / 0.8
SNDR [dB]	35.5			42.18
Power [µW/channel]	61.25			32.8
DSP	Yes	No	No	Yes
Operation	Digital LPF/HPF, LFP energy Detection, PI controller			Spike discrimination
Power [µW]	138			12.4
Stimulating Back-End	Yes	No	Yes	Yes
Number of channels	2 + 8		100	8
Max current [A]	4100µ / 116µ		600µ	94.5µ
DAC resolution [bit]	6		4	6
Transmitter	Yes	Yes	No	Yes
Type	Backscatter	Backscatter		FSK
Frequency [MHz]	2400			433
Data rate [kbps]	800	150~800		
Power [µW]	5			200
Oscillator	Yes	Yes	No	Yes
Output frequency [KHz]	800	1200 - 6400		1000
Power [µW]	60			20.8
Power supply	RF-DC (915MHz) 5V battery	RF-DC (915MHz)	Inductive (1-10MHz)	1.5V battery
Technology [µm]	0.18	0.13	1.2	0.35
Total area [mm²]	4	1.54	21.62	10.9

prototype system. The total system (excluding I/O pads) occupies 2×2 mm^2.

The prototype system is powered by a 915 MHz signal in a wirelessly powered mode, when Performance of the prototype system is measured. A 5 V battery is used only when high-current stimulators are used. The DNL/INL and output spectrum of the analog frontend (4 LNA channels and log-ADC combined) are measured with an input signal of 1.2 mV amplitude applied. The measured DNL and INL are shown in Figs. 16 and 17, respectively. The maximum DNL/INL are 0.82 LSB/0.89 LSB, and the maximum measured SNDR is 35.5 dB and the ENOB is 5.6 bit accordingly. A 10b dynamic range is achieved with the 8b logarithmic ADC with some trade-off in SNDR because of the log operation [10]. Fig. 18 shows the measured frequency response of the recording path (analog front-end and digital log-filters combined) when an input signal with amplitude of 1.2 mV is swept in frequency. The LNAs achieve a measured gain of 54 dB over a pass-band from 0.64 Hz to 6 kHz. Both the low-pass and high-pass digital filters have a 3 dB cutoff frequency of 700 Hz. Measured raw, LFP and spike recordings of a pre-recorded rat-brain neural signal recorded by the prototype are also shown in Fig. 19. These results clearly demonstrate that the log-scale recording path records neural signals in the frequency range of interest.

Fig. 20 shows measurements of stimulation current pulse trains in open-loop mode, with the current amplitudes set manually to the maximum amplitudes of 116 μA and 4.19 mA for the general-purpose and high-current stimulation currents, respectively. Fig. 21 shows a measurement of the stimulation current in closed-loop mode. The stimulation current changes automatically in real-time and the variation of the current depends on the P.I. constants, reference energy value, and

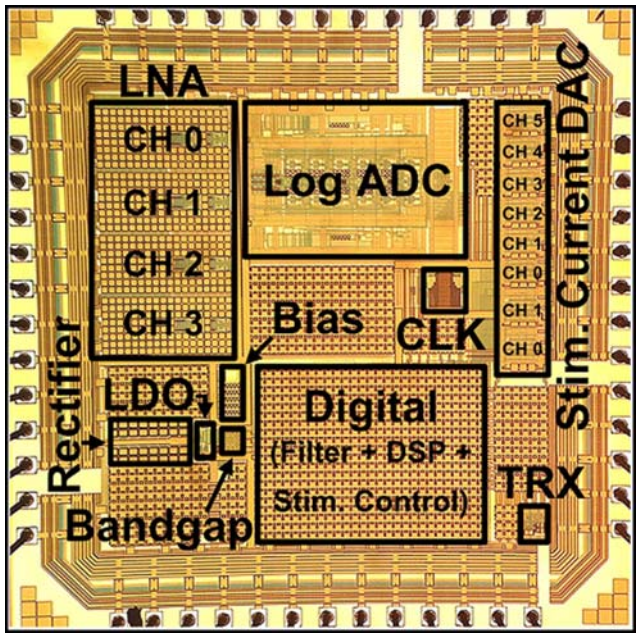

Fig. 15. Die micrograph of the prototype logarithmic closed-loop DBS system.

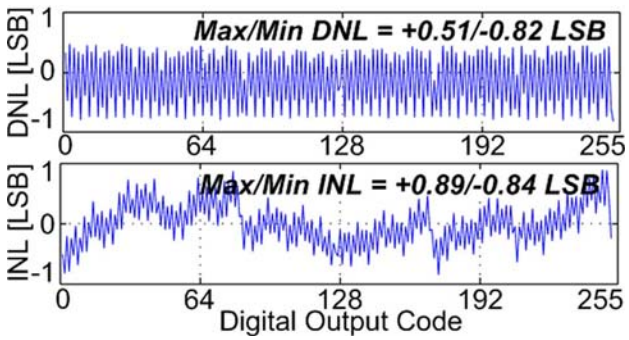

Fig. 16. Measured DNL and INL of the designed analog front-end $(4-\text{ch.LNAs}+\log-\text{ADC})$.

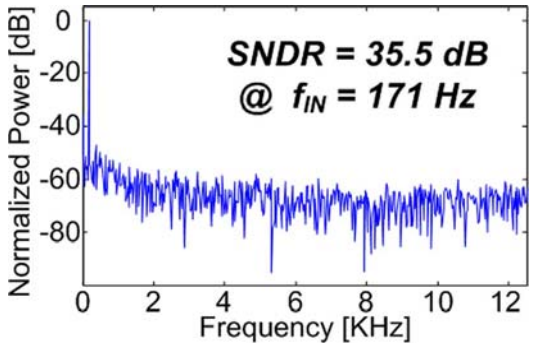

Fig. 17. Measured output spectrum of the designed analog front-end $(4-\text{ch.LNAs}+\log-\text{ADC})$.

the energy of input LFP signals. The P.I. constants and the reference value can be adjusted to further enhance the efficacy of closed-loop DBS treatment. As shown in Fig. 21, the prototype DBS system clearly demonstrates closed-loop stimulation based on LFP energy information.

Fig. 22 shows the measured output spectrum and transmitted bit stream of the backscatter transmitter. Backscatter modulation is exploited in the transmitter to minimize power consumption, achieving an energy consumption of 6.25 pJ/b.

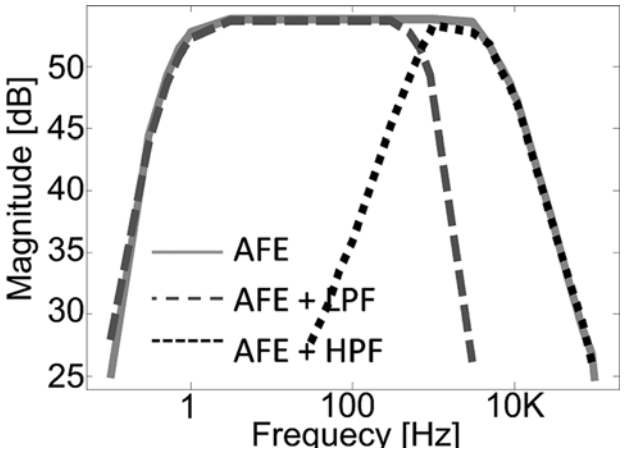

Fig. 18. Measured frequency response of the recording path (analog front-end + digital log-filters).

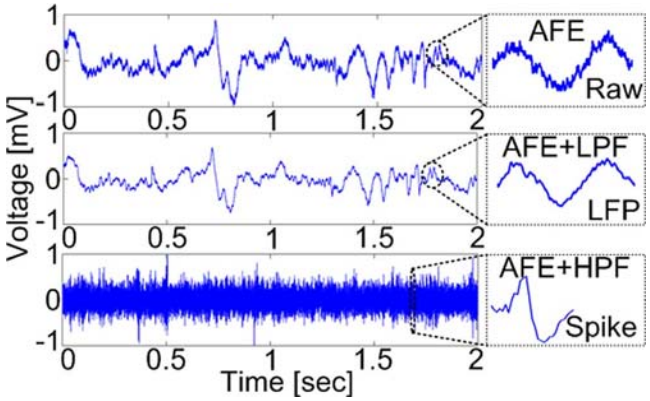

Fig. 19. Recorded transient output of the recording path (analog front-end + digital log-filters) with a pre-recorded neural signal from a rodent's brain applied as input to the system.

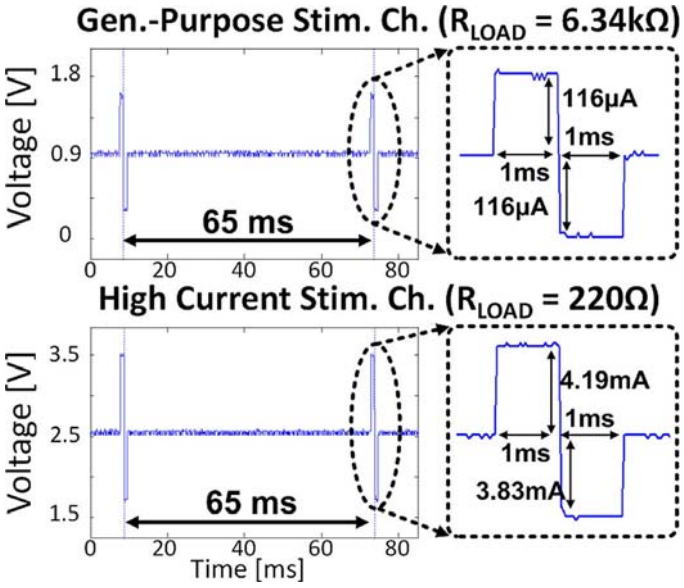

Fig. 20. Measured stimulation current waveforms of general-purpose (top) and high-current stimulation channels (bottom) with 6.23 kΩ.and 220 Ω resistor loads, respectively.

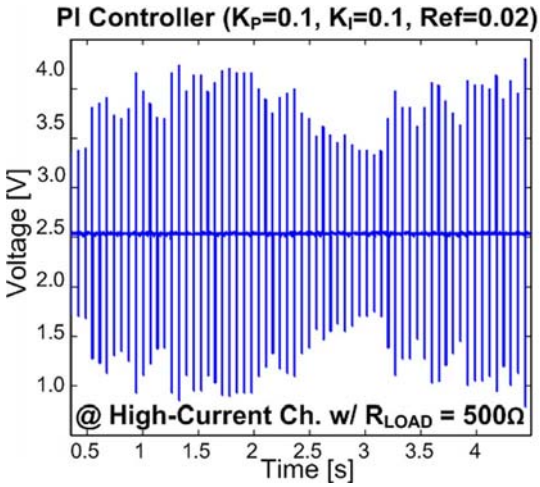

Fig. 21. Measured stimulation current waveforms of a high-current stimulation channel in closed-loop mode using LFP energy detection with a 500 Ω resistor load.

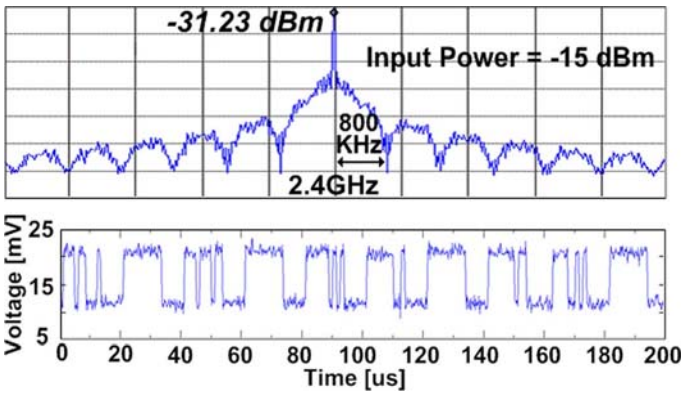

Fig. 22. Measured output spectrum of the backscatter transmitter and recovered data bit-stream from the backscatter transmitter after down-mixing with 2.4 GHz carrier.

The power consumption of each block is shown in Table IV. The measured total power consumption of the system is 468 μW. The overall system performance is summarized in Table V. Table VI compares the system performance of this work with that of other recent works.

VI. Conclusions

This work introduces the first fully-self-contained wirelessly-powered closed-loop DBS SoC. The closed-loop DBS system analyzes LFP energy information to set the optimal stimulation current amplitude. Log-domain digitization and signal processing improves energy efficiency, allowing wirelessly-powered operation. High-current stimulators facilitate optogenetic and DBS applications. A two-way wireless interface adds to the flexibility of the device.

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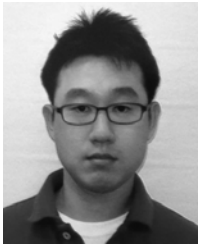

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