

A 69dB SNDR, 25MHz BW, 800MS/s Continuous-Time Bandpass $\Delta\Sigma$ ADC Using DAC Duty Cycle Control for Low Power and Reconfigurability

Hyungil Chae and Michael P. Flynn
University of Michigan, Ann Arbor, MI

Abstract

A new power-efficient, reconfigurable, 6th-order continuous-time bandpass delta-sigma modulator architecture is presented. A new duty-cycle-controlled DAC halves the number of DACs in the modulator, and also enables the center frequency to be reconfigurable. A prototype 800MS/s modulator achieves 69dB SNDR with a 25MHz bandwidth at a 200MHz IF. The center frequency can be varied from 180MHz to 220MHz. The 65nm CMOS prototype consumes 35mW and occupies a die area of 0.25mm².

Introduction

Despite recent improvements [1-3] in the power efficiency of continuous-time bandpass $\Delta\Sigma$ modulators (CTBPDSMs), CTBPDSMs still consume more power than other kinds of data converters and introduce design challenges. Furthermore, although a CTBPDSM with a reconfigurable center frequency could potentially eliminate analog blocks in the receiver chain and make the receiver more flexible [2], existing reconfiguration techniques are complicated. Another desirable characteristic is a signal transfer function (STF) with modest input signal filtering for robustness against out-of-band interferers, which would otherwise significantly decrease the dynamic range.

We introduce a new architecture that is both simple and reconfigurable, through a new duty-cycle-controlled feedback DAC scheme. A single, duty-cycle-controlled DAC replaces the conventional pair of return-to-zero (RZ) and half-clock-delayed RZ (HZ) DACs that are usually required for each resonator. This new architecture enables input signal filtering without peaking in the STF. Thanks to the duty-cycle controlled DAC, the center frequency is easily reconfigurable. Along with these new features, this CTBPDSM has the best figure-of-merit of any CTBPDSM with an active resonator.

Duty-cycle-controlled DAC

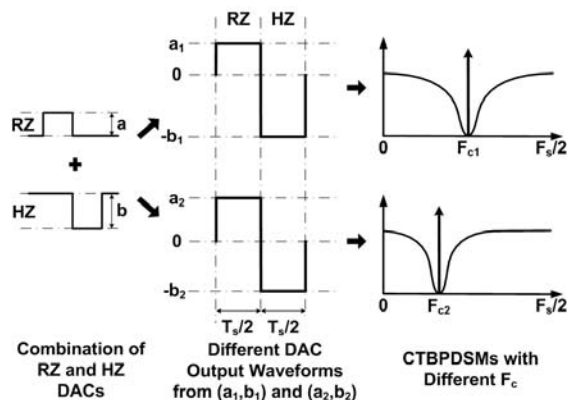


Fig. 1 Center frequency tuning by adjusting the amplitude of RZ and HZ DAC pulses.

A flexible modulator center frequency requires adjustment of both the feedback and/or feedforward coefficients, as well as modification of the resonance frequency of resonators. [4] transforms a discrete-time bandpass $\Delta\Sigma$ modulator (DTBPDSM) to a CTBPDSM with RZ and HZ DACs. Unlike

other approaches, this transformation is not limited to the condition that the center frequency F_c is $F_s/4$, and can be used for the transformation of DTBPDSMs with any F_c between DC and $F_s/2$. If the resonator is tunable then from analysis of the loop impulse response, the modulator can operate with any F_c by changing the amplitudes of the RZ and HZ pulses (Fig. 1). Different combinations of RZ and HZ DAC amplitudes (a_1, b_1) and (a_2, b_2) enable different center frequencies, F_{c1} and F_{c2} since they lead to the appropriate sampled loop impulse response required for different values of F_c . Therefore, reconfiguration of F_c can be achieved by adjusting the RZ and HZ DAC currents, but conventionally this requires both RZ and HZ DACs for each resonator.

A significant drawback with this conventional approach to frequency reconfiguration is that it requires both an RZ and an HZ feedback DAC for each resonator. This prevents the use of the new architecture in [3] that halves the number of feedback DACs. [3] eliminates one feedback DAC per resonator thereby significantly reducing power consumption, thermal noise and silicon area. However, the scheme in [3] requires a feedforward path to remove one DAC and this has the disadvantage of causing STF peaking. Furthermore, reconfiguration of F_c is not possible because the approximation made to remove another feedback DAC is only valid for $F_c = F_s/4$.

To overcome these limitations, we introduce a single variable-duty-cycle non-return-to-zero (NRZ) DAC to replace the combination of the RZ and HZ DACs, without affecting the original STF with filtering. Here adjustment of the duty cycle allows a single DAC to emulate the combination of HZ and RZ DACs in a CTBPDSM since both the pulse width and pulse amplitude convey information. Fig. 2(a) shows the waveform resulting from the combination of RZ and HZ pulses with RZ and HZ DAC amplitudes of 'a' and 'b'. The waveform of the new duty-cycle controlled DAC in Fig. 2(b) is NRZ, and has a constant amplitude 'c', and the duty cycle is no longer 50%. Thanks to the variable duty cycle, the waveform has information in the amplitude 'c' and the duty cycle ' α ', while the conventional combination of RZ and HZ DACs only has information in the amplitude of the two pulses. Therefore, the duty-cycle controlled DAC waveform of Fig. 2(b) is made equivalent to that of Fig. 2(a) in one clock period of a CTBPDSM by choosing 'c' and ' α '. It can be easily shown that the sampled loop impulse response of this duty-cycle-controlled DAC, plus resonator, in a CTBPDSM is exactly the same as that for the two DAC system. By adjusting the duty cycle, this new DAC easily facilitates a CTBPDSM with $F_c \neq F_s/4$.

The advantage of the duty-cycle-controlled DAC scheme is that it has constant amplitude and can be implemented with a single DAC. This significantly reduces the power consumption and thermal noise of the DACs, and simplifies the modulator architecture. The new DAC scheme halves the total number of DACs without any detrimental modification of the architecture (such as additional feedforward paths). In this way the

CTBPDSM needs only one DAC per resonator for any combination of feedback and feedforward paths.

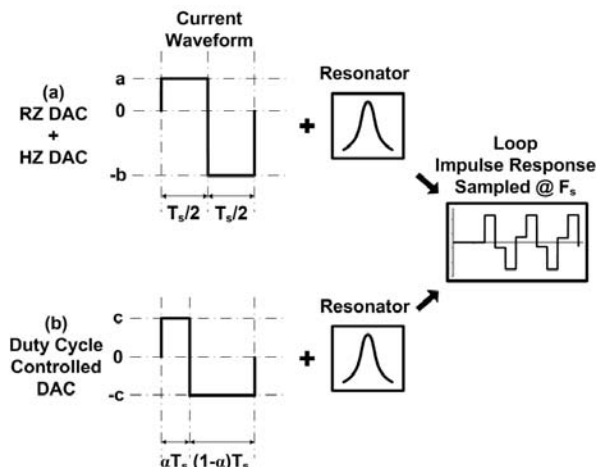


Fig. 2 A single duty-cycle-controlled DAC replaces the combination of RZ and HZ DACs to achieve the same loop impulse response with half the number of DACs

System Architecture

The prototype ADC, shown in Fig. 3, is a 6th-order modulator with 4bit quantization. There are three resonators and only two DACs. Single-opamp resonators [3] are used for low power consumption. Although the new DAC scheme does not require any feedforward path, we introduce a single feedforward path from the output of the first resonator to the input of the third resonator to relax the power and linearity requirements. Any peaking in the STF due to this path is minimized with little penalty in SNDR by adjusting the gain of the second resonator. This method significantly reduces the output swing of the first resonator and helps low power consumption. Furthermore, it does not require a summing amplifier before the quantizer. At the same time, we minimize STF peaking to below 1dB and achieve a bandpass STF.

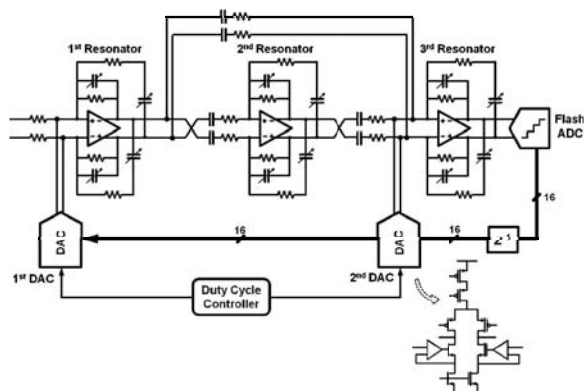


Fig. 3 System Architecture.

Measurement Results

The prototype is fabricated in 65nm CMOS, and the active area of the die is 0.25mm². Measurements show 69dB SNDR over a 25MHz bandwidth and 800MHz sampling rate when F_c is set to 200MHz (Fig. 4). The STF is also shown in Fig. 4, and the maximum peaking is less than 1dB. The 3dB bandwidth is 300MHz. The measured dynamic range and IM3 are 70dB and 73dB, respectively. The resonator and the on-chip clock-duty-cycle generator have +/-10% tuning range, and the center frequency of the prototype can be tuned from 180MHz

to 220MHz. Fig. 5 shows the operation of the prototype at a 220MHz center frequency, and indicates an SNDR of 67dB. The total power consumption including that of the clocking and bias generator is 35mW, and this corresponds to an FoM of 317fJ/conv-step. Even with addition of reconfigurability, to our knowledge this work demonstrates the best energy efficiency for any CTBPDSM using active resonators.

References

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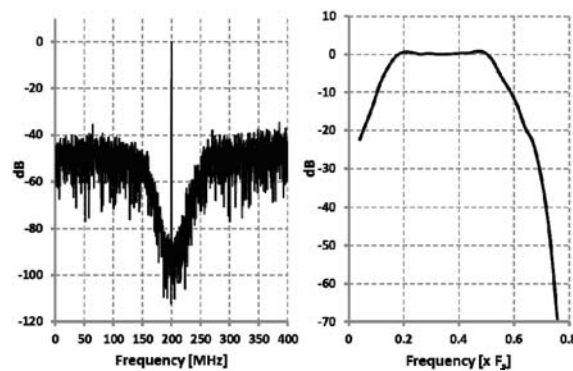


Fig. 4 Measured output power spectrum density and Signal Transfer Function (STF).

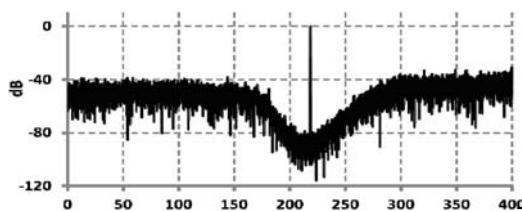


Fig. 5 Output power spectrum density with center frequency tuned to 220MHz

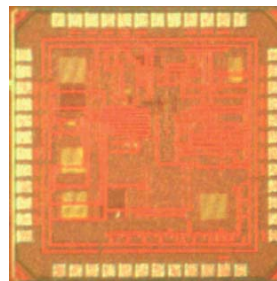


Fig. 6 Die Photo