8.2 A 12mW Low-Power Continuous-Time Bandpass ΔΣ Modulator with 58dB SNDR and 24MHz Bandwidth at 200MHz IF

Hyungil Chae[1,2], Jaehun Jeong[1], Gabriele Manganaro[2], Michael Flynn[1]

[1]University of Michigan, Ann Arbor, MI
[2]Analog Devices, Wilmington, MA

A continuous-time bandpass ΔΣ modulator (CTBPDSM) is a good solution for software-defined-radio (SDR) since it allows much flexibility in the digital back-end and also decreases the complexity of the receiver chain by combining several analog blocks into a single ADC [1]. However, conventional CTBPDSMs suffer from large power consumption and occupy large area. CTBPDSMs based on LC tanks are large, while biquad-based resonators are also large and suffer from high power consumption because two amplifiers are usually required in each resonator. The fact that there are typically twice as many feedback paths compared to a lowpass ΔΣ modulator with the same bandwidth and performance also increases power consumption, area and complexity. This paper presents a power-efficient resonator with a single amplifier and also introduces a simplified architecture utilizing return-to-zero (RZ) and half-clock-delayed return-to-zero (HZ) pulses to solve the power and complexity problems.

We introduce a single-amplifier resonator that halves the power consumption of the loop filter. Existing single-amplifier resonators [2] are either inappropriate for CTBPDSM due to their transfer function, or are not easy to integrate with a current-mode DAC. In this work, by applying positive feedback to a conventional active filter, a high-Q resonator is realized with a single amplifier, replacing the LC or biquad resonators in a conventional CTBPDSM. Figure 8.2.1 shows how the high-Q resonator is obtained from a low-Q BPF consisting of an LPF and HPF in series. While stop-band signals are filtered out, pass-band signals of a low-Q BPF resonate with help of the positive feedback path. The total Q factor of this filter can be increased to the level required for a loop filter depending on the feedback gain β. With the positive feedback, the original transfer function of the low-Q BPF, A(s) becomes A(s)' (Fig. 8.2.1). As β approaches 1, the Q factor goes to infinity and this filter has the same transfer function as that of an ideal 2nd-order resonator.

A differential-mode circuit implementation of the resonator is also shown in Fig. 8.2.1. The HPF outputs are directly fed back to inputs since positive feedback of 1 (=β) can be easily realized in the differential mode, and the resonance condition and Q factor now depend only on passive component values. The resonance condition of $R_nC_n + R_pC_p - R_nC_p = 0$ can be worked out from the transfer function of the differential circuit B(s). A solution of $C_p=2C_n$, $R_n=2R_p$ is chosen so that the filter has the best noise performance and the smallest passive area. Although the original resonator outputs are OUT+' and OUT-', the amplifier outputs OUT+ and OUT- directly feed the next block through another RC HPF formed by R_p' and C_p' for flexibility and kickback reduction. The time constant of this HPF is the same as R_pC_p, and here, C_p' smaller than C_p is used to reduce the amplifier's load without affecting the total noise performance.

Capacitor banks with 4b digital control are placed in parallel with the main capacitors for Q-factor control, and a Q factor of 20 sufficient for the target modulator performance is used in test. The main advantage of this resonator structure in a loop filter is that it consumes half the power, compared to traditional biquad resonators, but has the same noise performance. These power and area savings are significant, especially in higher-order modulators. The standalone linearity of this resonator can decrease due to the positive feedback, but this effect is negligible if a feedforward architecture is used for the modulator to reduce signal swing. A multi-stage gm-C amplifier with Miller compensation is used in the resonator, and is easily implemented with a low supply voltage. Simulations indicate that the amplifier has 73dB gain and 65° phase margin, and consumes 2mW.

Unlike a conventional biquad resonator, our resonator presents only one summing node for feedback loop paths, since it has only one virtual ground node. As with LC-resonator-based CTBPDSMs, which similarly present only one summing node, this motivates the use of a multi-path feedback design [3] for the modulator. However, the use of multiple feedback paths per resonator increases static power and adds more noise to the first resonator. In this work, a different analysis of a multi-path feedback design based on the approximation in Fig. 8.2.2 shows a way to reduce the noise as well as power consumption by putting one feedback DAC per resonator and feedforward paths.

The use of a half-width pulse enables a better approximation of a square wave to a constant value (i.e. DC) in the frequency domain. In a continuous-time system, a non-return-to-zero (NRZ) pulse has a transfer function $(1-\exp(-sT_s))/s$ for a sampling period T_s. In a lowpass system, the $\exp(-sT_s)$ term can be approximated as $1-sT_s$ because sT_s can be considered small in the frequency range of interest so that the overall transfer function is close to T_s, a constant value as required. On the other hand, this approximation is not valid at the bandpass signal frequency (e.g. at $F_s/4$) in a bandpass modulator. Instead, a half-width RZ or HZ results in an exponential term of $\exp(-sT_s/2)$ that achieves a much better approximation in a bandpass system thanks to the halved exponential term.

To explain how the number of feedback paths is halved, Fig. 8.2.2 shows a 4th-order multi-path feedback design with feedforward paths added for power reduction and NTF control. A key observation in Fig. 8.2.2 is that one feedback per resonator is enough to control the overall NTF of this architecture because the coefficients always appear in pairs of (k_1, k_2) and (k_3, k_4). HZ DAC is assigned to the first feedback and RZ to the second to compensate the phase shift of signals caused by one clock delay after the quantizer relieving the excess loop delay effect. The feedforward path from the input to the quantizer decreases signal swing through the analog signal path, which is helpful for low power consumption and for the linearity of resonators. As a result, this modulator architecture is advantageous in terms of power, complexity, and silicon area compared to existing architectures.

An oversampling ratio of 16.7 is used to achieve a reasonable bandwidth for SDR, and a 4th-order NTF with 9-level quantization sufficient for 11b resolution is applied. Figure 8.2.3 shows the full circuit implementation. The quantizer is a flash ADC and each comparator is offset-calibrated by trimming currents [4]. To compensate for clock skew between the DAC and quantizer, the clock to the quantizer is controlled by a 3b digitally controlled delay chain. Both current-steering DACs consist of 8 triple-cascode current sources, and the first stage DAC has large area current sources for excellent matching. A summing amplifier is used to sum two feedforward signals and the output of the second resonator.

The prototype is fabricated in 65nm CMOS and occupies a die area of 0.2mm^2. Figure 8.2.4 shows the measured power-spectrum density of this modulator output. The device has a measured SNDR of 58dB for a -3.9dBFS input while operating with 1.25V supply. A two-tone test indicates 65dB IMD, and the measured dynamic range is 60dB (Fig. 8.2.5). The total power consumption including that of the clock generator is 12mW. State-of-art CTBPDSMs are compared in Fig. 8.2.6 and this modulator has an FoM of 385fJ/step, the lowest in the table.

References:

[1] A. Pulincherry, M. Hufford, E. Naviasky, and U. Moon, "Continuous-Time, Frequency Translating, Bandpass Delta-Sigma Modulator," *IEEE Proc. ISCAS*, vol. 1, pp. 1013-1016, May 2003.
[2] K. Matsukawa, *et al.*, "A 5th-order Delta-Sigma Modulator with Single-Opamp Resonator," *Symp. VLSI Circuits*, pp. 68-69, Jun. 2009.
[3] O. Shoaei and W.M. Snelgrove, "A multi-feedback design for LC bandpass Delta-Sigma modulators," *IEEE Proc. ISCAS*, vol. 1, pp. 171-174, Apr. 1995.
[4] G. Mitteregger, *et al.*, "A 20-mW 640-MHz CMOS Continuous-Time ΣΔ ADC With 20-MHz Signal Bandwidth 80-dB Dynamic Range and 12-bit ENOB," *IEEE J. Solid-State Circuits*, vol. 41, no. 12, Dec. 2006.

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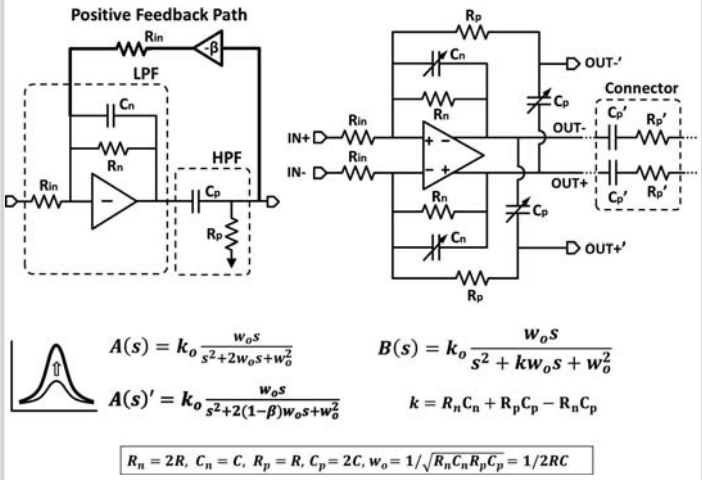

Figure 8.2.1: Single-amp resonator structure with positive feedback and its differential circuit implementation.

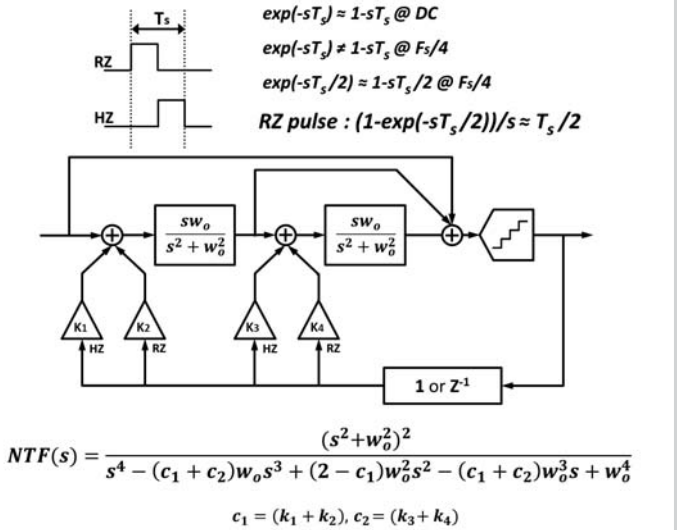

Figure 8.2.2: NTF analysis of 4th-order architecture with RZ and HZ pulse feedbacks.

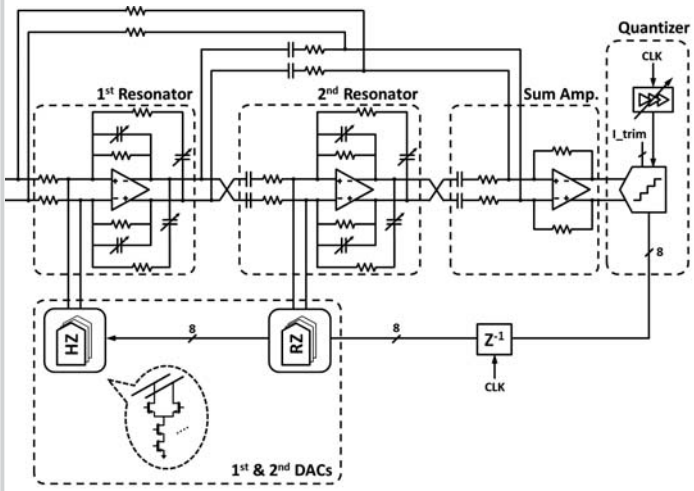

Figure 8.2.3: Circuit implementation of the modulator.

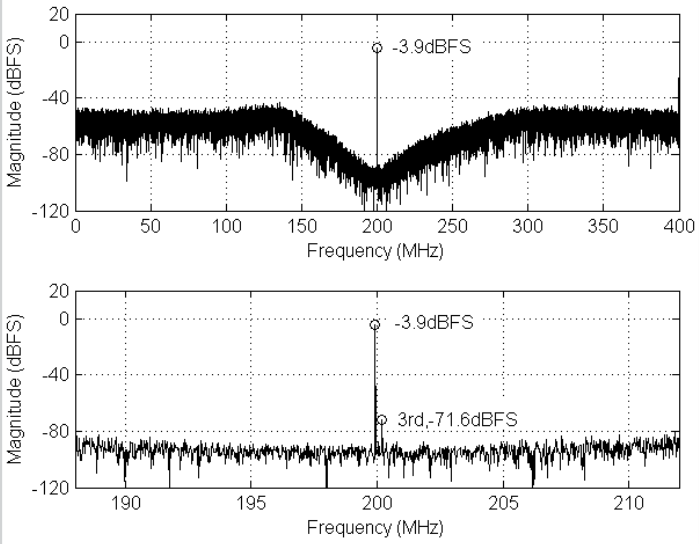

Figure 8.2.4: Output spectrum density with -3.9dBFS input at 199.9MHz.

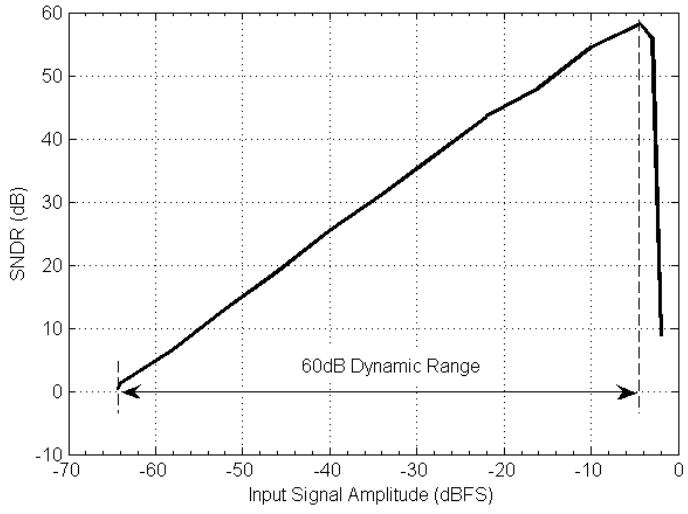

Figure 8.2.5: Measured dynamic range with 200MHz input.

Author	Schreier	Thandri	Chalvatzis	Ryckaert	Lu	This work
Publication	JSSC 2006	JSSC 2007	JSSC 2007	JSSC 2009	JSSC 2010	
Order	4th	4th	4th	6th	6th	4th
Resonator	active-RC	LC	LC	LC	active-RC	new RC
DR [dB]	90	65	53		70	60
F_s [MHz]	264	3800	40000	3000	800	800
F_c [MHz]	44	950	2000	2400	200	200
BW [MHz]	8.5	0.2/1	60/120	60	10	24
SNDR [dB]			55/52	40	68.4	58
SNR [dB]	77	63/59				
Power [mW]	375	75	1600	40	160	12
Area [mm²]	2.5	1.08	2.4	0.8	2.5	0.2
Process	0.18 CMOS	0.25 BiCMOS	0.13 BiCMOS	0.09 CMOS	0.18 CMOS	0.065 CMOS
FoM [pJ/step]	3.81	162/51	29/20	4.08	3.72	0.385

* $FoM = Power/(2 \cdot BW \cdot 2^{ENOB}),\ ENOB = (SNDR - 1.76)/6.02$

Figure 8.2.6: Comparison chart.

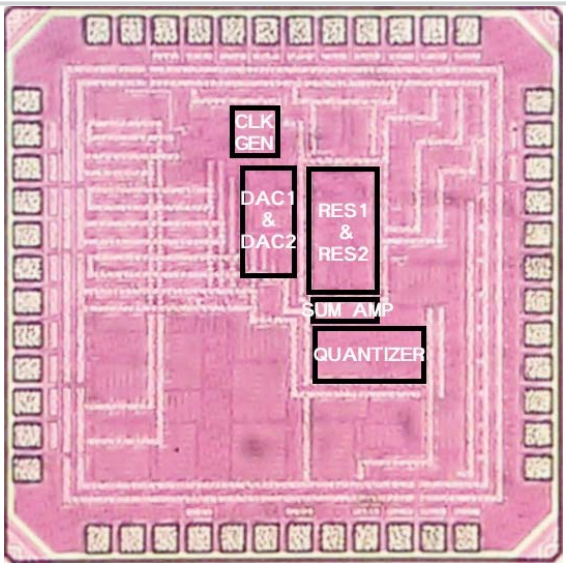

Figure 8.2.7: Die photograph. The active area is 0.2mm^2.

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