A 12 mW Low Power Continuous-Time Bandpass ΔΣ Modulator With 58 dB SNDR and 24 MHz Bandwidth at 200 MHz IF

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Abstract—A 800 MS/s low power fourth-order continuous-time bandpass ΔΣ modulator (CTBPDSM) with 24 MHz bandwidth at a 200 MHz IF uses a novel power-efficient resonator with a single amplifier as a loopfilter. The single op-amp resonator employs positive feedback to increase the Q-factor. A new fourth-order architecture is introduced for system simplicity and power efficiency. Reducing the number of feedback DACs lowers the power consumption and simplifies the modulator structure. A prototype ADC achieves 58 dB SNDR, 60 dB DR and 65 dB IM3, with a total power consumption of 12 mW. The total die area in 65 nm CMOS is 0.2 mm².

Index Terms—ADC, bandpass, continuous-time, delta-sigma, low power, resonator, single op-amp.

I. INTRODUCTION

THE super-heterodyne architecture, shown in Fig. 1, is one of the most popular receiver architectures. Although the super-heterodyne architecture offers good frequency selectivity and sensitivity [1], it makes the receiver chain complicated and difficult to reconfigure. Software defined radio (SDR) is attractive for future receivers because it allows one receiver to support multiple standards [2], [3]. As shown in Fig. 2, SDR eliminates many of the blocks in the super-heterodyne architecture by digitizing a wide-band signal without first down-converting to the baseband. In this way, digital signal processing (DSP) takes care of filtering, channel selection and mixing. In most cases, DSP costs less in terms of area and power because it is not affected by thermal noise and mismatch.

The design of an ADC with a wide bandwidth, high resolution, and reasonable power consumption is a bottleneck in the realization of SDR [4]. Continuous-time bandpass ΔΣ modulators (CTBPDSM) are very attractive for SDR because they can directly digitize RF or IF signals. Furthermore, in some architectures the frequency band can be tuned [5], [6]. Another

advantage is that IF digitization requires fewer circuit blocks since separate I/Q path are no longer required. Digital down-conversion of the modulator digital output eliminates the issues (e.g., limited image rejection) associated with path mismatch in quadrature baseband digitization schemes. Furthermore, IF digitization mitigates flicker noise, and the continuous-time ΔΣ modulators tolerate aliasing signals.

Although noise-shaping enables high resolution, the power consumption of existing schemes is too high. Continuous-time operation helps to achieve good power efficiency and recent work on the CTBPDSM has made significant progress in this regard [7], [8]. Nevertheless, state-of-the-art CTBPDSMs still have worse energy efficiency compared to other types of ADCs and this limits the use of CTBPDSM ADCs in practical receivers. On the other hand, lowpass continuous-time ΔΣ modulators (CTLPDSMs) are dominant in many applications due to their performance, simplicity and power efficiency. Fig. 3 compares the power efficiency of recently published lowpass and bandpass ΔΣ modulators. The Walden [9] figure-of-merit (FoM) for ADCs assumes digitization from 0 frequency to $F_s/2$ and does not consider that, for equal bandwidth, a bandpass ADC digitizes signals at much higher frequency than a classic ADC. That said, there is more than 2x difference between the best FoMs for CTLPDSMs and CTBPDSMs.

The filter in a CTBPDSM can be implemented with an LC tank resonator or a biquadratic resonator (Fig. 4). Regardless of the filter type, a conventional CTBPDSM requires two DACs per resonator. This increases both the silicon area and the overall power consumption. In contrast there is one feedback DAC per integrator in a CTLPDSM. An LC tank resonator can be used as the filter in a CTBPDSM [10]–[12] (Fig. 4(a)). Two kinds of DACs with different phases are used in the feedback loop to compensate for frequency modulation due to the zero-order-hold of the DAC. These DACs are a return-to-zero (RZ) DAC and a half-clock-delayed return-to-zero (HZ) DAC. The main advantages of the LC resonator architecture are low power, and low noise thanks to the high quality factor of the resonator. However, the die area tends to be large due to the size of the integrated inductors, and inductors do not get smaller as technology scales.

A biquadratic resonator can be used instead of LC tank resonators [13], [14]. A biquadratic resonator consists of two integrators in a loop as shown in Fig. 4(b). A biquadratic res-
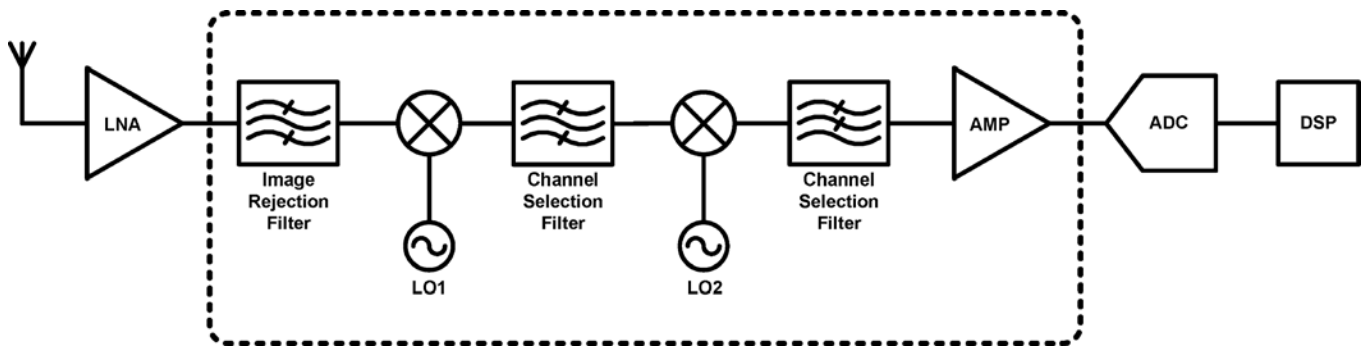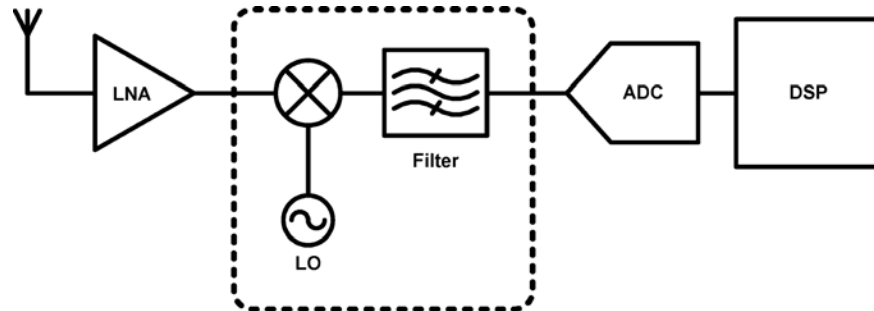
Fig. 1. Super-heterodyne receiver.

Fig. 2. Software-defined-radio architecture.
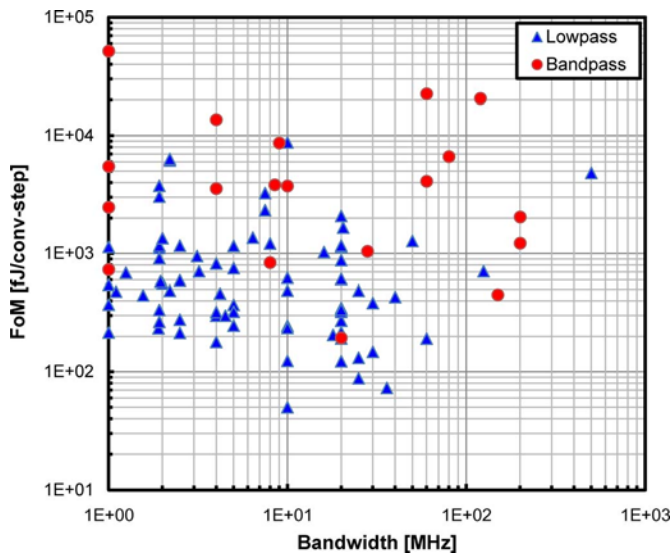

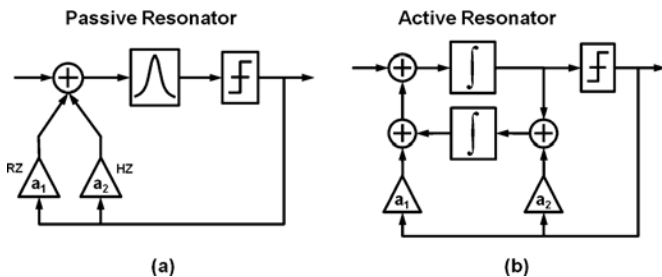Fig. 3. Comparison of figure-of-merits of CTLPDSMs and CTBPDSMs.

Fig. 4. (a) A passive and (b) an active resonator in a second-order modulator.

onator provides two summing nodes, which allows a different CTBPDSM architecture to that with LC tank resonators. Two feedback DACs per resonator are connected to each summing node, and these are both non-return-to-zero (NRZ) DACs. The use of an active resonator avoids the need for large inductors, but each integrator requires an op-amp, and these integrators consume lot of power and contribute thermal noise to the modulator.

In this work we replace the conventional resonators in a CTBPDSM with a single op-amp resonator to achieve lower power consumption and smaller silicon area [15]. The use of only one op-amp reduces the noise contribution to the loop and this also means a lower power consumption for a given noise requirement. There are many ways to implement single op-amp resonators [16], and the recently published single op-amp resonators shown in Fig. 5 improve the simplicity and flexibility [17], [18]. However these are not suitable for CTBPDSMs because they do not have the same transfer function as an ideal resonator and do not present summing nodes for the feedback DACs needed in a bandpass modulator. Also, the resonator in Fig. 5(b) has too many passive components. Furthermore, these resonators have many passive components that contribute to the total thermal noise. Therefore, we introduce a new single op-amp resonator with an appropriate transfer function and summing nodes, as well as fewer passive components. A new fourth-order architecture halves the number of feedback DACs to further reduce power consumption.

The goal of this research is to reduce the power consumption of CTBPDSMs by introducing a new architecture and a new single op-amp resonator. Section II introduces a new CTBPDSM architecture that minimizes the number of components in the feedback loop. This architecture lowers the total power consumption and the silicon area. In Sections III and IV, the circuitry for each block, including the new single op-amp
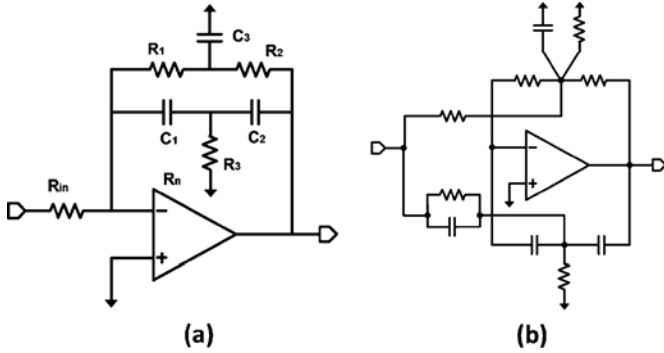
Fig. 5. (a), (b) Single op-amp resonators [17], [18].

Fig. 6. System block diagram.
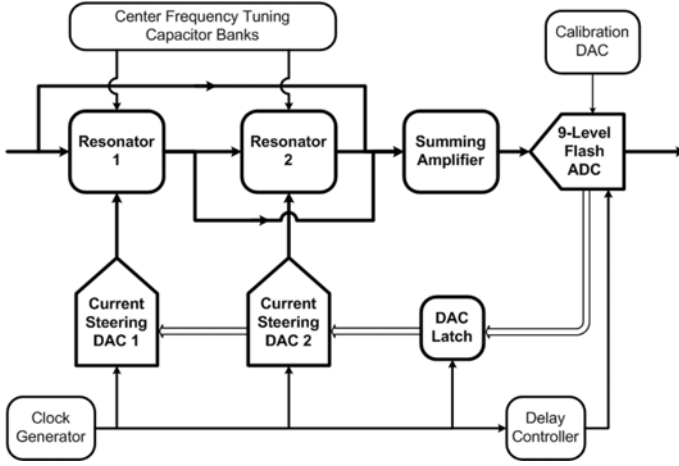

Fig. 7. Conventional fourth-order CTBPDSM with LC-tank resonators [10].

resonator, is explained. Section V presents the evaluation results of the CTBPDSM prototype.

II. SYSTEM ARCHITECTURE

A. Architecture Overview

The prototype CTBPDSM has a fourth-order architecture with 3 bit quantization as shown in Fig. 6. In the new architecture, two resonators and only two DACs are used to achieve fourth-order bandpass noise shaping. Both resonators are single op-amp resonators. Capacitor banks tune both the resonant frequencies and the quality factor. As discussed in Section II.B the modulator has two DACs instead of the four DACs needed in a conventional fourth-order bandpass architecture. To compensate the clock timing difference between the DACs and the flash ADC, a clock delay controller is used to clock the flash ADC.

The sampling frequency of the modulator is 800 MHz, and the center frequency is 200 MHz. With a 24 MHz bandwidth this gives an oversampling ratio (OSR) of 16.7. Based on this OSR, and ignoring noise, an ideal SNDR of 70 dB is achieved with a fourth-order architecture with 3 bit quantization or with a sixth-order modulator with 2 bit quantization [19]. Both alternatives offer reasonable power consumption and stability, however the fourth-order architecture is adopted for this modulator because it achieves better power consumption.
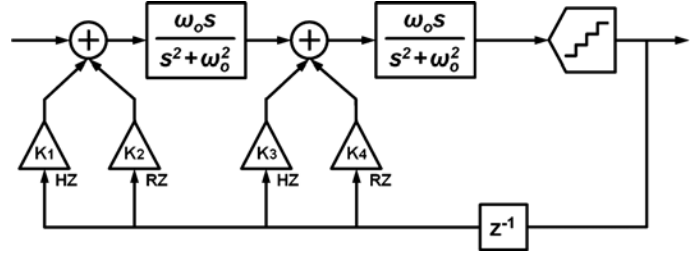
B. Elimination of Current-Mode Feedback DACs

As discussed in Section III, we use a single op-amp resonator in this CTBPDSM. This single op-amp resonator presents only one summing node for the feedback loop paths because it has one virtual ground node. As with LC resonators [10] and other CTBPDSMs that similarly present only one summing node which cannot use two NRZ DACs per resonator, this motivates the use of a multi-path feedback design for the modulator, shown in Fig. 7, that perfectly transforms a DTBPDSM into a CTBPDSM. However, the use of multiple feedback paths per resonator increases static power and adds more noise to the first resonator.

We can replace feedback DACs by adding feedforward paths to achieve the same overall loop transfer function. In this way, a feedforward path from the first resonator output to the quantizer allows us to remove two feedback DACs, K_{3-4} [19], in the fourth-order CTBPDSM of Fig. 7. Although, these two second-resonator DACs are removed, a disadvantage is that two DACs at the front of the modulator, which add noise to the first resonator input and contribute a significant portion of total modulator input referred noise, remain. Instead, in this work, a new analysis of a multi-path feedback design allows the use of only one feedback DAC for both resonators. In this way, the removal of one of the first-resonator DACs leads to reduced noise and power consumption.

Even if one of the feedback coefficients varies slightly due to some analog imperfections, a small change in the other coefficients can compensate for this and maintain stability and performance. A classical discrete-time to continuous-time pole-zero mapping to synthesize a continuous-time transfer function is not straightforward because of the delay block between the quantizer and the feedback DACs and the excess loop delay effect. The use of ideal modulator coefficients does not lead to optimal performance in a real system and the final pole-zero placement needs to be adjusted after the transformation. Imperfections, including the finite quality factor of the resonators, make further adjustment necessary. However, this characteristic also provides the possibility for some flexibility in the modulator coefficients.

We first consider the elimination of one of the two DACs, K_1 and K_2, connected to the first resonator. When the DAC coefficients are calculated as in [10] and optimized for 3 bit quantization (Fig. 7), K_2 is much smaller than K_1. The removal of K_2 does not lead to instability, but it does cause some peaking in the noise transfer function (NTF) and degrades the SNDR. However, as the original value of K_2 is small, and K_1, K_{3-4}
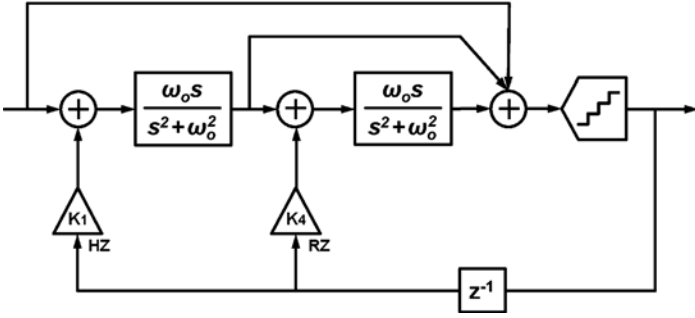
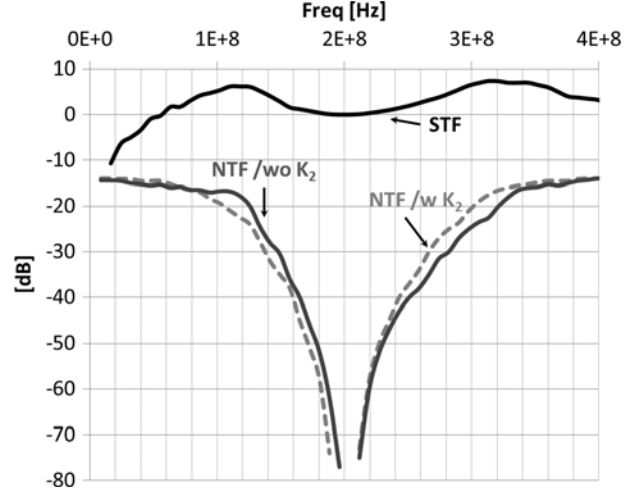Fig. 8. New fourth-order CTBPDSM with a reduced number of DACs.

Fig. 9. Noise transfer function (NTF) and signal transfer function (STF) of this modulator. Fourth-order modulation, with 3 bit quantization, and OSR of 16.7 provide 70 dB SNR. The symmetry is slightly affected by the removal of K_2.

can be tuned to compensate for the nulling of K_2. Appropriate tuning of K_1, K_{3-4} removes the NTF peaking and provides essentially the same noise shaping as the original value of K_2. The only effect caused by the removal of K_2 is a slight asymmetry of the overall power spectral density centered at the quarter of the sampling frequency. As shown in Fig. 9, zeroing K_2 makes the slopes of the NTF on the left and right side of the center frequency slightly different. However this asymmetry does not affect the noise shaping within the passband and the in-band performance, including the maximum SNDR, remains the same. The key point is that $K_2 < K_1$ allows the removal of K_2. On the other hand, removing K_1 instead of K_2 is difficult since in this case the sensitivity of the coefficients introduces instability and performance degradation since significant change in the other coefficients is required to null the large K_1.

On the other hand, the coefficients, K_3 or K_4, of the DACs feeding the second resonator cannot be nulled once K_2 is zeroed, because two other coefficients, K_1 and one of K_3 or K_4, have to be tuned to compensate, and this leads to a large variation in the coefficients and ultimately to a significant performance degradation. Instead, we add a feedforward path to remove feedback DAC, K_3. This feedforward path from the first resonator output to the quantizer has unity gain, and provides the same overall feedback as the HZ feedback DAC, K_3 and the second resonator because the new path consisting of the first resonator and the feedforward path also contains one HZ DAC and one resonator. Fig. 8 shows the new architecture after the modifications. This new architecture is valid for any resonator with the same transfer function.

This new architecture has a feedforward path from the input to the quantizer, and the gain is 0.7. Together with the other feedforward path, this feedforward path decreases the signal swing through the analog signal path by 60% which helps lower power consumption and relaxes the linearity requirement of resonators. As a result, this modulator architecture is advantageous in terms of power, complexity, and silicon area compared to existing architectures. The signal transfer function (STF) barely differs from the conventional one with feedforward paths, and there exists some peaking as shown in Fig. 9.

C. Comparison of the Inband NTFs of a Conventional CTBPDSM and the New CTBPDSM

Next we compare the NTF of a conventional CTBPDSM [10] with that of the new CTBPDSM, We begin by considering the advantages of a half-width pulse DAC compared to an NRZ

DAC. Due to the nonlinearity of the DACs, it is difficult to model the NTF, and therefore we make an approximation of the DAC transfer function. We focus on the NTF around the center frequency. Traditionally, in a z-domain representation of the modulator an NRZ DAC is represented by a constant coefficient.

In a continuous-time system, an NRZ pulse with a sampling period of T_s has a transfer function of:

$$(1 - \exp(-sT_s))/s \qquad (1)$$

At low frequencies, for a high oversampling ratio, sT_s is very small in the frequency range of interest so the exponential term can be approximated as:

$$\exp(-sT_s) \approx 1 - sT_s \qquad (2)$$

Hence (1) is close to T_s, leading to a constant value as required. On the other hand, this approximation is not accurate for the passband of a bandpass modulator (i.e., at $F_s/4$ in this work).

On the other hand, a half-width RZ or HZ pulse represented by:

$$(1 - \exp(-sT_s/2))/s \qquad (3)$$

gives a much better approximation to a constant value within the passband of a bandpass system thanks to the halved exponential term of $\exp(-sT_s/2)$ since the approximation of $\exp(x)$ to polynomial gets more accurate as x gets smaller. Using a half width pulse reduces the error in the approximation from 18% to 4%.

Equation (4) is the NTF of the fourth-order multi-path feedback design shown in Fig. 7. We get this NTF around the center frequency by assuming that the DAC coefficients are constants, as discussed above.

$$\mathrm{NTF}(s) = \frac{\left(s^2 + \omega_o^2\right)^2}{s^4 - c_2\omega_o s^3 + (2 - c_1)\omega_o^2 s^2 - c_2\omega_o^3 s + \omega_o^4} \qquad (4)$$

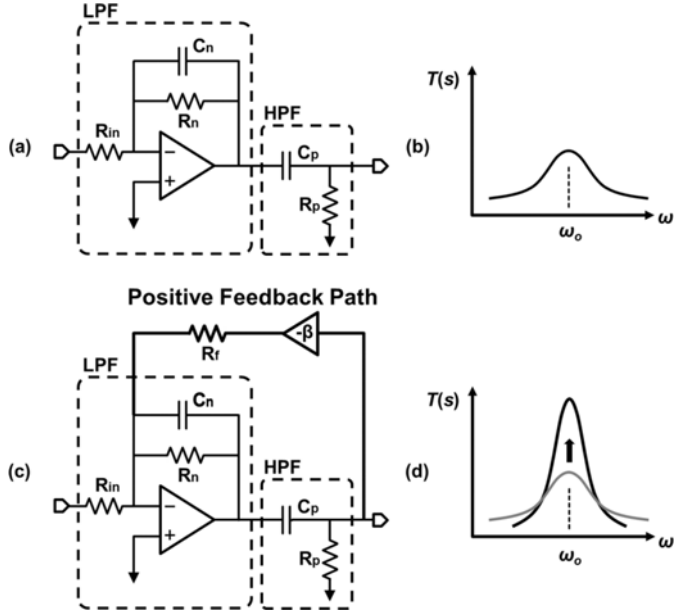$$\text{where } c_1 = (k_1 + k_2), \quad c_2 = (k_3 + k_4) \qquad (5)$$

Fig. 10. (a), (b) Bandpass filter with low Q-factor and frequency response. (c), (d) Q-factor boosting with the positive feedback.

Fig. 11. Differential-mode implementation of single op-amp.

Equation (6) is the NTF of the new architecture in Fig. 8 with the same approximation of the DAC coefficients to constants. ($K_2 = 0$, and K_3 is replaced by a feedforward path.)

$$\text{NTF}(s) =$$
$$\frac{\left(s^2 + \omega_o^2\right)^2}{s^4 - (k_1 + k_4)\omega_o s^3 + (2 - k_1)\omega_o^2 s^2 - (k_1 + k_4)\omega_o^3 s + \omega_o^4} \tag{6}$$

A key observation is that these two NTFs indicate the same noise shaping around the center frequency ω_o if the coefficients are properly chosen. In this way the new architecture can achieve the same SNDR as a conventional CTBPDSM even though the number of DACs is reduced.

III. SINGLE OP-AMP RESONATOR

A. Positive Feedback

We apply positive feedback to a conventional active filter, to realize a high quality-factor resonator with a single amplifier. This is similar to how positive feedback increases the quality-factor in voltage-controlled oscillators [20]. We begin with a conventional low-quality-factor single-amplifier bandpass filter (BPF) consisting of a lowpass filter (LPF) and a passive high-pass filter (HPF) in series, as shown in Fig. 10(a). The transfer function of this BPF is:

$$\text{T}(s) = k_o \frac{\omega_o s}{s^2 + 2\omega_o s + \omega_o} \tag{7}$$
$$\text{where } \omega_o = 1/R_p C_p R_n C_n \tag{8}$$

The first-order term in the denominator decides the quality factor, which is only 0.5 for this BPF as in Fig. 10(b) however we need a quality factor of ~20 to achieve the target SNDR. To enhance the quality factor we add a positive feedback path
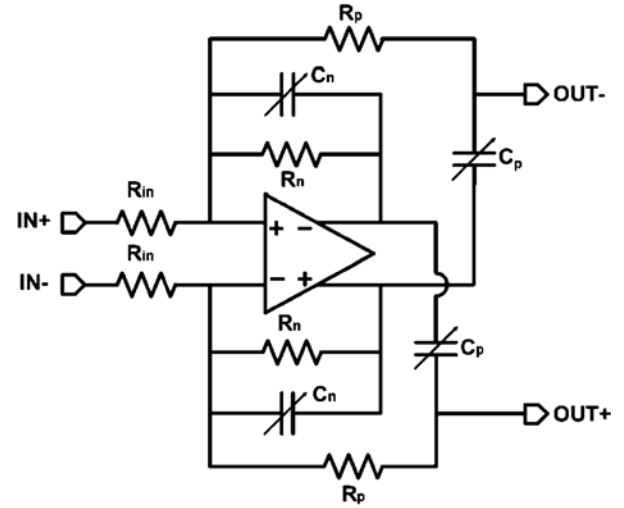
(Fig. 10(c)) to the BPF. This positive feedback path boosts the filtered output from the low quality-factor BPF around ω_o, therefore it resonates around the resonant frequency ω_o and suppresses the out-of-band signals. The positive feedback path results in the transfer function:

$$\text{T}(s) = k_o \frac{\omega_o s}{s^2 + 2 \cdot (1 - \beta) \cdot \omega_o s + \omega_o} \tag{9}$$

The quality factor of this filter can be increased to the level required for this modulator by choosing the appropriate value of the feedback gain β in Fig. 10(d). As β approaches 1, the first-order term in the denominator approaches zero and the quality factor goes to infinity making this filter have the same transfer function as that of an ideal second-order resonator. However, this requires positive feedback of 1 ($= \beta$) and an additional resistor, R_f.

The HPF is merged into this positive feedback path to avoid the need for extra components. A gain of -1 can be easily realized in the differential mode. Furthermore R_f can replace R_p because R_p connects the resonator output and the ground, while R_f is between the resonator output and virtual ground node.

A differential implementation of the resonator circuit is shown in Fig. 11. The feedback gain is set to -1, and the resonance condition and quality factor now depend only on passive component values. The transfer function of this circuit is expressed as:

$$\text{T}(s) = k_o' \frac{\omega_o s}{s^2 + 2 \cdot k \cdot \omega_o s + \omega_o} \tag{10}$$
$$\text{where } k = R_n C_n + R_p C_p - R_n C_p \tag{11}$$
$$\omega_o = 1/\sqrt{R_n R_p C_n C_p} \tag{12}$$

The resonance condition of the differential circuit is $k = 0$ from (10). There are innumerable solutions for $k = 0$, and the solution $C_p = 2C_n$, $R_n = 2R_p$ is chosen so that the thermal noise and the power consumption are optimally balanced while the resonant frequency is fixed. A ratio other than 2 makes one resistor too small and increases the power consumption while only slightly improving the noise.

An advantage of this new resonator is that it consumes 20% less power for the same noise performance compared to the traditional biquadratic resonator, which has two amplifiers. The standalone linearity of this type of resonator might be inferior to that of a more traditional circuit with negative feedback because negative feedback improves the linearity, however this is significantly mitigated when the resonator is used in a modulator with a feedforward architecture since feedforward reduces the swing where the nonlinearity occurs.

B. Center Frequency and Quality Factor Tuning

Both process variation and the mismatch of the passive components change the resonant frequency. The resonant frequency of the resonators determines the center frequency of the CTBPDSM, so calibration of passive components is required to get an exact center frequency. Calibration of the capacitors, C_p and C_n, in the positive and negative feedback loops in Fig. 11 enables calibration of both the center frequency and quality factor. Calibrating only capacitors is enough to correctly set the center frequency. Digitally controlled capacitor banks are placed in parallel with the main capacitors in Fig. 11 [21], and the modulator performance does not decrease from the capacitance change with the help of the careful design of the amplifier and switches. The quality factor of the resonator is also related to the capacitances since these decide the first-order coefficient of the denominator in (10). Fine-tuning of the capacitance is required to have good control of the quality factor and 4 bit capacitor banks are used for each capacitor.

The center frequency has to be accurate while the quality factor just needs to be above a certain threshold. Therefore the center frequency is calibrated first with 4 bit resolution (192–208 MHz, LSB = 1 MHz, $C_{STEP} = 0.5\%$), and then the quality factor is adjusted by adjusting the two capacitors C_p and C_n while maintaining the center frequency. Simulations show that the modulator performance starts to degrade by more than 1 dB in simulation if the quality factor is below 15 as quantization noise is not well filtered with a lower Q, so for this reason a Q of 20 is used to provide some margin [19].

C. Resonator Output Node

An alternative configuration for the resonator outputs gives more flexibility and reduces kickback compared to the original resonator outputs, $OUT+$ and $OUT-$, in Fig. 11. When the resonator in Fig. 11 feeds a block with resistive inputs, the time constant of the feedback paths changes and this also changes the resonant frequency and the quality factor. In Fig. 12 the amplifier outputs $OUT'+$ and $OUT'-$ directly feed the next block through another RC HPF formed by R'_p and C'_p. This HPF does not affect the feedback network around the amplifier and enables the connection to any blocks with resistive inputs in CTBPDSMs. The time constant of this HPF is the same as R_pC_p. This helps reduce kickback and improve flexibility. In the original configuration, kickback from other blocks is injected to the inputs through the resistor R_p, but the new configuration suppresses this because any kickback has to pass through the HPF. An advantage is that here, R'_p is bigger than R_p to
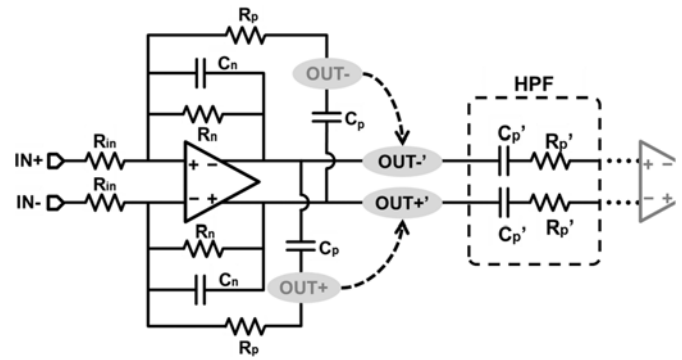

Fig. 12. Alternative resonator outputs.

reduce the amplifier's load without affecting the total noise performance. Furthermore, these capacitors are not calibrated since they barely change the resonance characteristic of the feedback loops.

D. Op-Amp

The resonator needs a high-gain op-amp to achieve a high quality factor and a small error in the resonant frequency. However, it is difficult to achieve the required high gain by cascoding because the supply voltage is low in advanced CMOS processes. A multi-stage amplifier is a good alternative for continuous-time modulators because it provides both high gain and wide bandwidth [8], [22]. Cascading of individual low gain amplifiers can provide high overall gain and also achieve a sufficient voltage swing even with a low supply voltage. As shown in Fig. 13, there are two paths in parallel; one is a high-gain, narrow-bandwidth amplification path with four amplifying stages (slow path) while the other is a low-gain, wide-bandwidth path, consisting of a single stage (fast path). The fast path provides the wide bandwidth of the op-amp. At high frequencies, the fast path, which has a much higher bandwidth than the slow path, dominates because the gain of the slow path falls off at lower frequency. Furthermore, the fast path also ensures stability because the phase of the fast path dominates the total phase response at high frequency. In the multi-stage amplifier described here, each stage is a single common-source amplifier with a current source as the load (Fig. 14(a)). Even when the circuit is implemented in a differential manner, there is still a signal headroom of more than half the supply voltage, for a 1.25 V supply. The amplifier in the fast path is also a single common-source amplifier for fast operation.

With the 65 nm CMOS process used for the prototype, a stage gain 15–20 dB leads to a good balance between the speed and the gain. In total, four stages are used to provide enough gain, and the fourth amplifier stage sums the fast path and the slow paths. As shown in Fig. 14(b), a push-pull structure enables the summing of two paths. Nested Miller-compensation is used to achieve good phase margin [23]. The simulated overall gain and phase response of this amplifier with load are shown in Fig. 15. The DC gain is 73 dB and the phase margin is 65 degrees. The gain at 200 MHz is 30 dB, and the total power consumption is 2 mW. The target gain-bandwidth product is 34 dB at 200 MHz, and the smaller gain causes some nonlinearity.
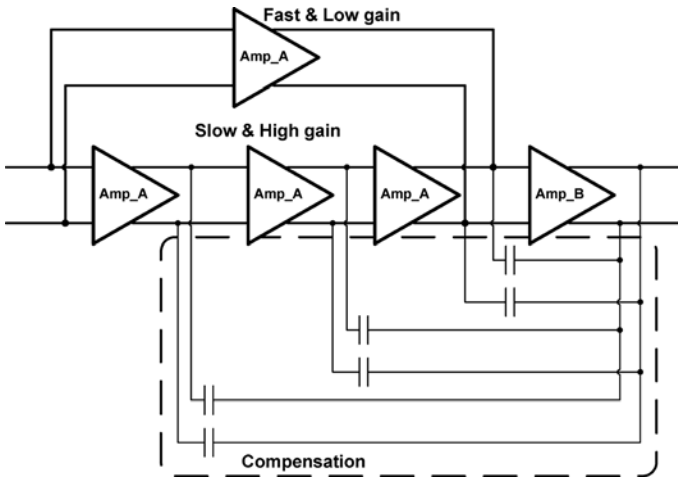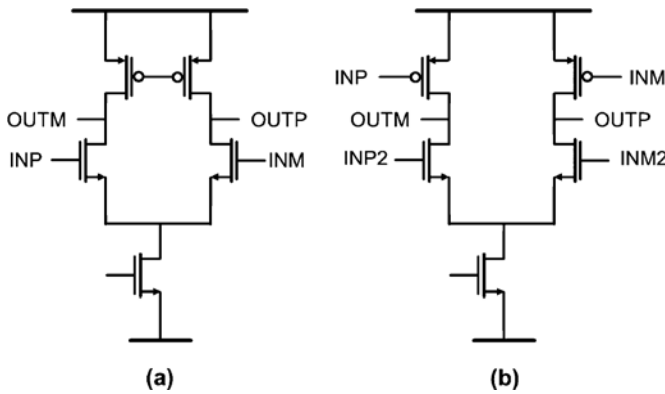
Fig. 13. Multi-stage amplifier.

Fig. 14. (a) Single stage of the amplifier (b) Last stage of the amplifier for summing (IN = fast path input, IN2 = slow path input).
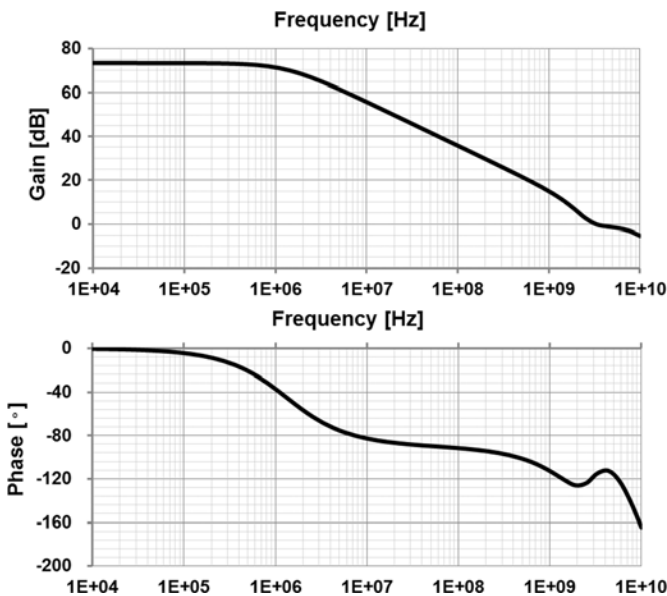

Fig. 15. Gain and phase response of the amplifier.

IV. Implementation of Other Blocks

A. DAC

A current steering DAC in Fig. 16 is used to achieve fast switching and is designed to have lower thermal noise than the input resistors. A triple-cascode structure isolates the current source at the bottom from the switches, and provides higher output impedance. By increasing the gate overdrive voltage of the current source to reduce g_m, the thermal noise is reduced.

Device size is also important for the linearity. Mismatch between the current sources modulates the output current and introduces nonlinearity regardless of the resonator performance. Although dynamic element matching (DEM) can cancel this nonlinearity by shuffling the mismatch, DEM is complex and increases power consumption. Also, DEM increase the excess loop delay, and can make the system instable. Here the target SNDR is met by increasing the device size to achieve sufficient matching by design. By increasing the device size of the current sources to $W/L = 10$ u/6 u *M1* in Fig. 16 [24], mismatch is minimized. Monte-Carlo simulations indicate a 0.2% mismatch (3-sigma), which is sufficient for the target SNR of 60 dB with 6 dB margin.

The current source of the second DAC does not need to be as large as that of the first DAC because the noise and linearity requirements are relaxed for the second resonator. Any nonlinearity caused after the first resonator barely appears at the output. The same is true for the thermal noise, and therefore a large overdrive is not necessary in the second DAC.

The current-steering switching devices *M3-4* are sized as small as possible for fast switching. This also helps to reduce the clock injection to the resonator by decreasing the parasitic capacitance. Also, the small switch size reduces the parasitic capacitance at the interface with the resonator, which can reduce the feedback factor of the amplifier. With a gate voltage of 900 mV, the switching devices are fully saturated to give the maximum output impedance. The cascode device *M2* is also sized small for fast operation.

The modulator has one HZ DAC and one RZ DAC. These generate return-to-zero pulses, with the outputs nulled for half of the clock period. We use an even number of current sources to generate the pulses. There are total eight current sources in each 9 level DAC. The differential-mode current output of the DAC is zero when the same current flows on both sides of the output. Four current sources are directed to each of the differential outputs to make the return-to-zero phase. Fig. 16 shows DAC latch and current cell implementation, focusing on one side of the differential implementation. The mux has two inputs; the comparator output from the quantizer and the pre-assigned value '0' or '1' that refers the current direction. Four of the eight DAC latches have a pre-assigned value of '0', and the others have a pre-assigned value of '1' to generate the same current on both halves of the DAC output during the return-to-zero output phase. The mux output drives an inverter, which controls the switching devices. The inverter is supplied with a separate 900 mV supply since the switching devices operate in the linear region if the gate voltage is higher than 900 mV. The use of the dedicated supply also helps to isolate the exact switching timing from supply noise
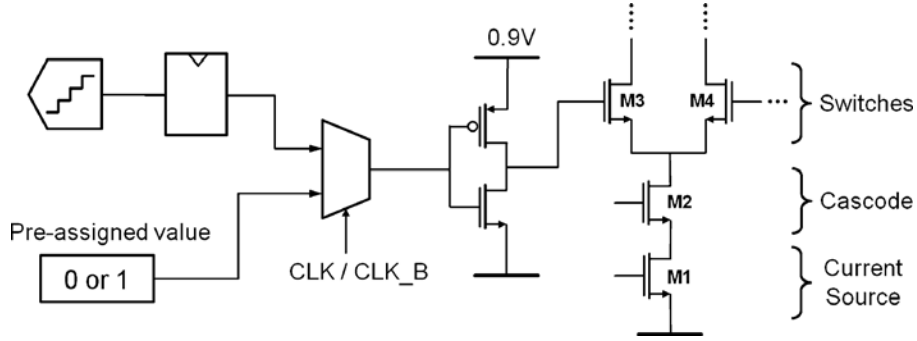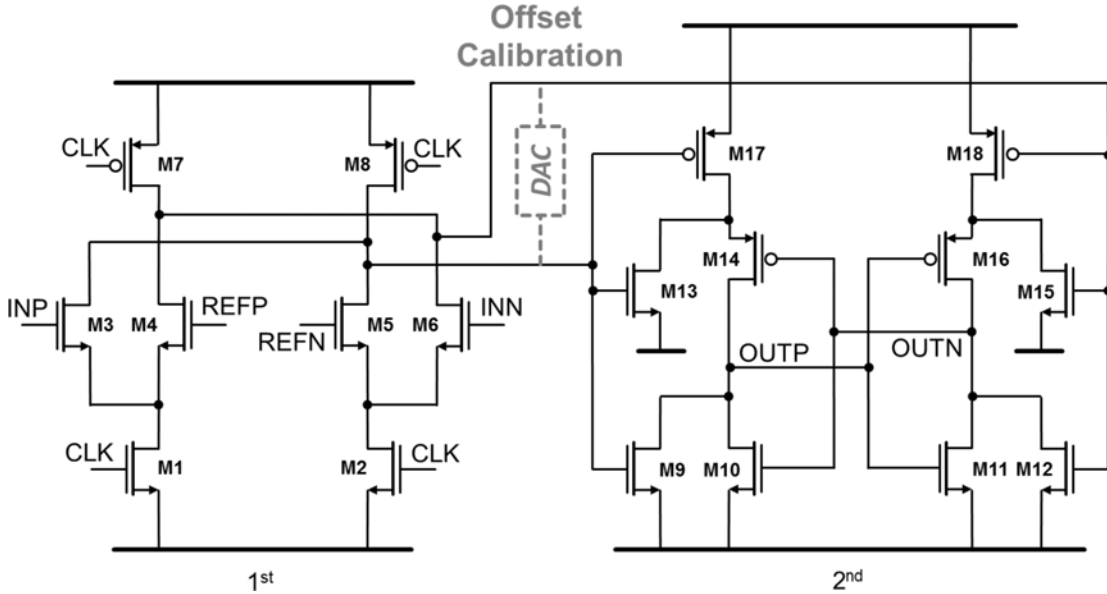
Fig. 16. DAC and DAC latch.

Fig. 17. Comparator in the flash ADC.

B. Flash ADC

The quantizer is a 3-bit flash ADC with eight comparators, and generates a 9-level digital output. The comparator is shown in Fig. 17 [25], and consists of two stages. The comparator outputs are valid only for half a clock period, and an SR latch after the comparator holds the value for the rest half clock period. The comparator input offset is calibrated by trimming the current on the differential inputs at startup [21].

C. Summing Amplifier and Clock Delay Controller

A summing amplifier before the quantizer sums the second resonator output and the feedforward paths. The nonlinearity and thermal noise added at this position hardly affects the modulator performance, so the op-amp can have very simple design. A multi-stage amplifier is also used, but without a feedforward path. The amplifier has three stages and no feedforward path. Miller compensation is used. Resistive feedback is applied to achieve a gain of 1, and large resistors are used for low power consumption, since the thermal noise from these resistors is insignificant.

The clock generator feeds the DACs as well as the quantizer. However, there is a clock path mismatch between these blocks, and more timing difference is caused because the clock receiving devices have different sizes. Furthermore, the summing amplifier is not ideal and introduces a slight delay. When the clock to the DAC is later than that to the quantizer, there is excess loop delay effect, which causes instability. A clock delay controller compensates these clock mismatches by aligning the sampling and the current triggering. The clock delay controller (Fig. 18) is between the clock generator and the quantizer, and consists of a series of buffers and muxes. The calibration is done manually while monitoring peaking in the measured output power spectral density.

V. MEASUREMENTS

The prototype is fabricated in a nine-metal 65-nm CMOS process and the active die area is 0.2 mm^2. Fig. 19 shows the die micrograph. The two resonators take the most of the area due to the passive components. The first DAC occupies most of the DAC block area since the current sources are very large. The measurements are done for 15 samples.

Fig. 20 shows the measured power spectral density of this modulator output. The top-left graph shows the entire spectrum from DC to $F_s/2$. The main graph shows the in-band spectrum over a 24 MHz bandwidth. The input is a 1.6 Vp-p 200 MHz tone, and the measured SNDR is 58 dB while operating with
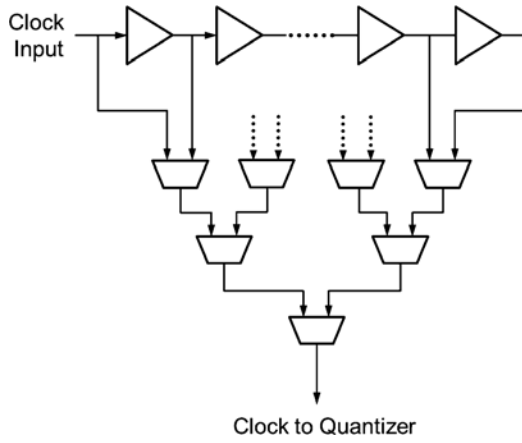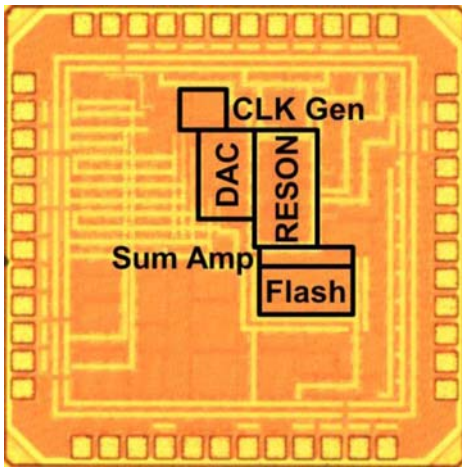
Fig. 18. Clock delay controller.

Fig. 20. Output power spectral density.

Fig. 19. Die photograph.

Fig. 21. Dynamic range with a single 200 MHz tone.

1.25 V supply. The third harmonic appears next to the fundamental tone because it is folded down from a higher frequency. The third harmonic is mainly caused by the amplifier and the DAC nonlinearity. The measured third harmonic is 67.7 dB below the fundamental and so is comparable to the in-band noise and does not reduce the SNDR. The dynamic range is also tested with a 200 MHz tone, and the minimum detectable signal amplitude is -63.9 dBFS. The input amplitude for the maximum measured SNDR is -3.9 dBFS, indicating a dynamic range of 60 dB as in Fig. 21. The dynamic range is limited by the thermal noise from both the first resonator and the first DAC. A two-tone test is performed with two tones 1 MHz apart, with amplitudes of -9.9 dBFS. In Fig. 22, the intermodulated tones are -74.72 dBFS and -74.47 dBFS, and this indicates a modulator IM3 of 65 dB.

The total power consumption including that of the clock generator is 12 mW. Table I shows the power consumption of each block. The digital part consists of the quantizer and the DAC latch. The DAC latch consumes most of the digital power due to the switching.

Table II summarizes the performance of this prototype. The sampling rate is 800 MHz, and the center frequency is 200 MHz, which is the quarter of the sampling frequency. The FoM is 385 fJ/conv-step, which to our knowledge is the best

Fig. 22. Two-tone test.

for CTBPDSMs using active resonators. Table III compares this work with the state-of-the-art.

VI. CONCLUSION

Several methods to reduce the power consumption of CTBPDSMs are introduced. A power-efficient single op-amp resonator replaces an LC tank resonator to achieve both low power and low area. A new positive feedback scheme enables a single op-amp resonator with only a few passive components. A simple fourth-order architecture with low power consumption

TABLE I
POWER CONSUMPTION

Analog		
1st Resonator	1.25V	2mW
2nd Resonator	1.25V	1.5mW
DACs	1.25V	1mW
Sum. Amplifier	1.25V	0.5mW
Digital	1V	4mW
Clock Gen	1V	2mW
DAC Driver	0.9V	1mW
Total		12mW

TABLE II
PERFORMANCE SUMMARY

Sampling Rate	800MHz
Center Frequency	200MHz
BW	24MHz
Power	12mW
SNDR	58dB
DR	60dB
IM3	64.5dB
Area	0.2mm^2
FoM	385fJ/conv-step

TABLE III
COMPARISON CHART

	Ryckaert 2009 [27]	Lu 2010 [28]	Harrison 2012 [7]	Shibata 2012 [8]	This Work [26]
Order	6th	6th	6th	6th	4th
Resonator	LC	active-RC	LC	LC + active-RC	new RC
DR [dB]		70		74	60
F_s [MHz]	3000	800	3200	4000	800
F_c [MHz]	2400	200	7-800	450	200
BW [MHz]	60	10	20	150	24
SNDR [dB]	40	68.4	70		58
SNR [dB]				69	
Power [mW]	40	160	20	550	12
Area [mm2]	0.8	2.5	0.4	5.5	0.2
Process	90nm CMOS	0.18um CMOS	40nm CMOS	65nm CMOS	65nm CMOS
FoM [pJ/ conv-step]	4.08	3.72	0.19	0.8	0.38

is also introduced. This architecture minimizes the number of DACs, and reduces power consumption, silicon area, and thermal noise.

A prototype based on these techniques achieves good performance, and has the better power efficiency than state-of-the-art designs. The power efficiency approaches the efficiency of CTLPDSMs, helping to make CTBPDSMs practical. This in turn makes it easier to build an SDR without a power penalty compared to super-heterodyne receivers.

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