A Long-Range RFID IC with On-chip ADC in 0.25 μm CMOS

Fatih Kocer and Michael P. Flynn

Wireless Integrated Microsystems Engineering Research Center (WIMS-ERC)
University of Michigan, Ann Arbor, MI, 48109

Abstract — **This 1mm² wireless telemetry device recovers power and a reference clock from a 450 MHz incident RF signal and returns data as a binary phase shift keyed signal on a 900 MHz carrier. The device generates a 3 V_{DC} supply from a -12.3 dBm incident RF signal. This corresponds to an operating distance of more than 18 meters in the US. The transmit data includes the output of an on-chip 5-bit single-slope analog-to-digital converter (ADC) and a 3-bit ID tag. The entire IC dissipates 4mW while active.**

Index Terms — **Analog-to-digital conversion, MOSFET power amplifiers, phase shift keying, RFID, UHF-transponders, wireless power transfer.**

I. Introduction

There is a growing interest in long-range radio frequency identification devices (RFID) for use in manufacturing, product distribution, sales, security and surveillance. Traditional RFID devices, used for remote entry and biomedical applications, work in very close proximity to a base station (often with a range of only tens of centimeters) [1,2]. RFID devices recover both power and a reference clock from an RF signal sent by a base unit. The maximum separation between the base unit and the RFID device is dictated by the efficiency of the RF-DC conversion and by the power dissipation of the wireless device.

The operating range has been extended through the use of more efficient RF-DC conversion and power efficient system design [3,4]. The ID device described in [4] has a reported range of 4.5 meters, but requires a non-standard CMOS process incorporating Schottky diodes.

A number of innovations are described in this paper that increase range and functionality, yet are compatible with CMOS technology. Power efficient techniques are employed for power rectification, power control and clock recovery. These increase the range of operation to more than 18 meters. The IC incorporates an on-chip analog-to-digital converter (ADC) for data gathering. A simple, yet efficient technique is proposed for binary phase shift keying modulation. The entire system is implemented with an area of 1 mm² in a 0.25 μm CMOS process.

Fig. 1 shows a block diagram of the system. The rectifier/multiplier recovers energy from the 450 MHz incident RF. Thanks to the voltage multiplication of the rectifier/multiplier, the storage capacitor can be charged to a useable supply voltage (>2.5 V) even with a small incident signal voltage amplitude (>160 mV_{rms}). A mode-selector circuit monitors the voltage on the capacitor, and enables the IC when sufficient energy is stored. During standby mode, while the capacitor is charging, the circuitry dissipates only 900 nA. The device requires an RF input power of only -12.3 dBm to generate a 3 V_{DC} supply.

A bias generator provides stable, supply-insensitive reference currents and voltages for the entire system. A 900 MHz carrier is generated by a 900 MHz LC oscillator, injection locked to the incident 450 MHz signal. In this way, a very low phase noise system clock is generated without the high power consumption of more conventional techniques, such as Schmitt triggers.

The 8-bit transmit data is supplied by an on-chip single-slope 5-bit ADC and a 3-bit programmable ID word. The BPSK modulator modulates this data onto the 900 MHz carrier. The modulated signal is fed to a pseudo-differential class-B power amplifier (PA) which drives -24 dBm into the 50 transmit antenna. A frequency divider provides a synchronous clock for the binary phase shift keying (BPSK) modulator and the ADC. Both the receive and transmit frequencies are much higher than with traditional RFID devices (<10 MHz), significantly reducing the size of the transmit and the receive antennas.

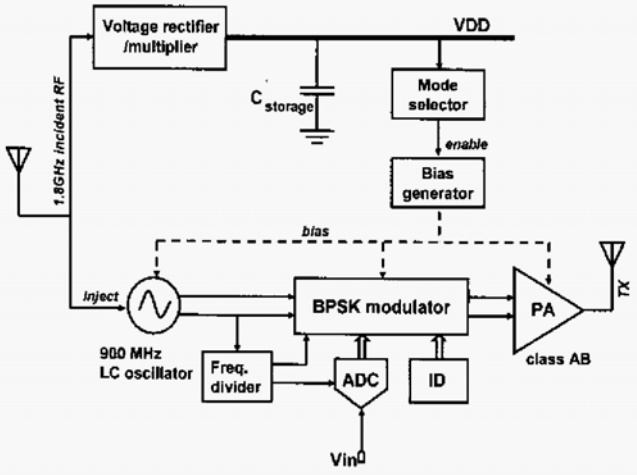

Fig. 1. Block diagram of the presented architecture

II. Building Blocks

A. RF-to-DC Converter

The rectifier/multiplier circuit is a MOS implementation of the Cockcroft-Walton voltage multiplier [5] as shown in Fig. 2. Each stage has two inputs. A DC input from the previous stage, and an RF input from the receiving antenna. Each stage works as a voltage rectifier adding peak amplitude of the received RF signal to the input DC voltage. The diodes are implemented with low V_{TH} PMOS transistors to achieve low voltage operation and low loss. The simulated voltage drop on each diode-connected transistor is only 150 mV at 17 µA. With an input signal of only 160 mV_{rms}, 3 V_{DC} is generated. We define voltage conversion efficiency of the multiplication as

$$Efficiency = \frac{V_{out}}{V_{in\_peak} \times n}. \quad (1)$$

where V_{out} is the generated output voltage, V_{in_peak} is the peak incident RF amplitude and there are n stages.

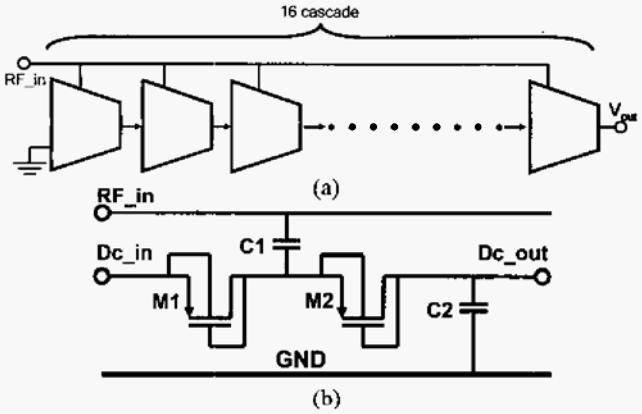

Fig. 2. (a) Block diagram, (b) single stage of voltage multiplier

With the minimum required incident RF power, the measured efficiency of the 16-stage multiplier is 78%. Wireless tests were done in a 2 meters long anechoic chamber. With the RFID device placed 1.65 meters from the transmitter, the minimum RF power transmitted from the base station to generate a 3 V_{DC} supply was measured at 17.5 dBm (~60 mW). Using Friis' free space propagation formula [6], this corresponds to a maximum operating distance of 18.3 meters assuming the 7 W (38.5 dBm) maximum transmit power specified by the FCC in the US.

B. Mode Selector and Bias Generator

The mode selector circuit detects when the capacitor voltage exceeds a threshold (3 V), powering up the entire device. The entire system continues to operate until the capacitor voltage drops below a lower threshold (1.5 V) allowing the capacitor to recharge. The mode selector circuit, shown in Fig. 3, is implemented entirely with MOS devices. Since this implementation does not incorporate resistors (unlike [7]) the circuit is very compact, occupying only 0.01 mm^2. A hysteresis comparator compares two trip voltages, generated by MOS resistive ladders **A** and **B.** Current starved buffers sharpen the transitions, yet add little power dissipation. The mode selector dissipates an average of only 900 nA.

Because supply regulation is inefficient, we use a bootstrapped bias generator (M1-M6 in Fig. 3) to produce current and voltage references that are stable over the 1 V to 3 V supply voltage range. The bias generator draws 12 µA when enabled by the enable transistor M6.

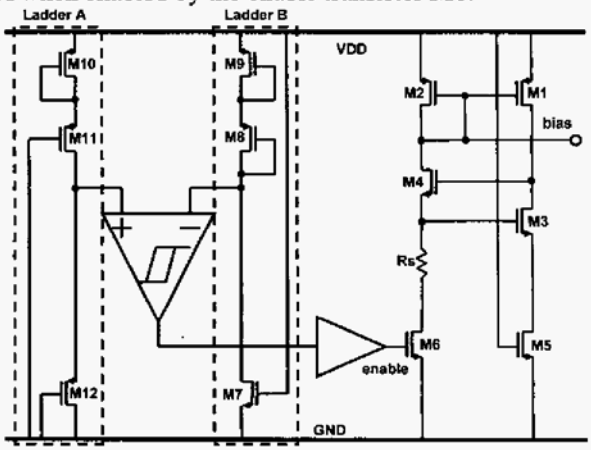

Fig. 3. Schematic of the mode selector and the bias generator

C. Clock Generator

Unlike conventional RFID systems, the proposed architecture employs an on-chip LC oscillator injection locked to the incident RF signal for clock recovery [7]. Injection-locking is far more power efficient than Schmitt trigger based schemes, and delivers a recovered clock with very low phase noise and jitter. Moreover, by locking to a harmonic of the incident signal, frequency separation between the incident RF signal and the transmitted carrier is achieved without using a PLL.

Careful biasing minimizes supply voltage dependence. The measured supply sensitivity of an unlocked oscillator is only 70 ppm/V. A lock range of 12 MHz for a -12 dBm 450 MHz incident RF signal is achieved. The measured phase noise of the oscillator in free running operation is -112.5 dBc/Hz at a 1 MHz offset, corresponding to a figure of merit [8] of 167 dBc/Hz. When locked to a 450 MHz signal the scheme provides outstanding reference frequency stability, with a measured phase noise of -99.1 dBc/Hz at 10 kHz offset.

D. BPSK Modulator

The IC incorporates a compact, yet power-efficient BPSK modulator, shown in Fig. 4. A divide-by-128 circuit comprised of a cascade of true-single-phase and static master-slave D-flip-flops generates a synchronous clock for the modulator. This approach differs from most modulator architectures where a lower frequency is already available.

The transmit ID and ADC data are latched by an 8 bit register. The modulator clock increments a 3-bit counter, the output of which is decoded to select the transmit bit in a round-robin fashion from the 8-bit register. The differential output of the LC oscillator is connected to the PA through a two-input, two-output multiplexer. The value of the selected transmit bit determines how the multiplexer routes the oscillator's differential output to the differential input of the power amplifier. In this way, when the transmit bit changes from 0 to 1 or 1 to 0, the phase of the modulated output changes by 180 degrees. A non-overlap circuit generates the gate signals to the four NMOS switches of the multiplexer, ensuring break-before-make switching, preventing the oscillator outputs from being inadvertently shorted together.

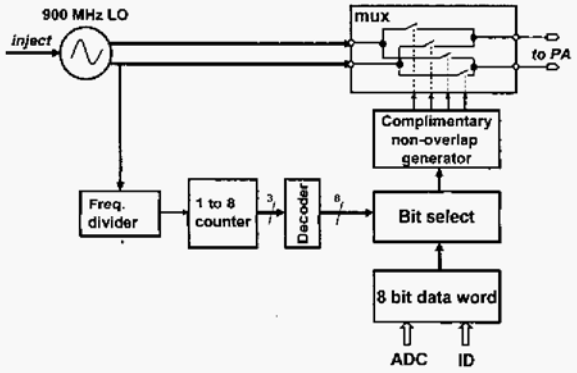

Fig. 4. BPSK modulator

E. Single Slope 5 bit ADC

A block diagram of the single slope on-chip ADC is shown in Fig. 5. A high output resistance current source charges an integrating capacitor, while the capacitor voltage is compared with the input voltage to the ADC.

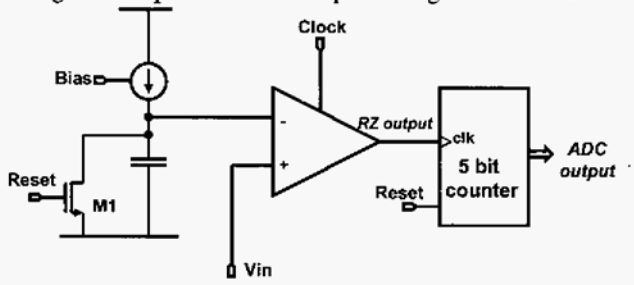

Fig. 5. Block diagram of the ADC

The comparator decision remains 1 while the capacitor voltage is less than the input voltage. The comparator output is supplied as a clock signal to a 5 bit counter. Since the comparator produces a return-to-zero output (conventional comparators produce non-return-to-zero), the counter increments while the capacitor voltage is less than the input voltage. At the end of the conversion cycle, the capacitor voltage is set to 0 V and the counter state is reset to 0. Both the reference current and reference voltage are supplied by the on-chip bias generator.

F. Class-B Push-Pull Output Stage

One of the two identical halves of the pseudo-differential class-B power amplifier is shown in Fig.6. Transistors M3, M4, and M5 set up the quiescent gate voltages for the NMOS and PMOS output devices (M1 and M2). The RF input signal (V_{RF_IN}) comes directly from the BPSK modulator, while the bias generator supplies the gate voltage for M4 (V_{BIAS}). Capacitors C1 and C2 couple V_{RF_IN} to the gates of the output transistors, M1 and M2.

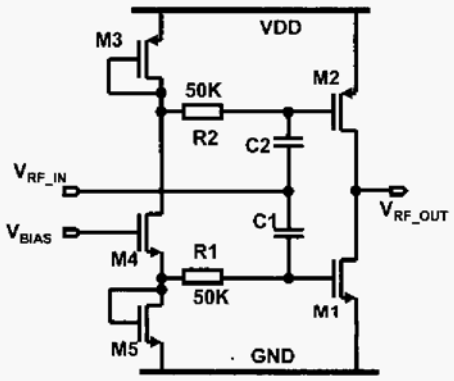

Fig. 6. Block diagram of the PA

III. TEST RESULTS

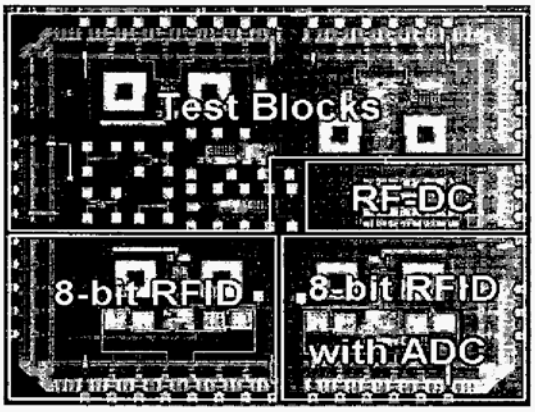

Fig. 7. Photomicrograph of the fabricated IC

The prototype was fabricated in a 5-metal 0.25 µm TSMC CMOS process, incorporating low V_{TH} transistors and thick top metal. The active area of the design is 1 mm^2. The prototype incorporates ESD protection on all pins. The IC was packaged in a 52-pin ceramic LCC package and surface mounted on a 4-layer PCB. A die photograph is shown in Fig. 7.

Transmitted, modulated 900 MHz signals from the prototype device were captured and verified with the help of an 8 Gsample/s oscilloscope and a spectrum analyzer. Captured transmit signals for two different words, along with a bit-rate reference clock, are shown in Fig. 8. The output spectrum of the BPSK modulated 900 MHz signal is shown in Fig. 9. The characteristics of the prototype IC are summarized in the Table I.

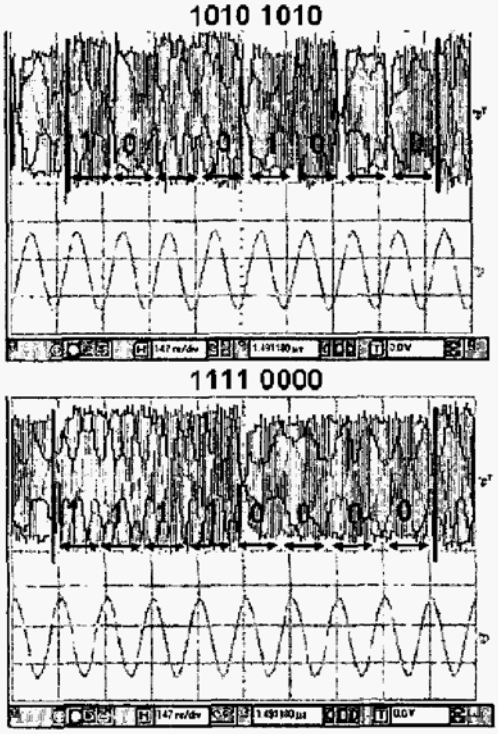

Fig. 8. Captured transmit signals for 4 different words.

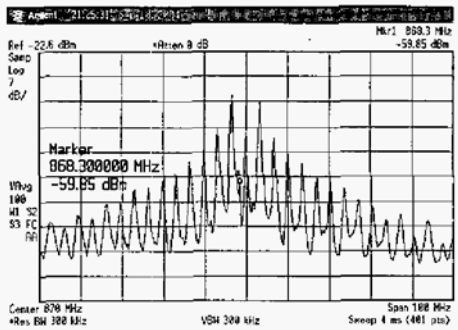

Fig. 9. Output spectrum for 10101010 word.

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Table I. System summary

Technology	TSMC 0.25 µm with thick top metal	
Active area	~1 mm^2	
Modulation	Binary Phase Shift Keying	
Carrier Freq.	900 MHz	
Carrier Power	-24 dBm on 50Ω	
Max Oper. Range	18.3 meters (7 W base station power)	
Power Consumption	**Standby**	**Active**
	<900 nA	2 mA
Ph.Noise @ 10kHz (dBc/Hz)	**Free Running**	**Locked @ f/2**
	-88.5	-99.1
FOM (dBc/Hz)	167	178

REFERENCES

[1] Q. Huang and M. Oberle, "0.5 mW passive telemetry IC for biomedical applications," *IEEE Journal of Solid-State Circuits*, vol. 33, pp. 937-946, July 1998.

[2] S. Masui, E. Ishii, T. Iwawaki, Y. Sugawara, and K. Sawada, "13.56 MHz CMOS RF identification transponder integrated circuit with a dedicated CPU," *Digest of Technical Papers IEEE International Solid State Circuits Conference*, pp. 162-163, Feb. 1999.

[3] F. Kocer, P. M. Walsh, and M. P. Flynn, "An injection locked, RF powered, telemetry IC in 0.25 µm CMOS," *2004 Symposium on VLSI Circuits, Digest of Technical Papers*, pp. 24-27, June 2004.

[4] U. Karthaus and M. Fischer, "Fully integrated passive UHF RFID transponder IC with 16.7 µW minimum RF input Power," *IEEE Journal of Solid-State Circuits*, vol. 38, pp. 1602-1608, October 2003.

[5] M. D. Bellar, E. H. Watanabe, and A. C. Mesquita, "Analysis of the dynamic and steady-state performance of Cockcroft-Walton cascade rectifiers," *IEEE Transactions on Power Electronics*, vol. 7, pp. 526-534, July 1992.

[6] D. K. Cheng, *Field and Wave Electromagnetics*: Addison Wesley, 1989.

[7] F. Kocer, P. M. Walsh, and M. P. Flynn, "Wireless, remotely powered telemetry in 0.25 µm CMOS," *Digest of Papers-2004 IEEE Radio Frequency Integrated Circuits (RFIC) Symposium*, pp. 339-342, June 2004.

[8] M. Tiebout, "Low-power low-phase-noise differentially tuned quadrature VCO design in standard CMOS," *IEEE Journal of Solid-State Circuits*, vol. 36, pp. 1018-1024, July 2001.