A 5GHz Fully Integrated Super-regenerative Receiver with On-chip Slot Antenna in 0.13µm CMOS

Dan Shi[1], Nader Behdad[2], Jia-Yi Chen[3], and Michael P. Flynn[1]

[1]University of Michigan, Ann Arbor, MI, [2]University of Central Florida, Orlando, FL
[3]ZeroG Wireless Inc., Sunnyvale, CA
734-647-1818, shid@eecs.umich.edu

Abstract

A single chip receiver based on super-regeneration incorporates an on-chip slot antenna and digital received data synchronization. A capacitively-loaded standing-wave resonator improves energy efficiency. An all-digital PLL timing scheme synchronizes the received data clock. The prototype 5GHz receiver, implemented in 0.13µm CMOS, achieves a data rate of up to 1.2Mb/s, dissipates 6.6mW from a 1.5V supply, and occupies a die area of 2.4mm^2.

Introduction

Single-chip, fully-integrated receivers have applications as diverse as sensing, smart cards, medical implants and contactless testing. We describe a complete single-chip multi-channel receiver incorporating on-chip antenna, self-calibrated super-regenerative core and digital baseband clock synchronization. Recently, super-regenerative receivers have shown promise for short-range low-data-rate applications [1-3]. However, for good performance, an off-chip resonator and an off-chip antenna are usually required. We present a super-regenerative receiver that utilizes an on-chip slot antenna in place of the large off-chip antenna and matching network, reducing total system size by more than an order-of-magnitude. To increase energy efficiency, the super-regenerative oscillator core is based on a compact, capacitively-loaded, standing-wave resonator (Q~35) [4]. An all-digital PLL scheme synchronizes the received data clock. As a compromise between antenna efficiency and receiver power consumption, an RF frequency of 5GHz is chosen. The prototype fabricated in a standard 0.13µm RF CMOS process occupies 2.4mm^2 and has a measured energy per received bit of 5.5nJ/bit.

Architecture

A super-regenerative receiver determines RF signal amplitude based on the variation of the start-up time of a resonant (e.g. LC) oscillator, making it ideal for the detection of AM or OOK. The RF signal is injected into the oscillator core, so that a larger RF signal leads to a shorter start-up time. The oscillator bias current is controlled by a quench signal. The critical oscillator bias current (*Icrit*) is defined as the minimum bias current for oscillation.

At the beginning of each detection period, the oscillator bias is set slightly below *Icrit* so that the oscillator core instead functions as a Q-enhanced filter, selecting the channel of interest. Next the bias current is raised above *Icrit* enabling super-regeneration and the start-up time is monitored. Finally, at the end of each bit detection period, the oscillator is disabled so that the next bit can be detected without interference from any residual oscillation.

Fig. 1 shows the system architecture of the proposed receiver. The incoming RF signal is received by the on-chip slot antenna, amplified by a differential LNA and injected onto the oscillatory nodes of the standing-wave VCO. The higher Q of a compact capacitively-loaded, standing-wave resonator [4] reduces the power consumption of the regenerative core from 3.2mW (for conventional LC) to a measured value of 2.1mW.

The quench bias current, which controls oscillator mode, is generated by an on-chip 9b DAC. Similar to [3], a SAR search estimates *Icrit*. Also during calibration, a frequency synthesizer loop (see Fig 1) tunes the receiver to one of eight possible frequency channels. Repeated detection periods follow the critical current search and frequency tuning. An all-digital PLL adjusts the timing of the quench waveform so that the phase and frequency of the receiver tracks that of the transmitted data. The overall output of the receiver is demodulated data and a data-rate clock signal.

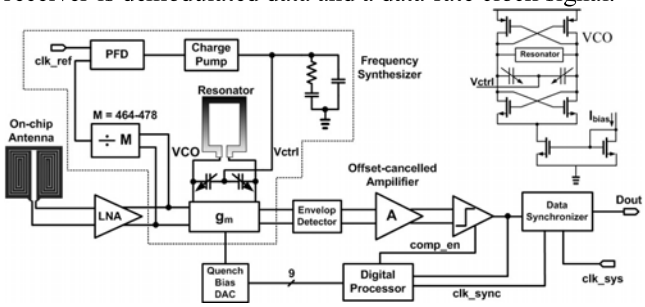

Figure 1: Block diagram of the receiver.

Each detection period spans 10 cycles of the synchronized 10x-data-rate clock (*clk_sync* in Fig. 2). During the first 4 cycles, the oscillator bias is set slightly below *Icrit*, so that the receiver operates as a Q-enhanced filter. During the next 5 cycles the oscillator bias exponentially increases above *Icrit*, the oscillator envelope is detected and the comparator is enabled, so that the receiver senses the RF amplitude. Finally during the last cycle the oscillator bias is quenched, so no residual oscillation interferes the next detection period.

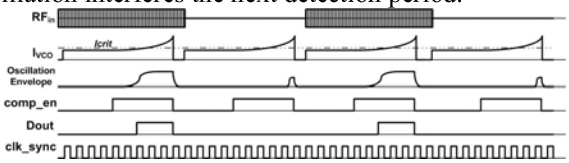

Figure 2: Timing diagram of system in detection mode.

On-chip Antenna and Circuit Implementation

The on-chip 5GHz antenna occupies a die area of only 0.47mm^2 making it 50 times smaller than a traditional dipole antennas operating at the same frequency. The antenna (Fig. 3) is composed of a straight slot section connected to two balanced spirals at its ends [5], with an overall electrical length of λ/4 from the feed point to the end of each balanced spiral. Shielding composed of two floating lower metal layers prevents the substrate from dissipating energy, increasing the radiation efficiency of the antenna. Although the measured antenna gain (-17dBi)

is less than that of a large off-chip antenna (> 1dBi), losses due to cabling, matching and ESD protection are avoided.

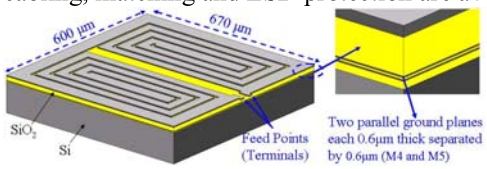

Figure 3: Topology of the 5GHz miniaturized slot antenna.

The 5GHz RF frequency and varying common-mode voltage the new resonator VCO structure pose challenges for the design of the envelope detector. Fig. 4(a) shows the schematic of the envelope detector (power consumption 0.12mW). To avoid problems with common-mode-level changes of the VCO output, a differential to signal-end converter is used. As the amplitude of input signal increases, the gate voltages of the weak inversion biased [6] N-type transistors (M1, M3) decrease to keep the average drain current constant, and the output voltage *Voutp* increases correspondingly, tracking the input signal amplitude. RC filters (R2, C3, and R4, C6) remove the AC component. A replica circuit (on the right) is used to generate a pseudo-differential signal envelope.

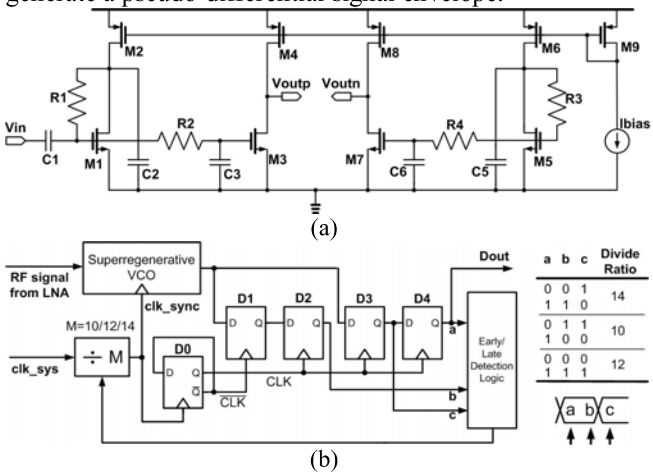

Figure 4: (a) Envelope detector. (b) Synchronizer.

The synchronizer (Fig. 4b) works as an all-digital PLL, changing the divide-ratio and *clk_sync* depending on early/late decision logic. The demodulated super-regenerative data (i.e. output of the envelope detection comparator) feeds two sets of flip-flops D1, D2 and D3, D4, where D2, D3, D4 are triggered by *CLK* (half of *clk_sync* frequency) and D1 is triggered by $\overline{CLK}$ [7]. *a*,*b*,*c* represent consecutive data samples with *a* and *b* coming from one super-regeneration detection period and *c* coming from the next. If correctly synchronized, *a* and *c* should sample the center of data eyes. Depending on the values of a, b and c the detection logic controls the divide ratio of the multi-mode divider (10, 12 or 14). The sampling position moves up (divide ratio =10), down (divide ratio =14) or does not change (divide ratio =12), depending on the early/late detection logic.

Prototype Measurements

The prototype (Fig. 5) is fabricated in an 8-level-metal 0.13µm RF CMOS process. The receiver, including antenna, occupies 2.4mm^2. The total die area including pads is 4mm^2. To measure the BER and sensitivity of the receiver alone, the on-chip antenna is disconnected and a pseudo-random NRZ modulated signal is fed to the LNA through a GSSG probe. The results are shown in Fig. 6. A 10dBm sensitivity improvement is observed when the synchronizer is enabled. Using the measurement setup described in [5] the gain of the passive antenna is measured to be approximately -17.0 dBi at 5GHz. The measured results are summarized and compared with [3] in Table I.

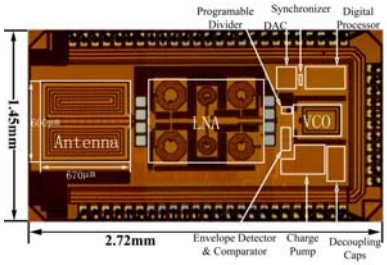

Fig. 5: Die micrograph.

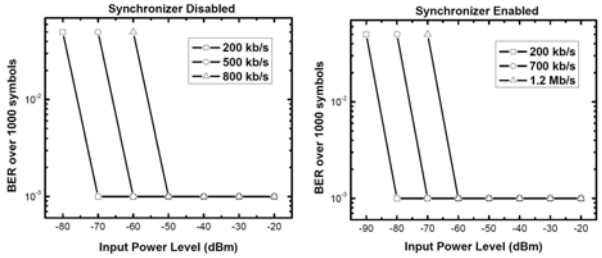

Figure 6: Measured BER vs. input power level at different data rate. (a) synchronizer disabled. (b) synchronizer enabled.

Table I: Summary of measurement results.

		This work	[3]
RF Frequency		4. 9184-5.0668GHz	2.35-2.53GHz
Power Consumption		6.6mW	2.8mW
Sensitivity		-90dBm	-90dBm
Adjacent Channel Rejection		30dB	30dB
Data Rate	**w/ on-chip antenna**	120kb/s	-
	w/o on-chip antenna	200kb/s to 1.2Mb/s	500kb/s
BER		≤0.1%	≤0.1%
Channel Number		8	9
Energy per received bit		5.5nJ @ 1.2Mb/s, 55nJ@120kb/s	5.6nJ@500kb/s
Synchronization		On chip (digital PLL)	Manual
On-chip Antenna		Yes	No
Tank Q		35	~15
Die Area		2.4 mm^2 inc. antenna	1mm^2
Technology		0.13µm CMOS	0.13µm CMOS

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