

# A Low-Power Adaptive Receiver Utilizing Discrete-Time Spectrum-Sensing

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**Abstract**—A flexible spectrum-sensing receiver in 65-nm CMOS consists of a wideband front-end spectrum-adaptive (SA) filtering, switched-capacitor amplifiers, and a filtering specific absorption rate ADC. The SA filter uses a discrete-time (DT) spectrum-analyzer and a reconfigurable DT notch filter to detect and suppress strong interferers over a 55-MHz range. In IEEE 802.15.4 tests, the receiver exceeds sensitivity and interferer rejection requirements. With SA filtering enabled, it achieves  $\geq +55$ -dB rejection from +25- to +65-MHz FM interferers.

**Index Terms**—Discrete-time (DT) filter, spectrum-sensing (SS), wireless receiver.

## I. INTRODUCTION

THE WIRELESS communication spectrum has become increasingly congested in terms of both the diversity of wireless standards and the number of users sharing limited spectrum. Recent research has focused on the first part of the congestion issue, leading to many successful software-defined radio (SDR) techniques, such as a highly linear front-end with tunable analog filters [1], frequency-translated RF and IF band-pass filters [2], and a configurable filtering specific absorption rate (“SARfilter”) ADC [3]. Although these techniques achieve certain performance goals, they inefficiently utilize hardware and power by always assuming the worst case operating environment.

We propose a spectrum-sensing (SS) method for detecting and adaptively filtering strong interferers. Integrating such a spectrum-adaptive (SA) filtering system into a wireless receiver enables the receiver to adapt to changing conditions and also

Manuscript received September 30, 2012; revised January 06, 2013; accepted January 08, 2013. Date of publication February 12, 2013; date of current version March 07, 2013. This work was supported by the U.S. Army Research Laboratory under Contract W911NF, prepared through collaborative participation in the Microelectronics Center of Micro Autonomous Systems and Technology (MAST) Collaborative Technology Alliance (CTA). This paper is an expanded paper from the IEEE RFIC Symposium, Montreal, QC, Canada, June 17–19, 2012.

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Digital Object Identifier 10.1109/TMTT.2013.2243747

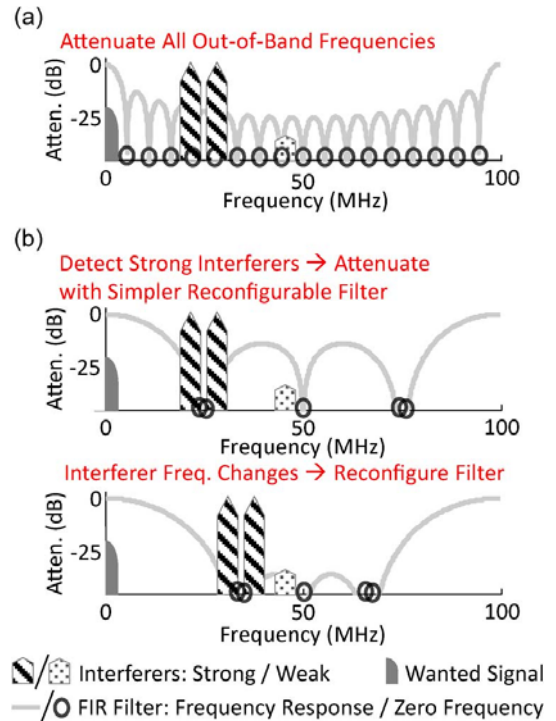


Fig. 1. Example comparing: (a) conventional and (b) SA filtering. A conventional filter attenuates all out-of-band frequencies with a relatively complex filter (18-tap analog DT FIR with 17 zeros). An SA filter uses SS to detect the largest interferers and configures the zero locations of a simpler SS-guided filter (six-tap FIR with five zeros) to attenuate these interferers.

use less circuitry and less power. Many of the existing SS techniques are specialized for cognitive wireless networks [4], such as IEEE 802.22 or 802.11af, which require high-sensitivity detection of licensed users. The SS method discussed in [5] implements a precise and configurable sensing bandwidth in an auxiliary signal path with a digitally driven analog correlator. The method discussed in [6] measures power in the main signal path with an energy detector that rectifies the baseband signal. Since this detector relies on the filters in the main path to define the measurement band, the measurements are limited to the channel being received. The authors of [7] propose digital-domain SS, which requires a high-speed high-resolution ADC and antialiasing filtering to digitize the entire band of interest. These approaches are not appropriate for use as a spectrum-analyzer in an SA filtering implementation because their power and complexity would eliminate the potential gains in power and area of replacing a conventional filter with the SA filter. Instead, we realize SA filtering by creating a robust, scaling-friendly, and low-power *analog* discrete-time (DT) SS technique to detect

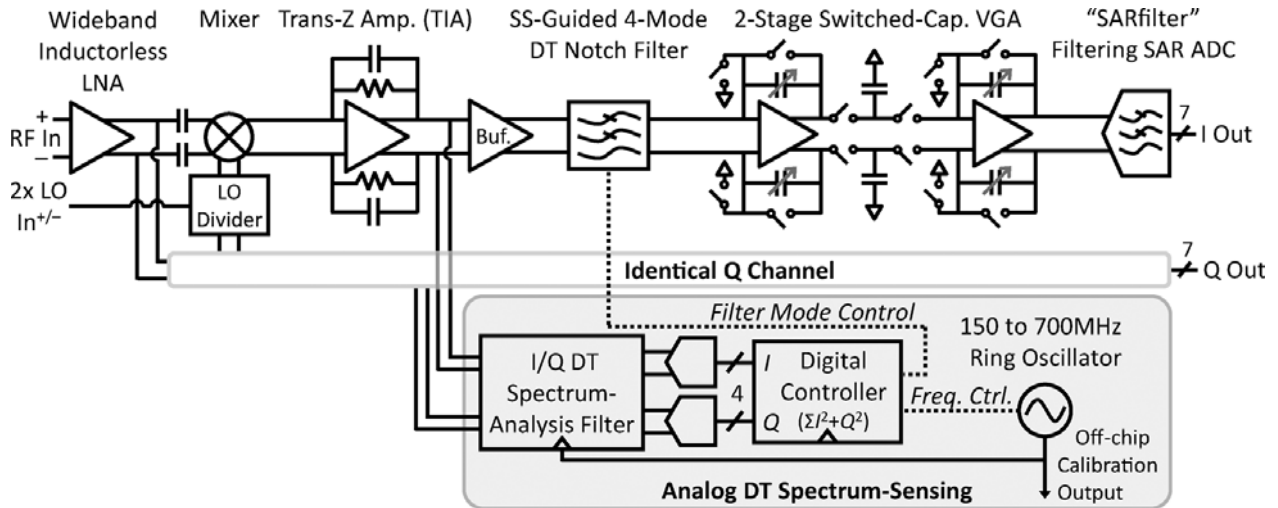


Fig. 2. Architecture of the prototype SS receiver. The SS path (*bottom*) scans to detect strong interferers and automatically selects the optimal rejection mode of the SS-guided reconfigurable DT notch filter.

strong interferers. We then adapt the attenuation profile of a reconfigurable filter in response to the detected interferers.

Without SS, we would have to overdesign the receive filters to attenuate all potential interferers at all times, even if we can reasonably expect only a limited number of intermittent simultaneous interferers. Empirical studies of spectrum occupancy in populated areas [8], [9] show that spectrum usage ranges widely from  $<10\%$  in many bands to nearly constant occupancy in broadcast television and cellular bands. In low occupancy bands, the low likelihood of simultaneous high-power interferers and their changing frequencies suggest that targeted SA filtering can fulfill a receiver’s interferer rejection needs. In high-occupancy bands with sporadic mobile transmitters, such as cellular bands, an SA filter greatly reduces the attenuation required of a conventional filter by adaptively rejecting the strongest interfering signals from nearby sources.

### A. Benefits of Targeted SA Filtering

SS and adaptive filtering enables more energy and area efficient filtering of strong, time, and frequency varying interferers than conventional fixed filtering. Fig. 1 compares possible conventional and SA *analog* DT filter configurations in a wireless receiver. Analog DT filters are charge-domain finite impulse response (FIR) and infinite impulse response (IIR) filters that are implemented by sampling onto different sections of a capacitor bank over multiple clock cycles and passively charge-sharing the sampled charge. In the conventional filtering case [see Fig. 1(a)], the filter implements a fixed frequency response. Therefore, the filter must create a large number of zeros, indicated by the black zeros, in order to attenuate potential interferers across the entire frequency band. In the SA filtering case [see Fig. 1(b)], a robust, scaling-friendly, and low-power analog DT SS system detects strong interferers and reconfigures a simpler SS-guided filter in real time to achieve equivalent or better rejection. Weak interferers are allowed to pass through and are rejected further down the receive chain. The area and power of an analog DT filter scales approximately with the FIR tap length so the SA filter in this example achieves approximately three times less area and power usage.

## II. OVERVIEW OF THE SS RECEIVER

An SA filter detects the largest interferer in the 15–70-MHz range and selects the mode of a configurable SS-guided *analog* DT notch filter [similar to Fig. 1(b)] that most strongly attenuates this interferer. We demonstrate SA filtering in a flexible receiver [10] (Fig. 2) consisting of an in-phase/quadrature (I/Q) RF-in to digital-out “main” receive path (Fig. 2, top half) and an analog DT SS “auxiliary” path (Fig. 2, bottom half in gray box). The main path consists of a wideband front-end, a transimpedance amplifier (TIA), a four-mode SS-guided analog DT notch filter, switched-capacitor (SC) amplifiers, and a 7-bit SARfilter ADC that performs both filtering and digitization. The auxiliary SS path splits from the main path at the output of the TIA. This auxiliary path consists of an I/Q analog DT spectrum-analysis bandpass filter, ADCs that digitize the filter’s output, a simple digital controller, and a calibrated ring-oscillator that clocks the bandpass filter. We verify the performance of SA filtering in this prototype receiver by receiving IEEE 802.15.4 packets in the presence of interferers that are offset 15–70 MHz from the wanted signal.

### A. Receiver Filtering Strategy

The SA receiver implements three filters that each serves a different purpose. The SS-guided configurable analog DT filter attenuates strong interferers offset 15–70 MHz from the wanted signal. If not attenuated, these interferers would distort the two stages of SC amplifiers that precede the ADC (Fig. 2). Lower power interferers that do not desensitize the receive chain are allowed to pass through to the SARfilter ADC, where an embedded configurable analog DT low-pass filter reuses the ADC’s circuitry to reject interferers *before* digitization. Both the SS-guided filter and the SARfilter ADC implement DT filters, which have high-frequency passbands located at multiples of their sampling frequency. A pole at  $\approx 8$  MHz in the TIA (after the mixer) attenuates these passbands.

### B. SS Guided Reconfigurable Notch Filter

Our proposed SA filtering system detects the frequency of a strong interferer with SS, and then uses this information as

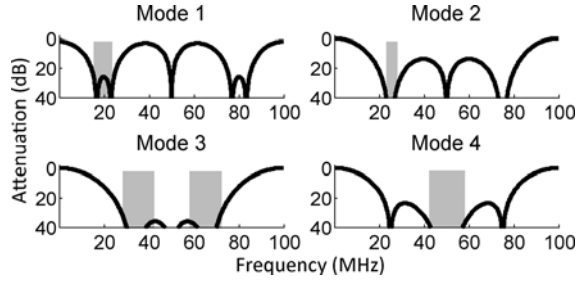


Fig. 3. Ideal frequency responses of the four modes of the SS-guided notch filter. The gray shaded areas indicate the frequencies that each mode targets.

a guide to configure a multimode filter. As a proof-of-concept of SS-guided filtering, we integrate a four-mode six-tap analog DT FIR filter into the receive chain after a TIA output buffer (Fig. 2). Fig. 3 plots the ideal frequency responses of the four filtering modes and highlights the frequencies that each mode attenuates with gray shading. Fig. 4 shows a schematic of a differential half-bank of this filter, which consists of 22 unit capacitors and switches in each time-interleaved channel. We create this six-tap FIR filter by sampling over six clock periods onto capacitors of different sizes and charge-sharing the capacitors.<sup>1</sup> Since a six-tap filter inherently decimates the rate by  $6\times$ , we time-interleave six channels to achieve equal input and output rates (100 MS/s in prototype measurements). In Section IV, Table III summarizes the FIR tap coefficients.

### C. SC Amplifiers

Two stages of SC variable-gain amplifiers (VGAs), located after the SS-guided DT notch filter (Fig. 2), amplify the received signal by up to 35 dB. Digitally tunable capacitances in the first stage scale proportionally to the number of active unit capacitors in each notch filter mode to preserve gain and also to compensate for 2.2 dB of loss at dc in mode 1 (Fig. 3) of the notch filter. Digitally tunable capacitances in the second stage implement variable gain. Chopping switches (omitted from Fig. 2) at the input and output of the first and second stages, respectively, reduce  $1/f$  noise.

### D. SARfilter ADC

A modified version of the SARfilter ADC [3] filters and digitizes the output of the second SC amplifier stage. The ADC embeds a reconfigurable low-pass analog DT FIR/IIR filter within an SAR ADC. The filter oversamples the signal at the output rate of the SC amplifiers (i.e., 100 MS/s for a  $\approx 2$ -MHz signal bandwidth in prototype measurements), rejects aliases in the analog DT domain, and then decimates the rate by  $\approx 20\times$  for power-efficient 7-bit analog-to-digital (A/D) conversion. Fig. 5 shows the SARfilter ADC frequency response setting that we use for prototype measurements (Section IV).

## III. DT SS

Our proposed SS technique uses identical frequency-programmable analog DT bandpass spectrum-analysis filters in the I and Q channels and simple digital signal processor (DSP).

<sup>1</sup>After the six-tap FIR filter powers on or changes modes, it needs to sample for six cycles before it can output the first valid sample.

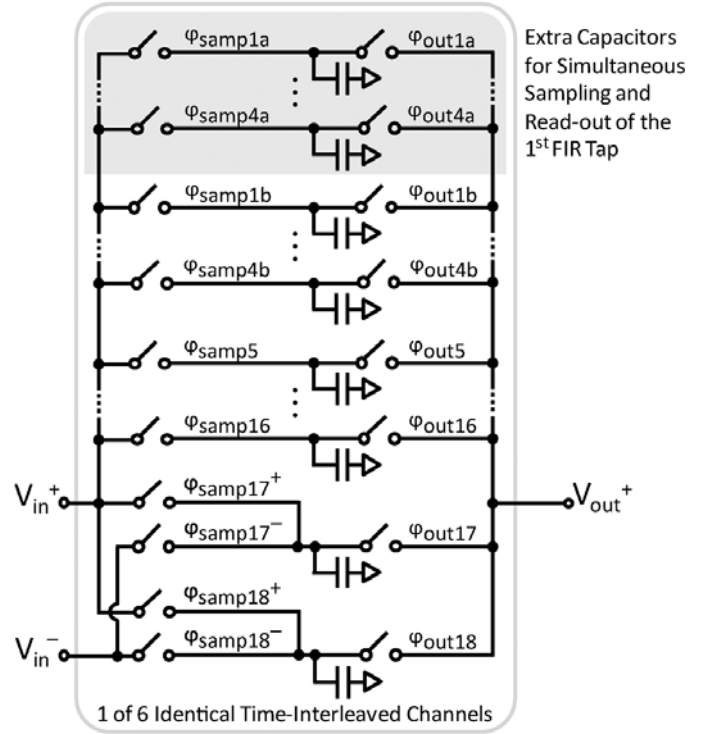


Fig. 4. Differential half-circuit schematic of the SS-guided reconfigurable DT FIR notch filter. The filter consists of six time-interleaved channels, each with 22 unit capacitors per half-circuit. Two capacitors connect to both  $V_{in}^{+/-}$  to implement negative coefficients and four capacitors are duplicated (gray background) for simultaneous sampling and read-out of the first FIR tap.

The spectrum-analysis filters isolate and subsample the interferer power within 12 equal bandwidth frequency bands at the output of the TIA buffer (Fig. 2). Analog DT spectrum-analysis filtering is simpler than digital filtering because it does not require high-speed high-resolution ADCs. Our analog DT filtering configuration also inherently rejects aliases by design (i.e., does not require a separate antialiasing filter). Analog DT filters [11], which consist of switches and capacitors (i.e., no op-amps), are also advantageous because switches function well in nanometer CMOS and the filter response is well defined by capacitor matching and clocking and independent of process variation.

### A. Bandpass Subsampling for Spectrum-Analysis

The I/Q DT spectrum-analysis filter in Fig. 2 performs bandpass subsampling, which refers to the process of sampling a high-frequency (i.e., IF or RF) bandpass signal at a sampling rate proportional to its passband bandwidth, instead of sampling at a rate proportional to its highest frequency. For a signal with bandwidth of less than  $B$  that is properly positioned in frequency [12], uniform sampling need only occur at a rate of  $2B$  to achieve alias-free signal down-conversion.

We adapt bandpass subsampling for interferer power detection in our analog DT spectrum-analysis filter. Since measuring the power of interferers does not require alias-free subsampling, we relax the bandwidth and frequency-positioning requirements. Fig. 6 shows a simplified diagram of an example spectrum of interest. The dark gray triangle represents an interferer signal of interest that lies within a power detection band

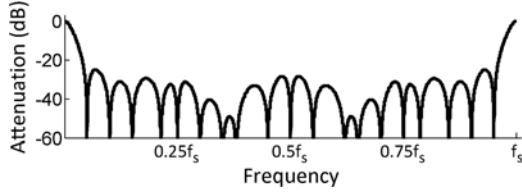


Fig. 5. Frequency response setting of the SARfilter ADC that prototype measurements use (Section IV).

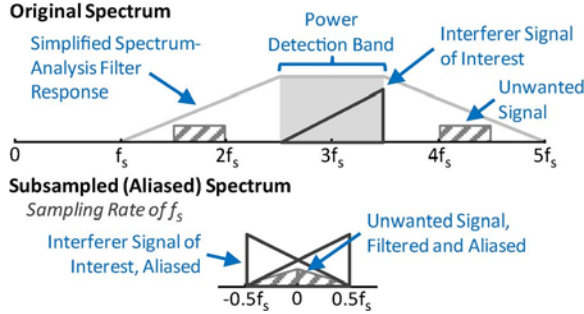


Fig. 6. Bandpass subsampling samples at a rate proportional to the signal’s passband bandwidth. A bandpass filter first attenuates the out-of-band signals before subsampling (*top*). The power of the sub-sampled spectrum (*bottom*) approximates the original signal well, even when aliasing occurs, as long as the filter adequately attenuates out-of-band signals.

ranging from  $2.5f_s$  to  $3.5f_s$ , within which we want to measure signal power. The striped bars represent unwanted signals outside of the detection band. In order to measure the power of the interferer signal of interest, we first attenuate signals outside of the detection band with a bandpass “spectrum-analysis filter” (light-gray line). We then subsample the signal at a rate of  $f_s$ , which causes the signal at higher frequencies to fold into the frequencies  $-0.5f_s$  to  $0.5f_s$ . Although subsampling aliases the interferer signal of interest and corrupts the signal’s content, it accurately down-converts the signal power to baseband. The partially attenuated unwanted signal also folds into the frequencies  $-0.5f_s$  to  $0.5f_s$  and introduces error in the measured power. This error is acceptable as long as the bandpass filter attenuates the power of the signals outside of the detection band to less than the minimum desired power measurement resolution.

### B. Calculation of Power from the Filter Output

The analog DT spectrum-analysis filter performs bandpass subsampling, so low-speed low-power A/D conversion and DSP are sufficient to calculate the average interferer power. The average power of the I and Q spectrum-analysis filter outputs,  $x_I[n]$  and  $x_Q[n]$ , is [13]

$$P_{\text{avg},N} = \frac{1}{N} \sum_{n=1}^N (x_I[n]^2 + x_Q[n]^2) \quad (1)$$

where we assume that  $x_{I/Q}[n] = 0$  for  $n \leq 0$  and that accumulating over a finite number of samples,  $N$ , can provide a good estimate of average power.

The necessary number of samples to accumulate depends on the modulation, bandwidth, and center frequency of the signals

contained within the power detection passband. If a signal is constant-envelope modulated (e.g., FM, minimum shift keying (MSK), etc.), has a bandwidth less than the bandwidth,  $B$ , of the spectrum-analysis filter, and has proper carrier frequency alignment relative to the subsampling rate to prevent aliasing, the complex envelope,  $e[n]$ , of the sub-sampled signal is constant and the  $P_{\text{avg}}$  calculation need only include one sample to be accurate. Otherwise,  $e[n]$  varies with time and  $P_{\text{avg}}$  should be calculated over a sufficient number of samples to average out the data dependent variation of the signal’s envelope (e.g., AM, quadrature amplitude modulation (QAM), etc.). We define  $\text{err}_P[N]$  to quantify the percentage error between  $P_{\text{avg},N}$  and  $P_{\text{avg}}$ , the average power as  $N \rightarrow \infty$ , as a function of  $N$

$$\text{err}_P[N] = \frac{|P_{\text{avg},N} - P_{\text{avg}}|}{P_{\text{avg}}} \times 100. \quad (2)$$

Fig. 7 illustrates the operation of the spectrum-analysis filter and the resulting  $\text{err}_P[N]$  for three different signals. The three rows plot MSK modulated signals with different bit rates and with aligned and offset center frequencies relative to a spectrum-analysis filter. (Section III-E describes the filter implementation.) Column (a) overlays the spectrum of these MSK signals (black) onto the frequency response of a bandpass spectrum-analysis filter (gray) with a subsampling rate of 5 MS/s and  $f_c$  of 20 MHz. The spectrum of the first two signals lies mostly within the filter’s bandwidth, but only the first of the two has a center frequency that allows subsampling to occur without aliasing. The spectrum of the third signal exceeds the filter’s bandwidth so the “skirts” of the signal alias onto the main lobe after subsampling. Column (b) plots the time-domain, bandpass filtered, and subsampled I and Q spectrum-analysis filter outputs and their complex envelopes,  $e[n]$ . Column (c) plots the 50th and 95th percentile boundaries of  $\text{err}_P[N]$  (2). Since  $e[n]$  of the first signal remains nearly constant and  $e[n]$  of the other two signals varies with time, the first signal requires fewer accumulated samples to achieve a low  $\text{err}_P[N]$ . These simulations demonstrate that SS based on DT bandpass subsampling and digital power calculation can achieve sufficient measurement accuracy for SA filtering of strong interferers.

### C. Digitally Controlled SS and Adaptive Filtering

A digital controller interprets the output of the spectrum-analysis filter and selects the optimal mode of an SS-guided reconfigurable notch filter (Fig. 2). A 4-bit  $\approx 5$ -MS/s<sup>2</sup> SAR ADC digitizes the bandpass filtered output in each of the I and Q channels of the filter (Fig. 9). The controller, which is clocked by an accurate external clock source, oversamples the ADC output to bridge the two clock domains, and then calculates  $N \cdot P_{\text{avg},N}$  (1), for selectable  $N \leq 64$ , to measure the average interferer power contained within each passband. It makes this measurement for every frequency bin from 15 to 70 MHz, in 5-MHz steps, as

<sup>2</sup>The sampling rate is approximate because the on-chip oscillator that clocks the ADC and spectrum-analysis filter is frequency calibrated, but not frequency locked, in order to eliminate the power that a PLL would otherwise consume. Section III-F below shows that the filter can tolerate clock jitter.

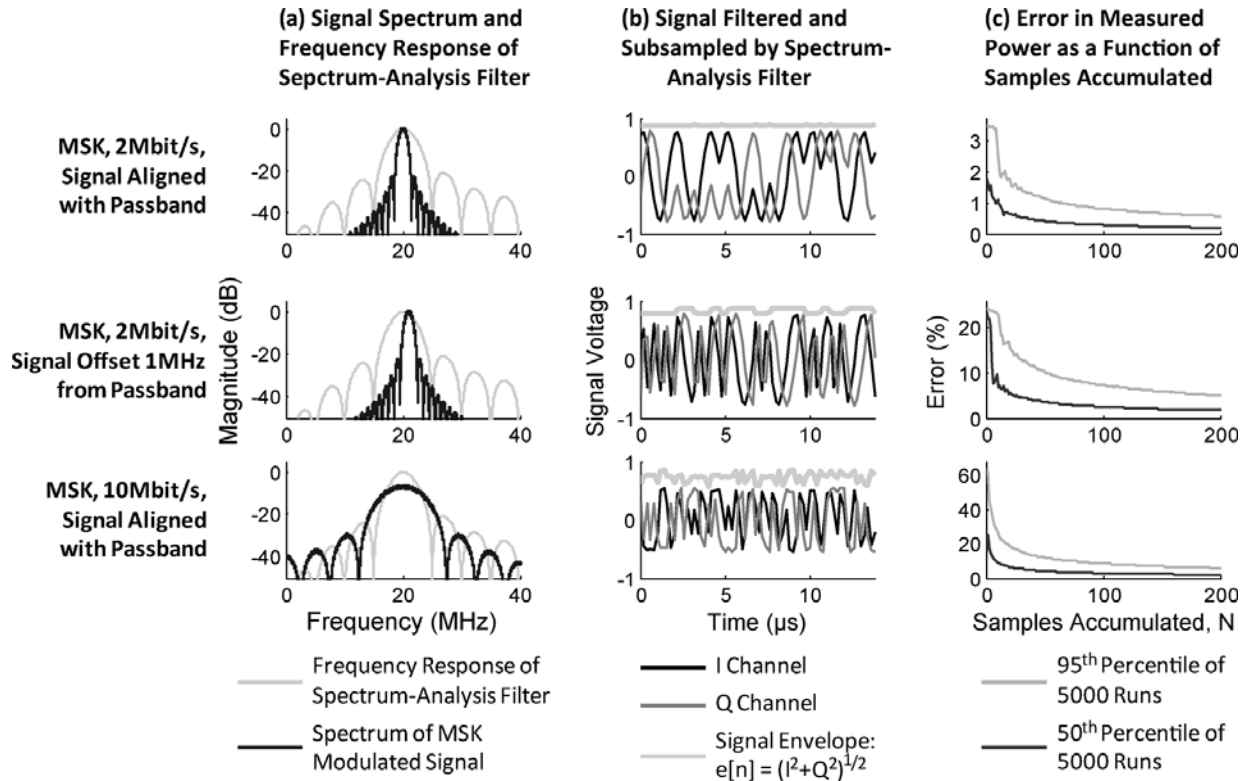


Fig. 7. Column (a) plots the IF spectrum of three different MSK modulated interferers (black) and the frequency response of the spectrum-analysis filter (gray) when its passband is centered at 20 MHz. Column (b) plots the filtered and sub-sampled I/Q signals at the output of the spectrum-analysis filter and their complex envelopes. Column (c) plots the 50th and 95th percentile boundaries of the error percentage (2) of the average measured signal power, as a function of the number of samples accumulated,  $N$ , over 5000 sets of randomized data in the MSK modulated interferer signal.

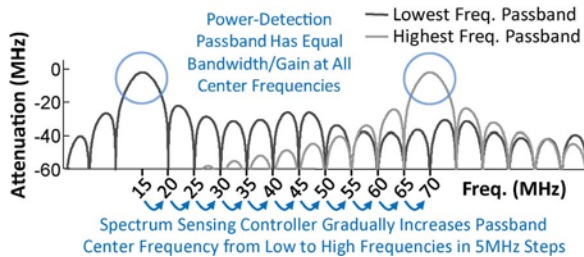


Fig. 8. Plots of the bandpass spectrum-analysis filter when configured to the lowest and highest center frequencies, 15 and 70 MHz, respectively. The digital controller adjusts filter parameters at each frequency so that bandwidth and gain remain constant.

shown in Fig. 8, and then directs the SS-guided notch filter to reject the interferer bin with the greatest measured power.

#### D. Accurate Frequency Tuning of the Spectrum-Analysis Filter

Our proposed DT spectrum-analysis filter achieves an easily and accurately tunable center frequency of the power detection passband,  $f_{PB}$ . The passband is always located at *one-tenth* of a clock frequency,  $f_{s,osc}$ , generated by an on-chip ring-oscillator (Fig. 2). This fixed relationship between  $f_{s,osc}$  and  $f_{PB}$  allows a digital SS controller to reliably control the passband center frequency by adjusting the ring-oscillator's frequency. Moreover, the oscillator frequency is accurately tunable by setting digital frequency-control bits on a 7-bit capacitive DAC (CDAC) that loads the oscillator. We calibrate the CDAC values that correspond to each desired oscillation frequency by measuring  $f_{s,osc}$  and storing the associated frequency-control bits into an on-chip

lookup table. Fig. 8 plots the frequency response of the spectrum-analysis filter when  $f_{PB}$  is set to its lowest and highest frequencies of 15 and 70 MHz, respectively. In order to perform SS across the 15–70-MHz band, the controller gradually increases  $f_{PB}$  in 5-MHz steps by increasing  $f_{s,osc}$ .

#### E. Creation of the DT Spectrum-Analysis Passband

Fig. 9 shows one of the identical I and Q branches of the four-stage DT spectrum-analysis filter and an example frequency response for each stage when  $f_{s,osc}$  is 250 MHz. The four filtering stages together generate notches and poles that create a distinct power detection passband centered at  $f_{PB} = 0.1 f_{s,osc}$ . Table I summarizes the sampling rate and frequency response of each stage. The  $G_m$  stage and the  $1\times$  and  $2\times$  gain “buffers” between the stages are simple open-loop differential pairs with source degeneration.

Fig. 10 plots the cascaded responses of the first three stages of the spectrum-analysis filter to emphasize how these stages create a distinct power detection passband at  $0.1 f_{s,osc}$ . The black line plots pole-zero cancellation between the second and third stages of Fig. 9, which creates a power detection passband at  $0.1 f_{s,osc}$  and unwanted passbands at  $n \cdot f_{s,osc} \pm 0.1 f_{s,osc}$ ,  $n = 1, 2, 3, \dots$ . Integration sampling in the first stage (Fig. 9), at a rate  $f_{s,osc}$ , creates notches at  $n \cdot f_{s,osc}$ ,  $n = 1, 2, 3, \dots$  (thick light-gray line) that attenuate the unwanted passbands. As a result, the cascade of the three filtering stages (medium-gray line) exhibits a sharp bandpass response centered at  $0.1 f_{s,osc}$ . Integration sampling requires resetting of  $C_{int}^{+/-}$  before sampling occurs and additional time to transfer the sampled charge to

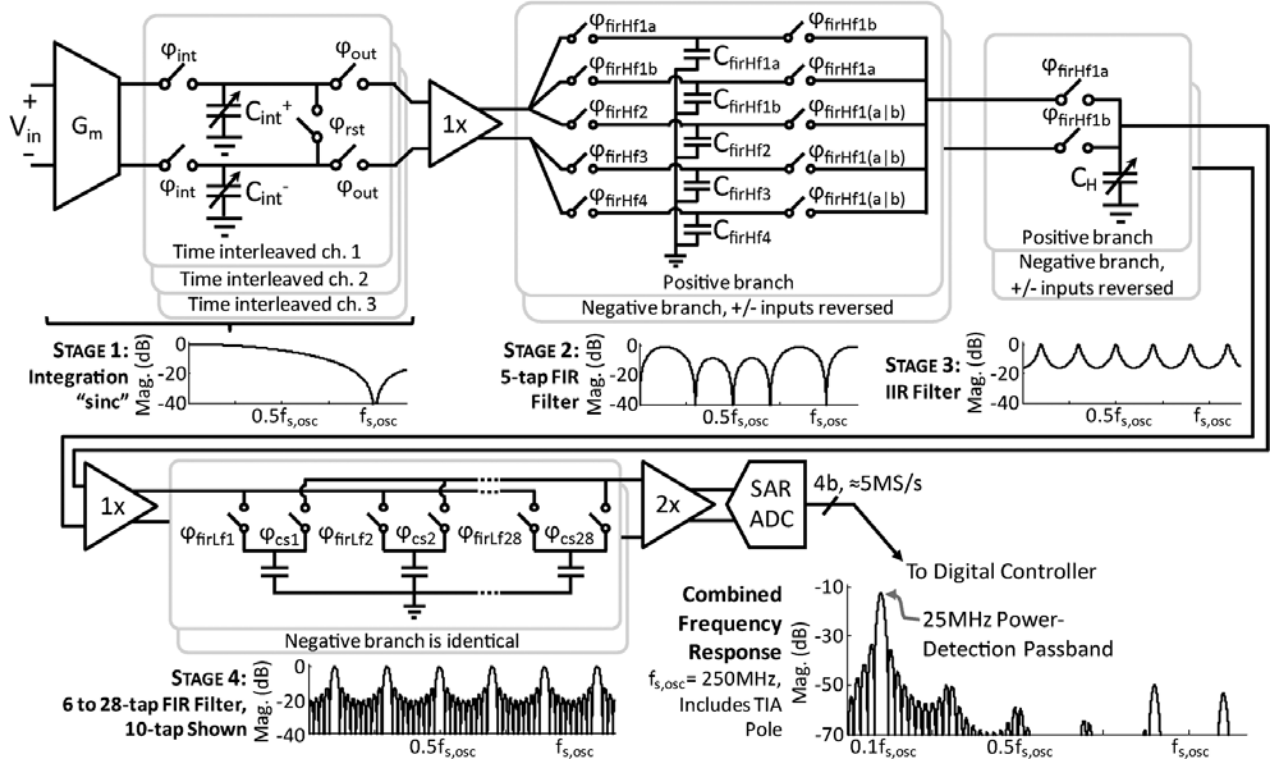


Fig. 9. One of the identical I and Q branches of the four-stage DT bandpass spectrum-analysis filter. The filter response of each stage is also shown. The combined response (lower right plot) shows that the spectrum-analysis filter and the TIA pole together create a distinct power detection passband.

TABLE I  
STAGES OF THE SPECTRUM-ANALYSIS FILTER

Stage	Rate In	Rate Out	Frequency Response
1	$f_s$	$f_s$	sinc-like, notches at $n \cdot f_s$ , $n=1,2,3\dots$
2	$f_s$	$f_s/5$	notches at DC, $0.3f_s$ , $0.5f_s$ , $0.7f_s$ , $f_s\dots$
3	$f_s/5$	$f_s/5$	poles at $0.1f_s$ , $0.3f_s$ , $0.5f_s\dots$
4	$f_s/5$	$f_s/140$ to $f_s/30$ , always $0.3f_s$ , $0.5f_s\dots$	notches at 0, 5, 10 MHz... except at $0.1f_s$ , $0.3f_s$ , $0.5f_s\dots$
Combined	$f_s$	$\approx 5$ MS/s	power detection passband at $f_s/10$

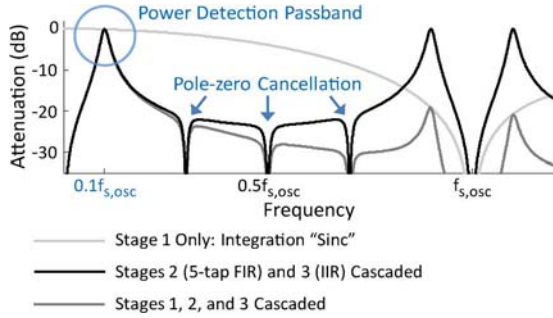


Fig. 10. Frequency responses of different combinations of the spectrum-analysis filter stages. Pole-zero cancellation between stages 2 and 3 create a power detection passband at  $0.1f_s$  and unwanted passbands at  $n \cdot f_{s,osc} \pm 0.1f_{s,osc}$ ,  $n = 1, 2, 3, \dots$ . The integration "sinc" of the first stage attenuates the undesirable passbands, as shown in the cascaded response of all three stages.

the capacitors of the following stage. Therefore, three identical channels are time-interleaved (Fig. 9) to permit simultaneous sampling, outputting, and resetting.

The FIR and IIR filters of the second and third stages, respectively, together implement the transfer function

$$H_{stg23}(z) = \frac{1}{1+x_{IIR}} (0.31 + 0.19z^{-1} - 0.19z^{-3} - 0.31z^{-4}) \cdot \frac{1}{1+x_{IIR}} z^{-5}$$

where

$$x_{IIR} = 11.86 \times 10^{-9} f_{s,osc} - 0.34. \quad (3)$$

The terms within the parentheses in the numerator correspond to the taps of the second stage of Fig. 9. The input is sampled onto capacitors  $C_{firHf1a/b}$  to  $C_{firHf4}$  over multiple clock periods, then charge-shared together to create a filtered sample of charge. Each of the  $C_{firHf}$  capacitors is sized in proportion to a corresponding filter tap coefficient. Negative coefficients in the FIR filter are implemented by sampling the negative input onto the positive half-circuit (and vice-versa). Sampling takes five clock cycles so this filter decimates the sampling rate by  $5 \times$ . The terms in the denominator of (3) represent the third stage IIR filter, which is implemented by connecting the IIR history capacitor,  $C_H$ , to the FIR capacitors when they charge-share. This combines a fraction of the FIR filter's present output sample with past output samples. The polarity of the connection between the two filters reverses in each subsequent charge-share to shift the pole locations from dc,  $0.2f_s$ ,  $0.4f_s, \dots$  to  $0.1f_s$ ,  $0.3f_s$ ,  $0.5f_s, \dots$

The output rate of the third stage varies because we adjust  $f_{s,osc}$  (i.e., the sampling rate of the first stage) to change the passband's center frequency. A low fixed rate at the output the spectrum-analysis filter would, however, enable power-efficient low-speed A/D conversion and digital power calculation. Therefore, we implement a variable rate FIR decimation filter in the fourth stage (Fig. 9) to reduce the sampling rate to  $\approx 5$  MS/s for all  $f_{s,osc}$ . This filter implements the transfer function

$$H_{stg4}(z) = \frac{1}{n_{tapFIRLf}} (1 + z^{-1} + z^{-2} + z^{-3} + \dots + z^{-(n_{tapFIRLf}-1)}) \quad (4)$$

where  $n_{\text{tapFIR}L_f}$  is the number of FIR taps and ranges from six taps for  $f_{s,\text{osc}}$  of 150 MHz (i.e., 15-MHz passband) to 28 taps for  $f_{s,\text{osc}}$  of 700 MHz (i.e., 70-MHz passband). For example, for  $f_{s,\text{osc}}$  of 250 MHz, shown in Fig. 9, the second stage decimates the rate  $5\times$ , from 250 to 50 MS/s, and the fourth stage decimates the rate an additional  $10\times$  in ten-tap mode, from 50 to 5 MS/s.

Stage 4 of Fig. 9 shows the frequency response of this filter when it is set to the  $10\times$  decimation, ten-tap mode.<sup>3</sup> Since the decimation filter's tap-length scales with  $f_{s,\text{osc}}$ , its passband lobe at  $f_{\text{PB}} = 0.1f_{s,\text{osc}}$  exhibits equal bandwidth for all  $f_{s,\text{osc}}$ . Furthermore, as  $f_{s,\text{osc}}$  (and  $f_{\text{PB}}$ ) increases, the controller decreases  $C_{\text{int}}^{+/-}$  in the first stage to keep the gain constant since the integration gain scales proportionally with the integration period. The controller also increases  $C_H$  in the third stage to keep the bandwidth constant since the IIR bandwidth scales proportionally with  $f_{s,\text{iir}} = f_{s,\text{osc}}/5$ . In the lower right corner of Fig. 9, a plot of the frequency response of the spectrum-analysis filter cascaded with the TIA (in the main signal path) shows that the combined attenuation strongly rejects all frequencies outside of the power detection passband.

#### F. Capacitor Mismatch and Sampling Jitter

The power detection passband of the spectrum-analysis filter exhibits little variation in its target gain, center frequency, and bandwidth in the presence of capacitor mismatch and sampling clock jitter. We see this robustness to mismatch and jitter in simulations of a simplified model of the filter.<sup>4</sup> Fig. 11 plots the frequency response of the spectrum-analysis filter for  $f_{s,\text{osc}}$  of 500 MHz and a greatly exaggerated capacitor mismatch of 0.05 and sampling clock jitter of 30 ps. The gray line plots the ideal frequency response and the dashed black line overlay the worst simulated attenuation at each frequency, when considering 50 different nonideal configurations. The power detection passband remains well defined, although nonidealities limit attenuation outside of the passband to  $\approx 50$  dB. Imperfect pole-zero cancellation at 150, 250, and 350 MHz results in 6–8 dB less attenuation than ideally possible.

Table II summarizes the effect of mismatch and jitter on the passband's gain, center frequency, and bandwidth, simulated over 500 different configurations for each mismatch and jitter combination. Mismatch and jitter negligibly effect the definition of the passband because the frequency of the calibrated on-chip ring-oscillator (i.e.,  $f_{s,\text{osc}}$ ) sets the passband center frequency and because mismatch and jitter most significantly affects the frequency and the depth of the FIR filter zeros. Therefore, changes to the frequency response occur close to those zeros and far from the passband.

<sup>3</sup>The frequency response shown for the fourth stage in Fig. 9 is bandpass with passbands at  $f_{s,\text{iir}}/2 = 0.1f_{s,\text{osc}}$ , but (4) describes a low-pass FIR filter. Alternating reversals of the sampling polarity in the third-stage IIR filter is equivalent to multiplying by  $e^{j\pi n} = \{-1, 1, -1, 1, \dots\}$ , which frequency shifts the signal by  $\pi = f_{s,\text{iir}}/2$ .

<sup>4</sup>The model makes the following simplifications. It: 1) omits the effect of time interleaving and instead assumes that outputting and resetting happens instantaneously; 2) omits sampling nonidealities aside from jitter; and 3) applies the stated mismatch to each capacitor shown in Fig. 9, regardless of size.

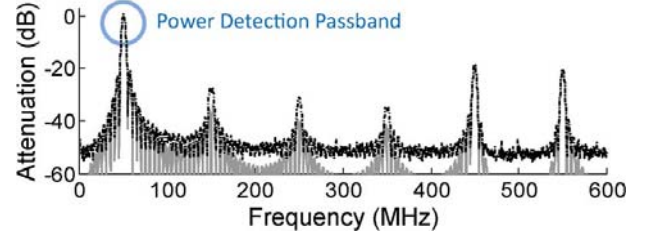


Fig. 11. Frequency response of the spectrum-analysis filter set to a center frequency of 50 MHz. The gray line plots the ideal response and the black dashed line overlays the worst simulated attenuation at each frequency, when considering 50 different nonideal configurations with  $\sigma_{\Delta C/C} = 0.05$  and  $\sigma_{\text{jitter}} = 30$  ps. The power detection remains well defined in the presence of nonidealities.

TABLE II  
EFFECTS OF MISMATCH AND JITTER ON THE SPECTRUM-ANALYSIS FILTER, SIMULATED OVER 500 RUNS

Controlled Variables		Result on the Power Detection Passband		
Capacitor Mismatch: $\sigma$ ( $\Delta C/C$ )	Sampling Jitter: $\sigma$ (ps)	Normalized Passband Gain: $\sigma$	Center Freq.: mean (MHz) and $\sigma$ (kHz)	-3 dB BW: mean (MHz) and $\sigma$ (kHz)
.01	0	0.0072	50.0375/0	3.2620/10.8
.05	0	0.0360	50.0364/2.2	3.2587/52.2
.1	0	0.0683	50.0358/3.2	3.2528/102.0
0	10	0.0001	50.0373/18.5	3.2597/2.8
0	30	0.0003	50.0462/32.5	3.2569/4.3
0	50	0.0005	50.0496/43.4	3.2527/6.6
.05	30	0.0336	50.0428/33.7	3.2514/49.4

#### IV. MEASURED PERFORMANCE

The prototype direct-conversion SS receiver is implemented in 65-nm CMOS. Fig. 12 shows a photograph of the die in which active circuitry occupies  $0.39 \text{ mm}^2$ . The prototype achieves 55.8-dB gain and supports carrier frequencies from 600 MHz to 3.4 GHz. Fig. 13 plots the combined frequency response of the receiver, which includes the TIA pole; the SS-guided filter when it is enabled in four different modes (Fig. 3 and Table III), overlaid when it is disabled; and the SARfilter ADC. The combined filter achieves  $>52$ -dB attenuation in the target frequency bands of all four SS-guided filter modes.<sup>5</sup>

In packet tests compliant to IEEE 802.15.4, we stimulate the receiver with RF packets and identify the power level that achieves 1% packet error rate (PER). As summarized in Table III, the receiver exceeds the sensitivity and interferer rejection requirements for both the 2450- and 915-MHz bands. Fig. 14 plots the measured minimum required power of an FM modulated interferer to activate the different SA filtering modes and shows that the controller sets the correct mode at all center frequencies. The power levels resemble inverted frequency responses of the SS power detection band (Fig. 8). The measured passbands are narrower than the ideal passbands because parasitic routing capacitances enlarge the effective size of the IIR capacitor ( $C_H$  in Fig. 9). Higher interferer power is also necessary to activate the filter at higher frequencies

<sup>5</sup>The SS-guided filter achieves limited notch depth because the unit capacitor cells within the filter use individually boot-strapped sampling switches [15] that occupy a large area (approximately  $10 \mu\text{m}$  by  $7 \mu\text{m}$ ), which results in routing nonidealities that limit sampling and charge-sharing accuracy. It is possible to eliminate this limitation by reducing the gain of the LNA and TIA, which would make boot-strapped sampling unnecessary and make the filter's area  $5\times$ – $8\times$  smaller.

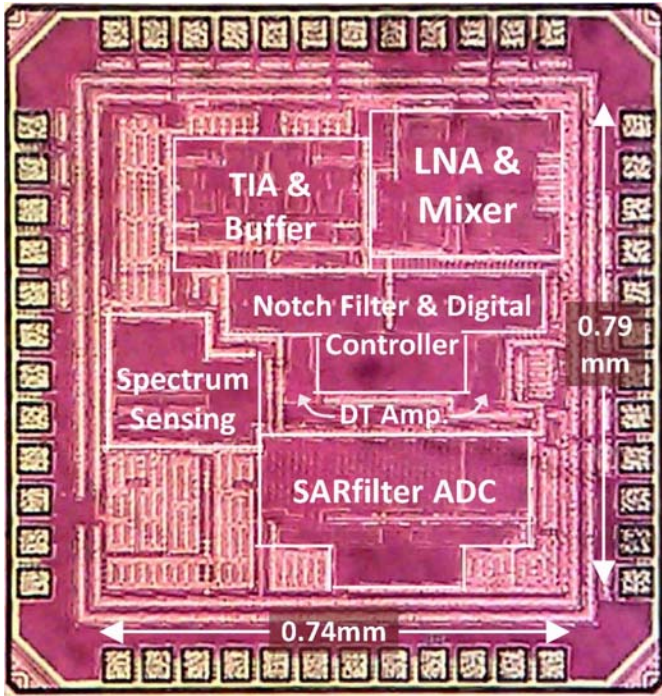


Fig. 12. Die photograph of the 65-nm CMOS prototype receiver.

TABLE III  
SUMMARY OF PARAMETERS AND MEASUREMENTS

Technology	65nm 1P9M w/MIMCAP	
Active Area	0.39 mm <sup>2</sup>	
Carrier Frequency Range	600 MHz to 3.4 GHz	
Max Gain	55.8 dB	
IIP3	-38 dBm	
SS Sweep Duration	≈121 μs for 25 to 65 MHz sweep, 64 samples per bin	
SS-Guided Notch Filter Mode, FIR Coefficients, and Target Attenuation Bands	1: [4 -1 4 4 -1 4], 15-23 MHz 2: [2 2 4 4 2 2], 23-28 MHz 3: [1 3 5 3 1], 28-42 MHz & 58-70 MHz 4: [1 3 4 4 3 1], 42 to 58 MHz	
SARfilter ADC FIR Filter	Tap Length: 16 to 64, Weight: 0 to 6C <sub>unit</sub>	
Power, 1.0 V Except for 0.9 V Digital	Analog	6.82 mW
	Digital: Controller, Notch Filter & SARfilter ADC	3.41 mW, $f_{conv}=5$ MS/s, 20-tap SARfilter ADC FIR filter
	Clocks	1.31 mW, $f_{conv}=2$ MS/s, 16-tap SARfilter ADC FIR filter
	LO Divider	1.94 mW, 4.8 GHz $2x_{f_{LO}}$
	Spectrum Sensing	0.90 mW, 1.8 GHz $2x_{f_{LO}}$
IEEE 802.15.4 Sensitivity & Interferer Rejection	2450 MHz, $f_{conv}=5$ MS/s	-93 dBm
	915 MHz, $f_{conv}=2$ MS/s	+5 MHz, +30 dB; +10 MHz, +39 dB
		-100 dBm
		+2 MHz, +29 dB; +4 MHz, +31 dB

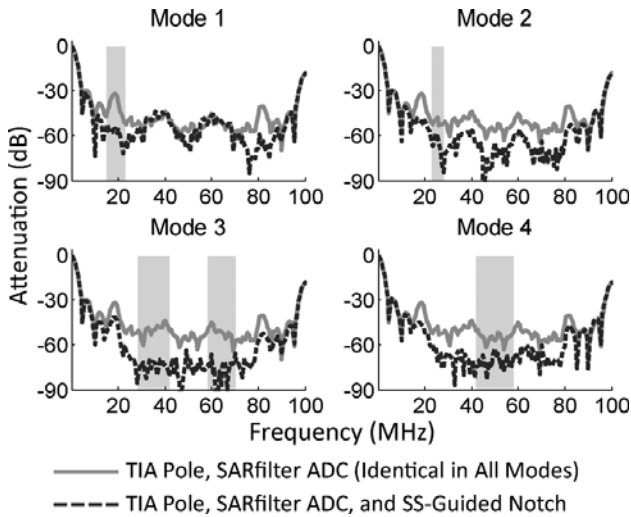


Fig. 13. Measured combined frequency responses of the receiver, which includes the TIA pole, SARfilter ADC, and SS-guided notch filter. The gray shaded areas indicate the frequencies targeted by each SS-guided filter mode.

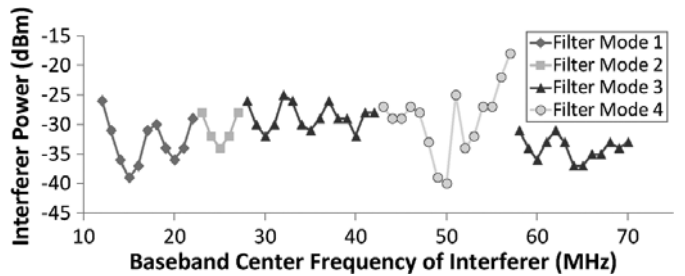


Fig. 14. Measured minimum power of an FM interferer (1-MHz deviation, 50-kHz rate) that activates the four modes of the SA filter. The power levels resemble inverted power detection passband frequency responses (Fig. 8).

because the TIA pole and a parasitic DT IIR filter at the output of the  $G_m$  stage in the SS filter attenuates the interferer.<sup>6</sup> The reduction of interferer power above  $\approx 50$  MHz does not occur in measurements made using other dies.

In SA filtering tests using IEEE 802.15.4 packets (Fig. 15), the receiver achieves from +55- to +63-dB rejection from a +25- to +65-MHz FM interferer when SA filtering is enabled, which averages to 9.4 dB more rejection compared to when SA

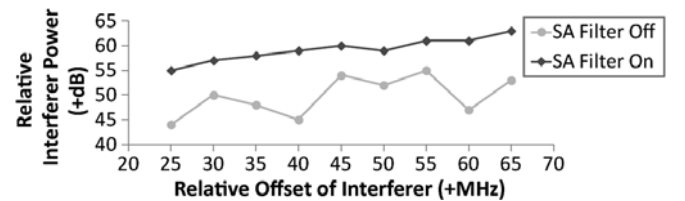


Fig. 15. Measured relative power versus frequency offset of an FM interferer (1-MHz deviation, 50-kHz rate) at which the receiver achieves 1% PER when receiving  $-85$ -dBm RF modulated IEEE 802.15.4 2450-MHz band packets. The TIA pole and SARfilter ADC are active in both the SA filter on and off cases. SA filtering improves interferer rejection by an average of 9.4 dB.

filtering is disabled.<sup>7</sup> SA filtering achieves this improvement by detecting the FM interferer and reconfiguring the SS-guided notch filter to the mode that best attenuates the interferer.

<sup>6</sup>Time and resource limitations prevented us from improving the layout based on post-layout simulations. These nonidealities do not limit the implementation of analog DT SS.

<sup>7</sup>When SA filtering is enabled, the power levels of the interferer ( $-85$  dBm +  $>55$  dB) cause it to saturate the output of the TIA and limit interferer rejection.

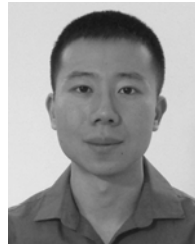


## V. CONCLUSION

We demonstrate a flexible wireless receiver that uses intelligent DT SA filtering to attenuate strong interferers. In this adaptive-filtering system, an analog DT spectrum-analyzer detects strong interferers, and then a digital controller automatically adjusts a configurable filter to the mode that most strongly attenuates these interferers. SA filtering reduces the need to overdesign a receiver for worst case operating conditions by sensing the receiver's operating environment.

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