A Flexible 500 MHz to 3.6 GHz Wireless Receiver with Configurable DT FIR and IIR Filter Embedded in a 7b 21 MS/s SAR ADC

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***Abstract*—A flexible, software-configurable wireless receiver is implemented in 65 nm CMOS. The receive chain consists of wideband LNA and mixer, baseband amplifiers, and a 7-bit 21 MS/s filtering SAR ADC. This filtering ADC embeds a highly-integrated and configurable DT FIR/IIR filter to replace dedicated filtering stages. The tap length and coefficients of the embedded FIR filter are configurable from 16 to 64 taps and 0 to 6 units, respectively. Interleaving of the SAR and DT filter sampling processes in the ADC maximizes the conversion rate and facilitates IIR filtering. The prototype receiver supports several standards and bands. In packet tests, the prototype exceeds the sensitivity and jammer resistance requirements of both the 915 MHz and 2450 MHz bands of IEEE 802.15.4 while consuming 4.0 mW and 5.5 mW, respectively. The receiver is also demonstrated with the DSSS specification of IEEE 802.11.**

***Index Terms*—Analog discrete-time filter, configurable filter, SAR ADC, wireless receiver.**

I. Introduction

MODERN wireless devices must operate with an ever increasing number of communication standards and bands. Wireless receivers that use a narrowband front-end and continuous-time (CT) analog filters [1], [2] perform well for the standards that they target, but cannot easily adapt to multiple standards. The performance of a narrowband front-end degrades outside of the frequencies for which it is designed. CT baseband filters do not scale well with process, are difficult to reconfigure, and are sensitive to process mismatch. The rapidly changing wireless communication landscape makes such rigid design approaches undesirable. At the same time, there exists a need for receiver architectures that take advantage of nanometer digital CMOS processes. This work introduces a receiver architecture based on a modified SAR ADC that achieves both digitization and reconfigurable, robust, and scaling-friendly filtering. This filtering ADC replaces the separate filters and ADC of a conventional receiver and enables the creation of a highly-integrated flexible wireless receiver.

Over the last decade, research has led to several techniques to enable software-defined radios (SDR). Many of these techniques are based on analog discrete-time (DT) finite impulse response (FIR) and infinite impulse response (IIR) filters that are implemented by sampling an input signal onto capacitors and then manipulating the stored charge. These charge-domain filters have been explored for a wide variety of uses and for many different wireless standards. In [3] and [4], integration of the signal current onto I and Q capacitors over multiple clock cycles, together with charge-sharing with history capacitors, implements a sub-sampler with a complex band-pass response. [5] discusses an RF sampling Bluetooth receiver, in which analog DT filters decimate an initially high sampling rate. In order to take advantage of both simple analog CT and DT filters, [6] proposes down-converting IEEE 802.11g and GSM signals to baseband and then filtering with simple analog filters before applying analog DT filtering. Other SDR innovations complement analog DT techniques, such as a highly linear front-end with tunable analog filters [7] and RF/IF bandpass filtering using frequency-translated baseband impedances [8]. We improve on existing analog DT filtering techniques by introducing a more integrated, more area-efficient, and more power-efficient DT filtering architecture.

We propose a flexible wireless receiver architecture based on a modified SAR ADC that achieves both filtering and digitization. A prototype of this architecture, implemented in 65 nm CMOS, consists of a wideband front-end, simple baseband amplifiers, and a reconfigurable analog DT filter that is embedded *within* a SAR ADC to create a unique "SARfilter ADC." The embedded DT filter uniquely reuses the capacitors in the capacitive DAC (CDAC) of a SAR ADC to achieve flexible filtering and eliminates the need for complicated CT baseband filters. This new approach leads to excellent scalability and conversion efficiency because a SAR ADC consists of scaling-friendly switches, capacitors, and a comparator [9], [10]. The embedded DT filter is also robust to process variation because relative, not absolute, capacitor values define the frequency response. Simulations also show that the filter is robust to mismatch and jitter. Compared to the use of separate DT filtering stages, the embedded DT filter eliminates the resampling of charge from the

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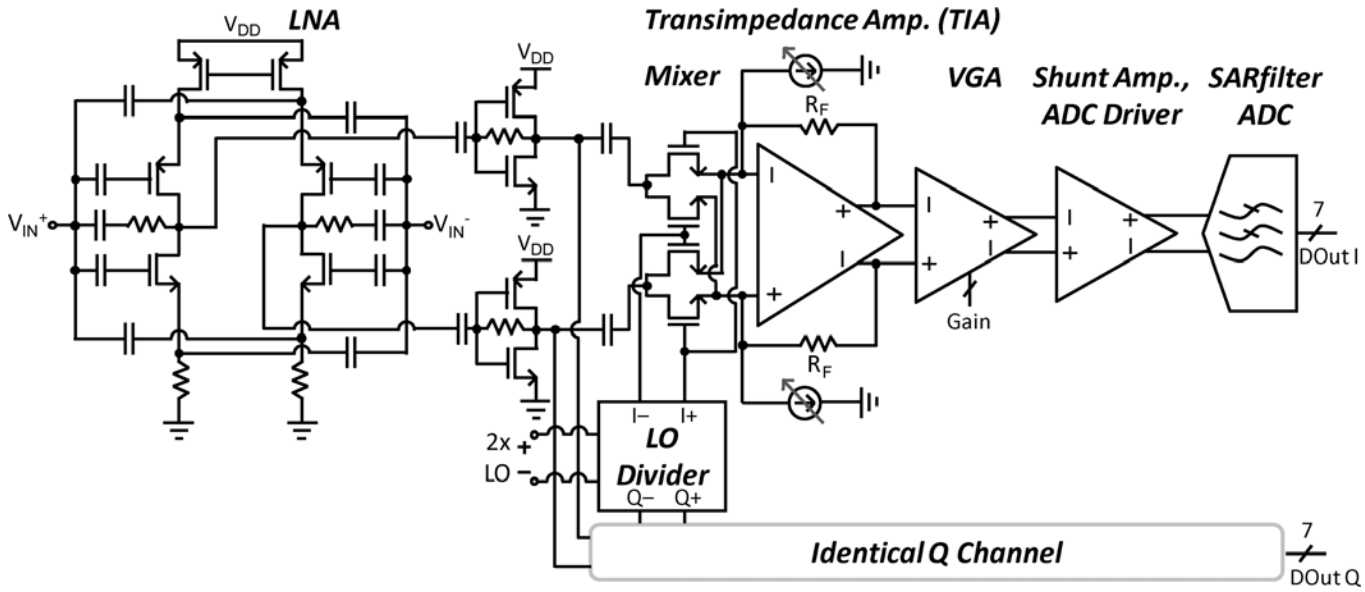

Fig. 1. Diagram of the SARfilter ADC receiver, consisting of a wideband front-end, 2× LO divider, simple baseband amplifiers, and SAR ADCs with embedded configurable DT filtering.

filtering capacitors to the ADC and the associated resampling noise and power consumption of a buffer. This configurable SARfilter ADC receiver supports carrier frequencies ranging from 500 MHz to 3.6 GHz and functions with multiple communication standards and bands by adjusting the sampling rate and the DT filter parameters. The performance of the prototype receiver is verified with packets compliant to the 915 MHz and 2450 MHz bands of the IEEE 802.15.4 standard and the 2.4 GHz DSSS specification of the IEEE 802.11 standard.

Section II below describes the architecture of the overall receiver that incorporates the SARfilter ADC. Section III describes the benefits and implementation of the DT filter embedded within the SARfilter ADC, the interleaving of sampling and SAR operations, and the conversion rate, mismatch, jitter, and noise implications of the architecture. Section IV presents the measured performance and the results of packet testing.

II. Receiver Architecture

The prototype receiver consists of direct conversion I and Q channels with individual SARfilter ADCs, which perform most of the required filtering. A wideband LNA drives a current-switching mixer, after which a chain of amplifiers amplifies the down-converted signal. A 7-bit SAR ADC filters and digitizes the output with an embedded, software-configurable analog DT filter that reuses the capacitive DAC (CDAC) of the SAR ADC to implement FIR and IIR filtering. The embedded filter achieves more than 30 dB of interferer attenuation, even at small frequency offsets from the wanted signal, which simplifies the baseband amplifiers and requires that these amplifiers only provide attenuation at higher frequencies.

Fig. 1 shows the receiver architecture [11]. No inductors are used, in order to support a wide range of carrier frequencies, to minimize circuit area, and to maintain compatibility with digital CMOS processes. The wideband LNA [12] with differential inputs, each matched to 50 Ω, achieves low-power and wideband operation by connecting two common-gate and two shunt feedback stages in parallel. Self-biased inverters buffer the output of the LNA and sink current through a passive switching NMOS mixer into a transimpedance amplifier (TIA). The use of a passive mixer minimizes flicker noise and second order non-linearity [6], [13]. A 2× LO divider [14] drives the mixers with non-overlapping, differential I/Q 25% duty-cycle LO clocks from a differential 2× LO clock input. Self-mixing of the LO signal and device mismatch in the front-end and baseband amplifiers can create a DC offset. Binary weighted current DACs generate counteracting voltages by sourcing current through the feedback resistors, R_F, of the TIA. The output of the TIA first enters a variable gain amplifier (VGA) with a five-level digitally-controlled load resistance, which enables the gain to span a range of 25 dB. The VGA output drives a shunt-connected amplifier and a pseudo-differential ADC driver. The two lowest poles of the amplifiers are set at approximately 6 MHz by the TIA and at 30 MHz by the shunt amplifier after the VGA.

The 7-bit SARfilter ADC attenuates interferers by more than 30 dB *before* A/D conversion, by introducing an embedded reconfigurable analog DT filter with both FIR notches and an IIR pole at DC. The filter implementation makes use of interleaved sampling and SAR conversion processes, in order to increase the ADC conversion rate and to ensure that the FIR filter generates enough notches to coincide with all multiples of the conversion rate. These notches strongly reject interferers that would otherwise fold onto a wanted signal at DC. The low frequency attenuation that this embedded DT filter provides greatly relaxes the attenuation required of the amplifiers that precede the SARfilter ADC. The following section describes the SARfilter ADC in-depth.

III. The SARfilter ADC

We replace conventional baseband filtering with a SAR ADC with embedded analog DT filtering, which more efficiently uses

area and power than separate DT filtering and ADC stages, functions well in scaled processes, and easily reconfigures. The SAR ADC architecture is well suited to implementing a DT filter, because the capacitive DAC (CDAC) that performs iterative A/D conversion already contains capacitors and switches, which are the key components of an analog DT filter. The simple switch and capacitor implementation allows power consumption, sampling rate, and area usage to benefit from process scaling. The frequency response of the DT filter is easily configurable by modifying the sampling rate and the digital that drives the sampling switches. The DT filtering operation occurs *before* the SAR conversion process, so unlike a digital domain filter, this filter does not suffer from quantization error and can perform anti-aliasing. The following sections explain analog DT FIR and IIR filtering and also how these filters are embedded into a SAR ADC.

A. Benefits of Embedded Filtering

Embedding of the DT filter into the SAR ADC generally decreases capacitor area and power consumption compared to separate DT filtering and SAR ADC stages. A separated implementation eliminates the need to duplicate half of the CDAC in the ADC for interleaved sampling and SAR processes (Section III-F below), but instead requires a bank of dedicated capacitors for the filter. If the capacitors are sized in the noise-limited range, the total capacitor area of the separated implementation increases, because both banks need to achieve noise less than the noise threshold *and* compensate for the noise that resampling from the filter to the ADC adds. If the capacitors are sized in the mismatch-limited range, then either implementation can be more area efficient depending on the desired accuracy of the filter's frequency response.

The other drawbacks of the separated implementation depend on how the filter transfers charge to the ADC—buffer and resample, reset and charge-share, or charge-share only. The first case uses a buffer between the filter and the ADC; the buffer consumes power and adds noise. The second case resets the capacitors in the ADC before charge-sharing the capacitors in the filter and the ADC, which results in voltage attenuation. The third case charge-shares the capacitors in the filter and the ADC, which implements an undesirable DT IIR filter (similar to Section III-D below). Unlike the proposed IIR filter (Fig. 9), the poles of this filter repeat at multiples of ADC conversion rate and greatly attenuate in-band frequencies if the total capacitance of the ADC exceeds the total capacitance of the filter. Therefore, the filter's capacitance should be greater than the ADC's capacitance, which increases the filter's area and the power consumption of the stage that drives it.

B. Charge-Sharing to Create Analog DT Filters

The fundamental operation in an analog DT filter is the sharing of sampled charge. A simple example, shown in Fig. 2, quantifies the charge and voltage when two capacitors, C_a and C_b, sample V_{in} at times a and b, respectively, and then share charge. When the capacitors are shorted together, the resulting voltage on the combined capacitors is

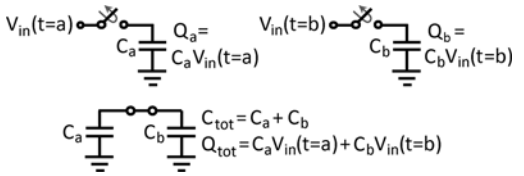

Fig. 2. Sampling of V_{in} at times $t = a$ and $t = b$ onto C_a and C_b, respectively, and subsequent charge-sharing of C_a and C_b result in a weighted sum of the inputs.

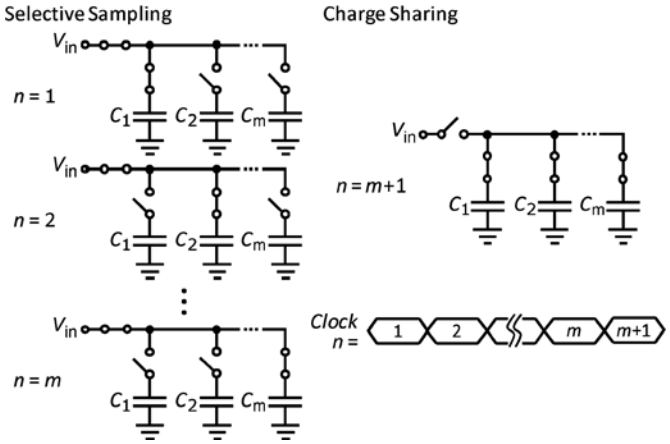

Fig. 3. The DT filter response is created by selectively-sampling onto the SAR ADC capacitors over multiple cycles and then charge sharing before SAR ADC conversion.

$$V_{out} = \frac{c_a}{c_a + c_b} V_{in}(t = a) + \frac{c_b}{c_a + c_b} V_{in}(t = b). \qquad (1)$$

V_{out} is a weighted sum of the sampled inputs, which suggests that sampling and charge-sharing can perform the delay, scaling, and summation operations that are necessary to implement a DT filter.

C. DT FIR Filter

To create an embedded DT FIR filter, we sample onto sections of the CDAC array of a SAR ADC over multiple clock cycles and then charge-share the DAC capacitors [15]. For example, Fig. 3 shows that for an m-tap FIR filter, we first divide the CDAC into m capacitor groups. Then the input signal is sampled onto each of the m groups over m clock cycles. Since this multi-cycle selective sampling process stores charge proportional to the input onto each group of capacitors, each group represents an FIR filter tap. Therefore, we set the size of each FIR filter tap coefficient by scaling the relative size of each capacitor group.[1] Finally, we short the capacitors together in the $m + 1$ clock cycle to average the stored charge and generate an FIR filtered sample of charge. The conventional SAR algorithm then uses the CDAC to perform a 7-bit binary search to digitize this filtered charge sample.

[1]Negative FIR coefficients can be easily implemented in a differential analog DT filter by reversing the polarity of the input. Although the SARfilter ADC prototype is differential, it does not implement negative coefficients.

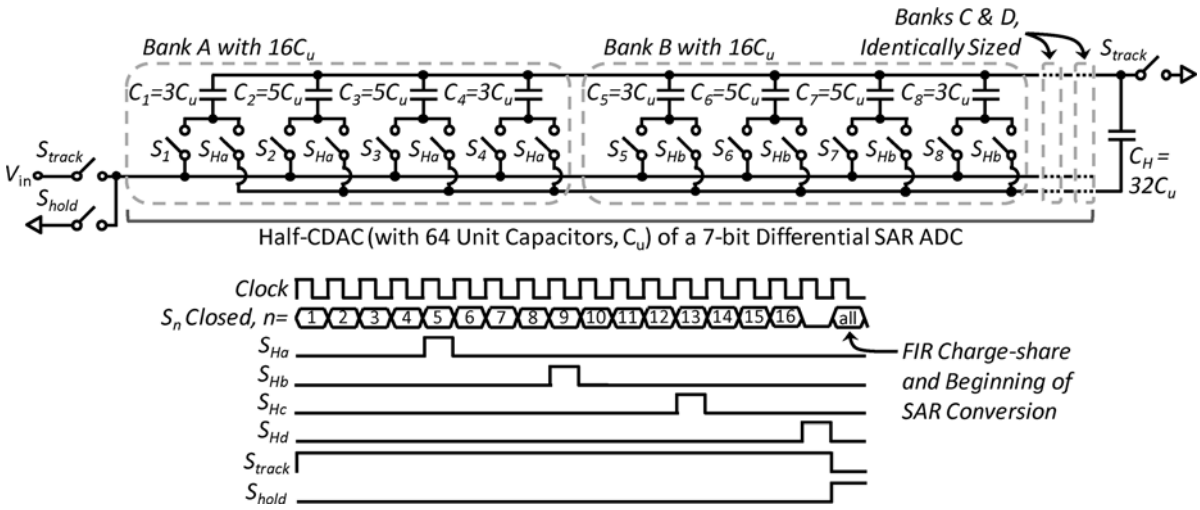

Fig. 4. Schematic and timing diagram of the SARfilter ADC differential half-CDAC setup that implements the DT filter described by (3). After every capacitor subgroup within a bank samples the input through the switches S_n, the bank charge-shares with C_H through S_H while the first subgroup in the next bank samples the input. Once all of the capacitors sample the input and charge-share with C_H, S_{hold} and all of the S_n switches close to charge-share all of the sampling capacitors and generate a single filtered output for SAR A/D conversion. The filtering operations in the other half-CDAC are identical.

D. DT IIR Filter

We add a history capacitor, C_H, that is never reset, to the CDAC to implement an IIR filter. We begin by considering the simplest form of IIR filtering (i.e. not combined with FIR filtering), where we first sample a voltage, V_{in}, onto the entire CDAC capacitance, C_S, and then charge-sharing C_S with C_H. When this sampling and charge-sharing process is repeated, the resulting charge on C_S is IIR filtered because charge-sharing with C_H adds a decreasing fraction of the previous samples to the current sample. The voltage, V_{out}, and frequency response, $H(z)$, that correspond to the filtered charge on the n^{th} clock period is described as follows:

$$\begin{aligned} V_{out}(n) &= r_s V_{in}(n) + r_H V_{out}(n-1), \text{ where} \\ r_s &= \frac{c_s}{c_s + c_H}, r_H = \frac{c_H}{c_s + c_H} \text{ and} \\ H(z) &= \frac{V_{out}(z)}{V_{in}(z)} = \frac{r_s}{1 - r_H z^{-1}}. \end{aligned} \tag{2}$$

Eq. (2) shows that charge-sharing with C_H creates a pole at DC and the distance of the pole from the unit circle depends on the relative sizes of C_S and C_H. A relatively larger C_H compared to C_S results in a sharper pole. Because this is a DT filter, the pole repeats at integer frequency multiples of the rate at which C_S is charge-shared with C_H, $f_{s,filterIIR}$.

E. Constraints on DT Filtering Configuration

The IIR response described by (2) is correct only if the ratios r_H and r_S remain constant during every charge-share, which means that the size of C_S must remain fixed. This is always true for the previously described simple IIR example. But when we combine IIR filtering with the selective-sampling process of an FIR filter, we must configure the filter coefficients to ensure a constant C_S. We clarify this point with the following example, in which we explain how to implement the filter described by (3) in a 7-bit SAR ADC, with the schematic and timing diagram shown in Fig. 4.

$$\begin{aligned} H(z) &= \frac{\frac{1}{192}(b_1 z^{-16} + b_2 z^{-15} + \ldots + b_{16} z^{-1})}{1 - \frac{2}{3} z^{-4}} \\ [b_1 b_2 b_3 b4] &= [b_5 b_6 b_7 b_8] = [b_9 b_{10} b_{11} b_{12}] \\ &= [b_{13} b_{14} b_{15} b_{16}] = [3\ 5\ 5\ 3] \end{aligned} \tag{3}$$

The 16-tap FIR component of this DT filter, with repeating coefficients [3 5 5 3], is one of many FIR filters that the reconfigurable SARfilter ADC can implement.

The following description explains the setup of the CDAC array to implement the example and the timing of the switches. Fig. 4 shows a $32C_u$ history capacitor, C_H, on the right side of the schematic and the 64 unit capacitors, C_u, in the differential half-CDAC of a 7-bit differential SAR ADC that need to be sampled onto before SAR conversion. To implement FIR filtering, we first divide these 64 capacitors into four banks of $16C_u$ each (i.e. banks A, B, C, and D in Fig. 4), which gives us more flexibility to choose the FIR filter coefficients. This is because each entire $16C_u$ bank is equivalent to C_S in the simple IIR example described by (2), in the sense that each bank is charge-shared in turn with C_H to implement the IIR filter. The capacitors within each $16C_u$ bank are further divided into subgroups that correspond to the repeating FIR tap coefficients [3, 5, 5, 3] in (3), because each bank must implement the same FIR filter when it is charge-shared with C_H.[2] In this way, charge-sharing an entire $16C_u$ bank with C_H keeps C_S constant, as required for IIR filtering, but the tap coefficients within the bank can be unequal (e.g. 3 and 5 above). Selective sampling of V_{in} onto the subgroups of bank A, through switches S_1, S_2, S_3, and S_4 in Fig. 4, implements the first four taps of the 16-tap FIR filter. These four samples then charge-share with C_H through switches S_{Ha} to implement the IIR filter response,

[2]This DT filtering example can be viewed as a cascade of 4-tap FIR filtering with coefficients [3 5 5 3], then IIR filtering, and then 4-tap FIR filtering with coefficients [1 1 1 1]. Therefore, each bank must have the same filter coefficients in order to correctly implement the first filter in the cascade.

while selective-sampling onto bank B through switch S_5 happens at the same time. After this selective-sampling and IIR charge-sharing process occurs for all four banks (A, B, C, and D), these banks charge-share through switches $S_1 - S_{64}$ to combine the filtered samples of charge on the four banks into a single sample. The conventional SAR ADC algorithm then digitizes this combined sample.

In the analog DT filtering process described above, the IIR filtering rate differs from the FIR filtering rate, $f_{s,filterFIR}$. As before, the lowest frequency pole of the IIR filter is located at DC and the poles of this DT filter repeat every 2π; that is, at integer frequency multiples of the rate at which C_S charge-shares with C_H, $f_{s,filterIIR}$. Eq. (4) describes $f_{s,filterIIR}$, where m is the number of selective samples that is collected before charge-sharing with C_H.

$$f_{s,filterIIR} = \frac{f_{s,filterFIR}}{m} \tag{4}$$

In the example above, charge-sharing with C_H occurs after every 4th sample, which results in a DT IIR pole that repeats every $f_{s,filterIIR} = f_{s,filterFIR}/4$ and is represented by the z^{-4} term in the denominator of (3).

F. Interleaved Sampling

We introduce interleaving of the FIR selective sampling and SAR conversion processes, in order to facilitate IIR filtering and increase the conversion rate of the ADC, f_{conv}. As shown in Fig. 4, input sampling and IIR charge sharing $(S_{H(a-d)})$ happens periodically. Interleaving enables this periodic process to continue while the ADC performs SAR conversion. Interleaving also counteracts the reduction in f_{conv} that results from multi-cycle selective sampling. Section III-H below explains how this improvement to f_{conv} ensures that the FIR filter creates enough filtering zeros to reject the alias frequencies of a direct down-converted wanted signal.

We first analyze the reduced rate without interleaving before we analyze the improved rate. The following analysis derives f_{conv} as a function of filter and SAR conversion parameters and the frequency of a master clock, f_{CLK}, which specifies the underlying unit-sampling period. As indicated by S_n in the timing diagram of Fig. 4, selective sampling requires as many periods as the number of filter taps, n_{tap}. And as indicated by S_{Hd}, IIR charge-sharing requires one extra period between sampling and SAR conversion. In (5), n_{IIR} represents this extra period. SAR ADC conversion requires as many periods as ADC bits, n_{SAR}. Without employing any special techniques, the embedded filtering reduces the 7-bit ADC conversion rate, f_{conv}:

$$f_{conv} = \frac{f_{CLK}}{(n_{tap}+n_{IIR}+n_{SAR})} = \frac{f_{CLK}}{(n_{tap}+1+7)} = \frac{f_{CLK}}{(n_{tap}+8)}. \tag{5}$$

We introduce interleaving of the sampling and SAR conversion processes to counteract the reduction in f_{conv} due to the filtering. Fig. 5 and Fig. 6 show the modifications that are made to the traditional SAR ADC architecture to implement interleaved DT filtering. The CDAC in the prototype 7-bit ADC consists of $96C_u$ cells, instead of $64C_u$ cells, per differential half-circuit. These $96C_u$ cells are equally divided into capacitor banks 1a, 1b, and 2. Bank 1a duplicates bank 1b and implement interleaved sampling and SAR operations over four multi-cycle phases. This introduces an approximate increase of 50% in the capacitor bank size, which in the prototype increases the entire differential capacitor bank area from 14,000 μm^2 to 21,000 μm^2.[3]

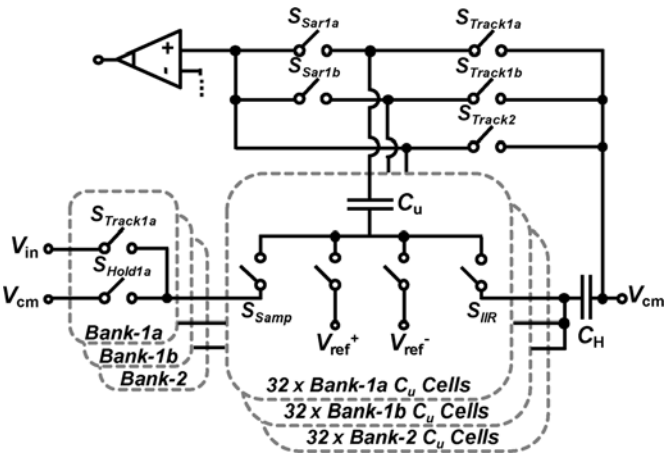

Fig. 5. Diagram of a unit capacitor cell and the switches that implement interleaved DT filtering and SAR conversion in the SARfilter ADC. The 1a, 1b, and 2 banks each has dedicated S_{Track} and S_{Hold} switches. The S_{Sar1a} and S_{Sar1b} switches isolate bank-1a from the comparator while bank-1b participates in SAR conversion and vice versa. Each capacitor unit has an S_{Samp} switch for FIR selective sampling and an S_{IIR} switch for IIR charge-sharing.

Interleaved sampling and SAR processes happen over four phase, each of which consists of *many* clock cycles. In the first of four phases, we selectively sample the first $n_{tap}/2$ taps of an n_{tap} FIR filter onto bank-1a, while SAR conversion digitizes the previously sampled and filtered charge on bank-1b and -2 (top of Fig. 6). In phase 2, we selectively sample the remaining $n_{tap}/2$ taps onto bank-2 (center of Fig. 6), while bank-1a/b remain idle. Phase 3 is identical to phase 1, except that bank-1a and -1b switch roles. We selectively sample the first $n_{tap}/2$ taps of the next conversion cycle onto bank-1b, while SAR conversion digitizes the filtered charge on bank-1a and -2 (bottom of Fig. 6). Phase 4 is identical to phase 2. We once again sample the remaining $n_{tap}/2$ taps onto bank-2, while bank-1a/b remain idle (center of Fig. 6). Then the process repeats from phase 1. IIR charge-sharing occurs periodically throughout this interleaved sampling process in the same way as Fig. 4 shows for non-interleaved sampling.

Fig. 5 shows the extra switches required for interleaving. Each bank (i.e. 1a, 1b, and 2) has dedicated S_{Track} and S_{Hold} switches because, as described above, each bank participates in sampling and SAR at a different time. The S_{Sar1a} and S_{Sar1b} switches between the bank-1a and -1b capacitors and the comparator isolate bank-1a from the comparator while bank-1b participates in SAR conversion and vice versa. In each C_u cell, the

[3]The unit capacitor cell in the prototype measures 8.9 μm $\times$ 12.1 μm. The 10 fF minimum-sized unit MiM capacitor consumes ≈45% of this area, mostly in contact and spacing overhead. An optimized layout would instead place the routing and switches in each unit cell (Fig. 5) beneath the capacitor, thus reducing the area of the entire differential capacitor bank by 45% to $\approx 11,600$ μm^2.

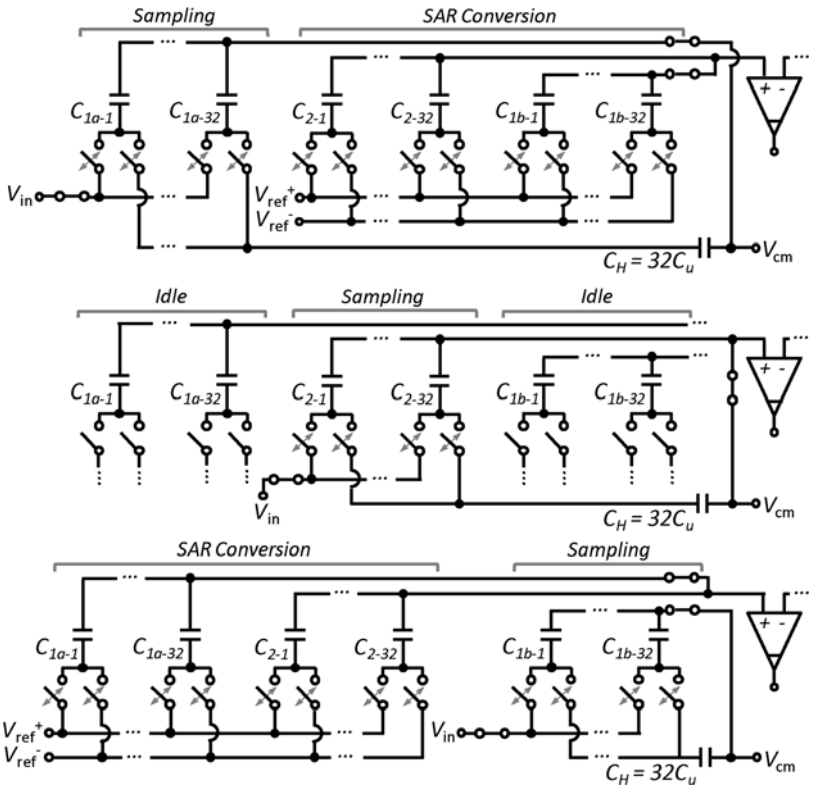

Fig. 6. Interleaved sampling and SAR operations require the ADC to cycle through four multi-cycle phases: (1) sampling onto bank-1a, SAR with bank-1b and -2 (top), (2) sampling onto bank-2 (center), (3) sampling onto bank-1b, SAR with bank-1a and -2 (bottom), and (4) sampling onto bank-2 (center). Some inactive switches are omitted.

S_{Samp} switch between V_{in} and C_u implements selective sampling for FIR filtering. The S_{IIR} switch between C_H and each C_u cell creates a charge-sharing path for IIR filtering.

Interleaving increases the ADC conversion rate:

$$f_{conv} = \frac{f_{CLK}}{max\left(\frac{n_{tap}}{2}, n_{IIR} + n_{SAR}\right) + \frac{n_{tap}}{2}}. \quad (6)$$

In the first term in the denominator, $n_{tap}/2$ accounts for the time spent on interleaved selective sampling and $n_{IIR} + n_{SAR}$ accounts for IIR charge-sharing and SAR conversion (phases 1 and 3 above). This term takes the greater (i.e. max) of the number of clock periods spent: (1) selectively sampling the first half of the FIR filter taps, $n_{tap}/2$, onto one of the 1a/b banks and (2) IIR charge-sharing and SAR conversion with the *other* 1a/b bank and bank-2. The second term in the denominator represents the time spent selectively sampling the second half of the FIR filter taps onto bank-2 (phases 2 and 4 above). Eq. (7) simplifies (6) by substituting typical values of the variables. The first expression in (7) substitutes n_{SAR} of 7 for a 7-bit ADC and n_{IIR} of 1 for the one extra clock cycle spent on IIR charge-sharing immediately before SAR conversion (S_{Hd} in Fig. 4). The second expression assumes that the FIR filter has at least 16 taps, $n_{tap} \geq 16$, so that $n_{tap}/2 \geq 8$ in the max expression.

$$f_{conv} = \frac{f_{CLK}}{max\left(\frac{n_{tap}}{2}, 8\right) + \frac{n_{tap}}{2}} = \frac{f_{CLK}}{n_{tap}} \quad (7)$$

In absolute terms, the benefit to f_{conv} of interleaving decreases as n_{tap} increase, as can be seen by comparing (7) to (5) for n_{tap} of 16 vs. 64. Nonetheless, Section III-H below explains why interleaving is still important for all n_{tap} values because it allows the creation of a DT FIR filter with a sufficient number of anti-aliasing zeros.

G. Constraints on DT FIR Filtering Complexity

The parasitic capacitances and layout area of the sampling and IIR switches (S_{Samp} and S_{IIR} in Fig. 5) and the digital lines controlling these switches limit the number and resolution of the FIR filtering taps. If interleaving is not considered, the CDAC consists of $64C_u$ cells with minimum or nearly minimum-sized switches. Aside from the constraints described in Section III-E above, having $64C_u$ cells limits the FIR filter to a maximum of 64 equally-sized taps, or fewer taps with coefficients limited to the different combinations of C_u groupings (i.e. limited coefficient resolution). Therefore, it is necessary to increase the number of C_u cells in order to increase the tap-count or resolution of the FIR filter. If the number of C_u cells increases and mismatch does not limit the filter response (Section III-J below), then the unit capacitance can be proportionally reduced in size. In contrast, the minimum-sized switches cannot be reduced in size, so their parasitic capacitance increases proportionally with array size. Also, the routing area that digital control lines occupy more than doubles with each doubling of the number of C_u cells, because an increasing number of lines need to be routed through the cells close to the edge of the array. Therefore, the number of C_u cells can realistically only be doubled or possibly quadrupled without migrating to a finer process node.

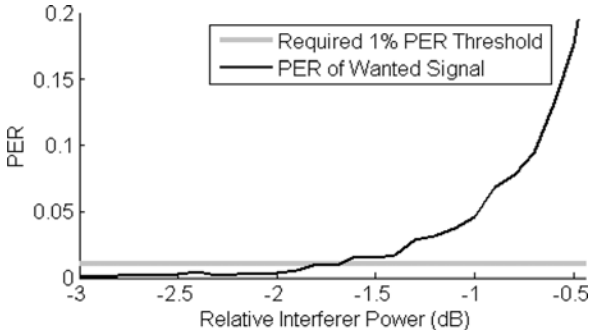

Fig. 7. PER resulting from demodulation of a wanted signal comprised of 208-bit long packets, as a function of the relative power of an aliasing interferer. Both the wanted and interfering signals are compliant to the 2450 MHz band of 802.15.4.

The embedded filter can tolerate limited increases to parasitic capacitances because they do not directly impact the filter's frequency response. The parasitic capacitors attached to the bottom nodes of the unit capacitors (Fig. 5) have equal capacitances (mismatch aside) in all unit cells, so the relative sizes of the FIR coefficients remain constant. The parasitic capacitors attached to the top nodes of the unit capacitors do not participate in charge-sharing. The parasitic capacitor attached to C_H can be absorbed into the size of C_H to keep r_S and r_H (2) constant. The non-linearity of the parasitic capacitances due to NMOS switch junctions, however, indirectly degrades the filter's attenuation, so C_u must remain significantly larger than these parasitic capacitances.

H. Anti-Alias Filtering

Filtering in the receive chain must sufficiently attenuate aliases to permit demodulation of a wanted signal with minimal degradation to the PER. As an example, Fig. 7 plots the simulated PER that results from demodulation of a wanted signal in the presence of an interferer that aliases completely onto the wanted signal. Both the wanted signal and the interferer consist of modulated 2 Mchip/s, 208-bit long packets that are compliant to the 2450 MHz band of IEEE 802.15.4 [16]. Achieving the specified packet error rate (PER) of less than 1% requires the power of the filtered aliasing interferer to be at least 1.8 dB less than to the power of the wanted signal. With further 2 dB of attenuation of the interferer, its effect becomes negligible. For the 2450 MHz band, the specified adjacent ($\pm$5 MHz, +0 dB) and alternate ($\pm$10 MHz, +30 dB) interferers alias completely onto a direct down-converted wanted signal when f_{conv} is 5 MHz. Since the power of the aliased signal should be at least $\approx$2 dB less than the power of the desired signal, the filters should attenuate the adjacent and alternate interferers by more than 2 dB and 32 dB, respectively.

In order to achieve this attenuation, interleaving improves f_{conv} and enables the creation of an FIR filter with enough notches to be placed at all of the alias frequencies lower than f_{CLK} of a narrowband direct down-converted wanted signal. For example, the 16-tap filter shown in Fig. 8 uses interleaving to achieve f_{conv} of 5 MS/s with a filter sampling rate, f_{CLK}, of 80 MS/s. Without filtering, the interferers located at 15 frequencies between DC and f_{CLK}—$m \cdot f_{conv}$,

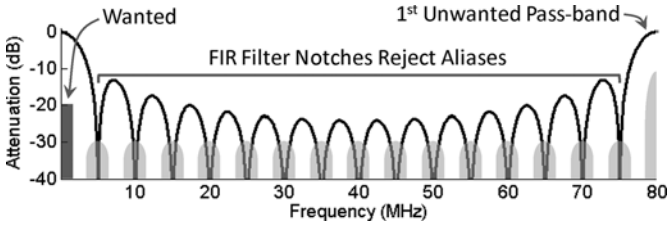

Fig. 8. An example of the FIR component of a SARfilter ADC DT filter, with f_{CLK} of 80 MS/s and f_{conv} of 5 MS/s. Interleaving increases f_{conv} and allows notch placement at all multiples of 5 MHz less than f_{CLK}. These notches reject interferers (light gray) that would otherwise alias onto a wanted signal at DC.

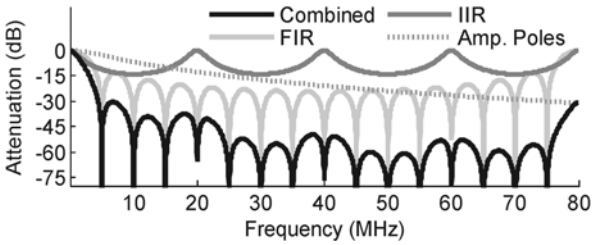

Fig. 9. An example ideal combined filter response and its DT FIR/IIR and amplifier pole components. The DT contribution is described by (8), which results in f_{conv} of 5 MS/s when f_{CLK} is 80 MS/s.

where $m = 1, 2 \ldots 15$—would alias onto the wanted signal at DC. A 16-tap FIR filter creates 15 notches, such that a notch can be placed at all 15 of these alias frequencies of concern. The first unwanted pass-band of the DT FIR filter occurs at $f_{CLK} = 16 \cdot f_{conv} = 80$ MHz. At this relatively high frequency, the amplifier poles in the prototype receiver provide nearly adequate alias rejection of approximately 30 dB.

I. Ideal Receiver Filter Response

The complete filter response of the SARfilter ADC consists of DT and baseband amplifier pole components. As an example, Fig. 9 plots an ideal complete filter response and its components for one of many selectable DT filter configurations. (Fig. 17 below plots the measured response.) Packet tests (Section IV-C) use this exact DT filter configuration because the FIR filter notches are ideally placed to attenuate aliases, as described above and shown in Fig. 8. In this example, f_{CLK} is 80 MHz and f_{conv} is 5 MS/s. The DT components are described by (8), which quantifies an FIR filter with 16 equal tap coefficients and IIR charge-sharing (with C_H) after every 4th sample.

$$y(n) = \frac{1}{48}\left[x(n-1)+x(n-2)+\cdots+x(n-16)\right]+\frac{2}{3}y(n-4)$$
$$H(z) = \frac{\frac{1}{48}(z^{-16}+z^{-15}+\cdots+z^{-1})}{1-\frac{2}{3}z^{-4}} \quad (8)$$

The FIR filter creates narrowband anti-aliasing notches at multiples of f_{conv} (5 MHz, 10 MHz, 15 MHz...) and the IIR filter poles provide wideband attenuation at all frequencies except DC and multiples of $4 \cdot f_{conv}$ (20 MHz, 40 MHz, 60 MHz...).[4] The pole at DC is especially useful for attenuating interferers located at small frequency offsets from the wanted signal at DC.

[4]The FIR and IIR filters together attenuation significantly at $f_{conv}/2$ ($\approx$10.5 dB for (8)), so this filter functions best with modulations that place more spectral power close to DC than at higher frequencies, such as MSK.

TABLE I
ATTEN. (dB) VERSUS MISMATCH, EQ. (8) FILTER, $F_{CLK} = 80$ MS/s
SIMULATED OVER 30,000 DIFFERENT CONFIGURATIONS

Fractional Unit Cap. Mismatch ($\sigma_{dC/C}$)		0	0.1%	0.5%	1%	5%	10%
4 to 6 MHz	Min.	22.24	22.22	22.15	22.03	21.23	20.30
	Mean.		22.24				
	σ		<0.01	0.02	0.05	0.24	0.48
9 to 11 MHz	Min.	33.36	33.29	33.03	32.73	30.41	28.02
	Mean.		33.36			33.20	32.64
	σ		0.02	0.09	0.17	0.69	1.14
14 to 16 MHz	Min.	33.74	33.67	33.39	32.94	30.31	27.85
	Mean.		33.74			33.54	32.93
	σ		0.02	0.10	0.19	0.76	1.25
19 to 21 MHz	Min.	27.33	27.30	27.16	27.00	25.78	24.45
	Mean.		27.33			27.21	26.90
	σ		0.01	0.04	0.09	0.32	0.55

TABLE II
ATTEN. (dB) VERSUS MISMATCH & JITTER, EQ. (8) FILTER, $F_{CLK} = 340$ MS/s
SIMULATED OVER 10,000 DIFFERENT CONFIGURATIONS

Fractional Unit Cap. Mismatch ($\sigma_{dC/C}$)		0			10%
Sampling Jitter (σ_{ps})		0	10	20	10
250.75 to 259.25 MHz	Min.	27.33	25.74	24.78	24.51
	Mean.		27.26	27.01	26.83
	σ		0.34	.59	0.61
272 to 280.5 MHz	Min.	33.74	30.31	28.36	28.05
	Mean.		33.58	33.03	32.83
	σ		0.74	1.27	1.38
293.25 to 301.75 MHz	Min.	33.36	30.03	28.26	27.98
	Mean.		33.20	32.67	32.51
	σ		0.83	1.38	1.29
314.5 to 323 MHz	Min.	22.24	21.22	20.16	20.44
	Mean.		22.24	22.23	22.24
	σ		0.30	0.59	0.56

The amplifier poles in the prototype receiver are located at approximately 6 MHz and 30 MHz and provide high frequency attenuation. Together, the filters very effectively reject aliasing interferers.

J. Capacitor and Clocking Non-Idealities

Analog DT filters are robust to process variation. Unlike continuous-time filters, relative capacitor sizes define the zero and pole locations in DT filters. Therefore, when process variation identically scales the sizes of all of the filtering capacitors, the DT frequency response does not change.

Simulations show that DT filters are also robust to capacitor mismatch. Table I summarizes notch attenuation versus C_u mismatch for over 30,000 different configurations of the analog DT filter that (8) describes. The simulations reflect the analog DT topology shown in Fig. 5 and Fig. 6, in which 96 unit capacitors are grouped together, sampled onto, and charge-shared to produce a filter output. The model includes the effects of a differential array, interleaving of bank-1a and -1b, and proper scaling of mismatch of the $32C_u$ IIR history capacitor, C_H. The model does *not* include the amplifier poles. F_{CLK} is 80 MS/s. Each of

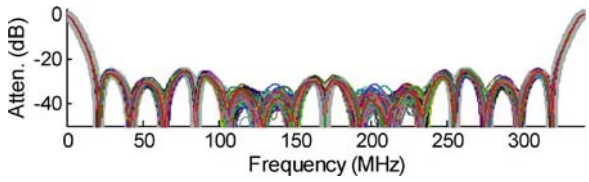

Fig. 10. Simulated frequency response of the DT filter described by (8), when f_{CLK} is 340 MS/s. The gray line plots ideal capacitors and sampling clocks and the colored lines overlay 100 different non-ideal configurations with $\sigma_{\Delta C/C} = 0.1$ and $\sigma_{jitter} = 10$ ps (same as rightmost column of Table II). The non-idealities shift zero locations and decrease notch depth, but the overall frequency response remains well-defined for attenuation of <30 dB.

the rows in Table I lists the minimum, mean, and standard deviation of the attenuation, across the 30,000 mismatched configurations, for 2 MHz wide bands centered at the four lowest frequency FIR notches—5, 10, 15, and 20 MHz (Fig. 8). Each of the columns lists the statistics for different amounts of fraction C_u mismatch, including the non-mismatched case. For example, the 14 to 16 MHz row states that for 5% mismatch, the poorest performing configuration achieves 30.31 dB attenuation across the entire 2 MHz band and that the configurations overall achieve an average of 33.54 dB attenuation across the entire band, with a standard deviation of 0.76 dB. This data shows that even with strongly mismatched unit capacitors, attenuation in nearly all configurations (i.e. $\pm 3\sigma$) does not degrade by more than ≈4.5 dB.

The 10 fF MiM unit capacitors[5] that we use in the prototype have mismatch of less than 0.5%, so the expected effects of mismatch are negligible. The unit capacitors are also physically placed in an approximate common-centroid layout, with respect to how the embedded FIR filter typically groups together unit capacitors to form tap coefficient subgroups (Section III-E above). This placement mitigates mismatch in the tap coefficient sizes due to process doping gradients. In addition, the corresponding bank-1a and -1b capacitors (i.e. C_{1a-1} and C_{1b-1}, C_{1a-2} and C_{1b-2}, etc. in Fig. 6), which duplicate each other in the interleaved sampling and SAR processes, are placed adjacent to each other to reduce mismatch due to distance.

Table II presents the effect of simulated sampling jitter in addition to capacitor mismatch. The model remains the same, but instead the non-idealities are simulated over 10,000 different configurations, f_{CLK} is 340 MS/s, and each row lists statistics for 8.5 MHz wide bands[6] centered at the four highest frequency notches. The columns list the statistics for different amounts of jitter and one case of jitter combined with mismatch. Attenuation in nearly all configurations (i.e. $\pm 3\sigma$) does not degrade by more than ≈5 dB. Synthesizers typically achieve significantly less jitter, so the expected effects of jitter in the prototype are negligible. This data suggest, however, that in the presence of systematic mismatch (edge effects, poor layout, etc.) and other

[5]These minimum-sized MiM capacitors are neither mismatch nor noise limited. The use of metal finger capacitors instead can reduce the unit capacitance while negligibly affecting performance.

[6]The bandwidth of interest is scaled by 340/80, such that the bandwidths normalized to f_{CLK} for the rows in Tables I and II are equal.

clocking non-idealities (supply bounce, coupling, etc.), the attenuation degrades by no more than a few decibels.

Fig. 10 plots the effect on frequency response of the same non-idealities given in the rightmost column of Table II—10% mismatch and 10 ps sampling jitter. The colored plots overlay 100 non-ideal configurations onto the gray ideal plot and show that the non-idealities shift notch locations and decrease notch depth. The overall frequency response remains well-defined for attenuation of less than 30 dB.

K. DT Filter Noise

Multi-cycle FIR selective sampling results in the same total sampled noise as sampling onto the entire SAR ADC CDAC at once. Consider the resulting noise from sampling onto and charge-sharing of two capacitors sized xC and yC,

$$\overline{v_n^2} = \frac{kT}{xC}\left(\frac{x}{x+y}\right)^2 + \frac{kT}{yC}\left(\frac{y}{x+y}\right)^2 = \frac{kT}{(x+y)C}, \quad (9)$$

which is identical to the kT/C noise from sampling in a single clock period onto the capacitance $(x+y)C$.

The DT IIR filter requires charge-sharing of the sampling capacitance with a history capacitor, which introduces additional noise onto the sampling capacitor, C_S.[7] The amount of additional noise is solved as kT/C noise, where C is C_S in series with C_H, followed by capacitive division to determine the component of this noise that is left on C_S.

$$\overline{v_{n,IIR}^2} = \frac{kT}{C_S\left(1+\frac{C_S}{C_H}\right)} \quad (10)$$

In practical filter implementations, C_H is 1–3 times larger than C_S, in order to maintain a good balance between out-of-band attenuation and in-band signal droop. Therefore, IIR filtering approximately doubles the sampled noise.

IV. Results

A. Prototype CMOS Flexible Receiver IC

A prototype flexible receiver with broadband LNA and mixers, amplifiers, and SARfilter ADCs is implemented in a 1P9M 65 nm CMOS process with MIM capacitors. Measurements confirm that the wideband front-end supports communication standards with a wide range of carrier frequencies and that the SARfilter ADC achieves low-power reconfigurable DT interferer rejection and digitization. Fig. 11 shows a photo of the die, in which the active area is 0.24 mm^2. Table III summarizes the measured performance of the receiver operating in the maximum gain setting, in order to determine the best achievable sensitivity. The prototype receiver does not have intermediate probe or stimulus points, so all measurements are for the entire receive chain from the LNA to the ADC. Assuming minimal input loss from a matched RF source, which is reasonable given the measured S_{11} of -10.5 dB, the maximum gain from the RF input to the ADC input is approximately 60 dB. The receiver achieves a NF of approximately 6 dB, which we determine by assuming perfect LNA input matching and comparing 50 Ω source noise with the measured variance of the ADC output code when input-referred to the LNA input. The frequency response of the DT filter can be digitally modified by configuring the number of taps in the FIR filter from 16 to 64 and the size of each coefficient from 0 to $6C_u$. The ADC conversion rate can be as high as 21.25 MS/s when the 16-tap filter described by (8) is enabled, which corresponds to f_{CLK} of 340 MS/s. The measured power consumption of the entire receiver is 3.98 mW, 5.51 mW, and 9.47 mW for the 915 MHz and 2450 MHz bands of IEEE 802.15.4 and for the DSSS PHY of IEEE 802.11, respectively.

TABLE III
Prototype Measurement Summary

Technology		65nm 1P9M w/MIMCAP
Active Area		0.24mm^2
Carrier Frequency Range		500MHz to 3.6GHz
Maximum Gain, from LNA input to SARfilter ADC input		≈60dB
S_{11}		< -10.5dB
Noise Figure (DSB)		≈6dB
IIP3, in-band, from LNA input to SARfilter ADC input		-45dBm
ENOB		≈5b, limited by front-end and baseband amplifier noise and distortion
Maximum f_{conv}, Eq. (8) DT Filter		21.25MS/s
Configurable Filter Tap Length / Weight		16 to 64 / 0 to 6C_u
Power Eq. (8) DT Filter	Analog	5.24mW @ 1.0V 2.79mW @ 0.85V
	Digital	2.16mW @ 1.0V, f_{conv}=11MS/s 0.65mW @ 0.9V, f_{conv}=5MS/s 0.30mW @ 0.9V, f_{conv}=2MS/s
	Clocks, LO Divider	2.07mW, 4.82GHz 2xLO 0.89mW, 1.82GHz 2xLO
	Total	9.47mW, 802.11 5.51mW, 802.15.4 2450MHz 3.98mW, 802.15.4 915MHz
802.11, Eq. (8) DT Filter, f_{conv}=11MS/s		Sensitivity of -83dBm
		Rejection of +20MHz, +41dB unframed interferer
802.15.4 2450MHz, Eq. (8) Filter, f_{conv}=5MS/s		Sensitivity of -92dBm
		Rejection of +5MHz, +33dB and +10MHz, +39dB interferers
802.15.4 915MHz, Eq. (8) Filter, f_{conv}=2MS/s		Sensitivity of -99dBm
		Rejection of +2MHz, +30dB and +4MHz, +33dB interferers

Fig. 12 plots a 16384 point FFT of the ADC output given a 0.9 MHz input tone. The filter described by (8) is enabled and f_{CLK} is 80 MS/s, resulting in f_{conv} of 5 MS/s. The input enters the receiver at the LNA at RF frequencies of 2.4 GHz + 0.9 MHz. Therefore, the FFT includes all of the non-idealities of the entire receiver. The ADC achieves an ENOB of 4.99 bits. The SFDR is limited by an $f_{conv}/2$ tone caused by interleaving, although this tone exceeds the power of the 8th harmonic by only 0.95 dB. Fig. 13 plots the ENOB as a function of f_{conv}. ENOB decreases from 5.08 to 4.56 bits as f_{conv} increases

[7]Noisy FIR charge-sharing switches redistribute charge between the many capacitors that jointly hold the sampled and filtered charge. The SAR algorithm then digitizes the *total* charge held on these capacitors, so FIR charge-sharing noise does not appear in the digital output. Noisy IIR charge-sharing switches redistribute charge between the sampling and history capacitors. The SAR algorithm only digitizes the resulting charge on C_S, so IIR charge-sharing noise *does* appear in the digital output.

TABLE IV
PERFORMANCE COMPARISON OF IEEE 802.15.4 RECEIVERS

	This Work	[14]	[19]	[2]	[20]
Gain	60dB	37dBv/dBm	75dB	--	83.5dB
NF	6dB	6dB	12dB	5.7dB	9.5dB
IIP_3	-45dBm	-12dBm	-12.5dBm	-16dBm	-18dBm
Sens.	-92dBm	--	--	-101dBm	-96dBm
Adj. Blocker	+33dB	+30dB	+35dB	+36dB	+54dB
Power	5.5mW	5.4mW	3.6mW	16.7mW	≥18.4mW
Process	65nm	90nm	90nm	180nm	180nm
Notes	--	No ADC, IEEE 802.11b Blocker	No ADC	Complete digital baseband	

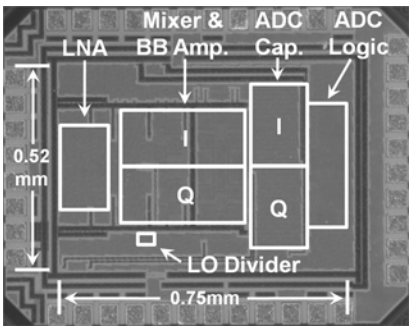

Fig. 11. Die photo.

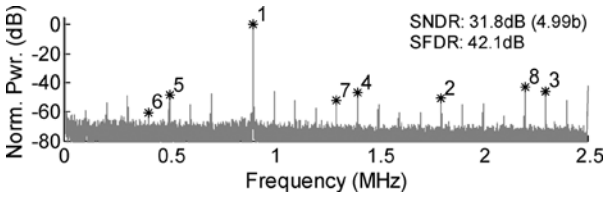

Fig. 12. 16384 point FFT of the ADC output in response to an $f_{LO}+0.9$ MHz input tone to the LNA of the receiver. Eq. (8) describes the embedded DT filter, which results in f_{conv} of 5 MS/s when f_{CLK} is 80 MS/s. The numbers label the input tone and its harmonics.

from 2.5 to 21.25 MS/s, respectively. Fig. 14 plots the ENOB as a function of the ADC input frequency, $f_{in,dc}$, normalized to f_{conv}. The ENOB remains nearly constant until $f_{in,dc}/f_{conv}$ exceeds 0.4, at which point the amplifiers that precede the ADC can no longer drive large enough of an input into the ADC to fill its full-scale input range, due to the embedded filter's attenuation. Fig. 15 plots the DNL and INL of the ADC.

The receiver supports RF carrier frequencies ranging from 500 MHz to 3.6 GHz. Fig. 16 quantifies this capability by plotting the necessary *RF input* power to achieve a fixed *ADC output* dynamic range of 4-bit ENOB (25.84 dB SNDR) as a function of carrier frequency. The RF input power ranges from -70 to -60.5 dBm.[8] These measurements reflect the achievable sensitivity at a given RF carrier frequency. For example, the ADC output achieves 25.84 dB SNDR at 2.4 GHz with a -66 dBm RF input. This implies that the output can

[8]Variation in gain and other less significant factors contribute to the range of input power. At lower frequencies, the coupling capacitor between the LNA and mixer impedes the signal. At higher frequencies, the output power of the LO divider decreases, which reduces the conversion gain of the mixer.

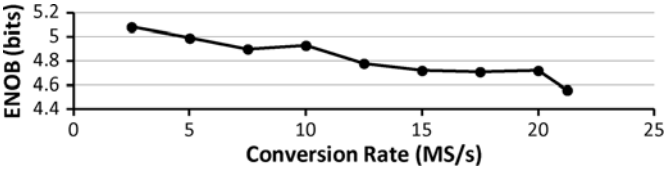

Fig. 13. ENOB vs. ADC conversion rate, in response to an $f_{LO}+0.9$ MHz input tone to the LNA of the receiver (f_{LO} is 2.4 GHz). Eq. (8) describes the embedded DT filter that the ADC implements.

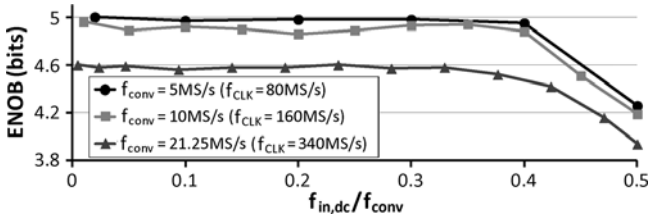

Fig. 14. ENOB vs. $f_{in,dc}$ normalized to f_{conv}, where $f_{in,dc}$ is the down-converted frequency of an RF input tone to the LNA of the receiver (f_{LO} is 2.4 GHz). Eq. (8) describes the embedded DT filter that the ADC implements. At $f_{in,dc}/f_{conv}$ greater than ≈0.4, the ENOB decreases because the test tone does not fill the full-scale input of the ADC, regardless of input power, due to the filter's attenuation.

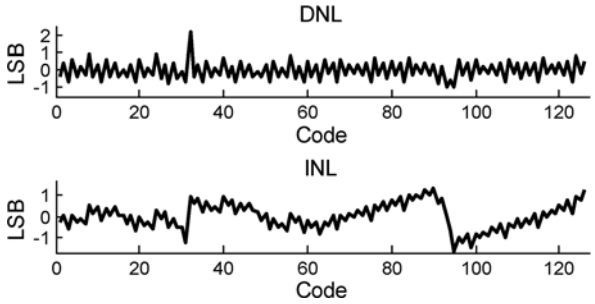

Fig. 15. DNL and INL of the SARfilter ADC, when operating in the DT filtering mode described by (8). As with the ENOB measurements above, these measurements includes the effect of the RF front-end and back-end and the test input is a RF tone.

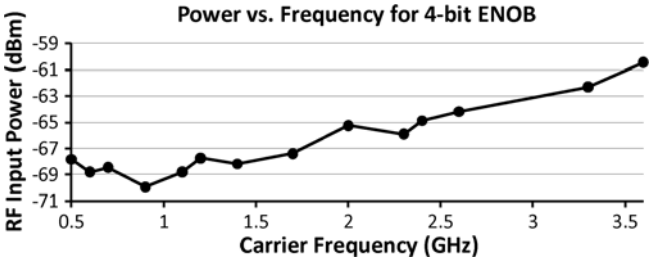

Fig. 16. RF input power necessary to achieve a fixed (4-bit ENOB) ADC dynamic range with an $f_{carrier}+1$ MHz tone input, as the carrier and LO frequencies vary from 500 MHz to 3.6 GHz. Supplies are fixed at 1 V.

achieve the required -2.2 dB SNDR for the 2450 MHz band of IEEE 802.15.4 [17] with an RF input power of -94.04 dBm (i.e. -66 dBm $-$ 25.84 dB $-$ 2.2 dB), which is consistent with the measured sensitivity of -92 dBm (Section IV-C below).

B. Measured Filter Response

Fig. 17 overlays the measured and ideal frequency responses at the output of the ADC. The measured frequency response

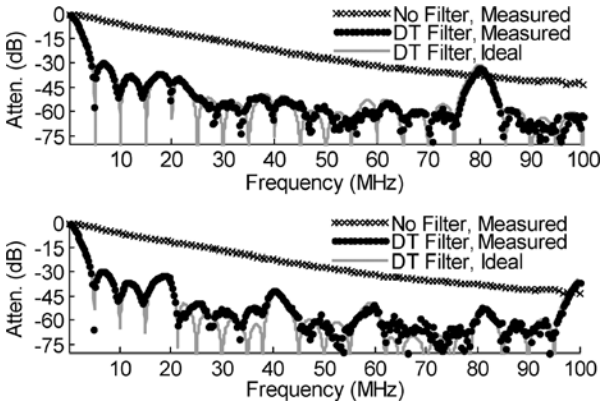

Fig. 17. Measured no-filter mode filter response and ideal and measured filter responses of the DT filter described by (8) with $f_{CLK} = 80\ \mathrm{MS/s}$, $f_{conv} = 5\ \mathrm{MS/s}$ (top) and by (11) with $f_{CLK} = 100\ \mathrm{MS/s}$ and $f_{conv} = 5\ \mathrm{MS/s}$ (bottom).

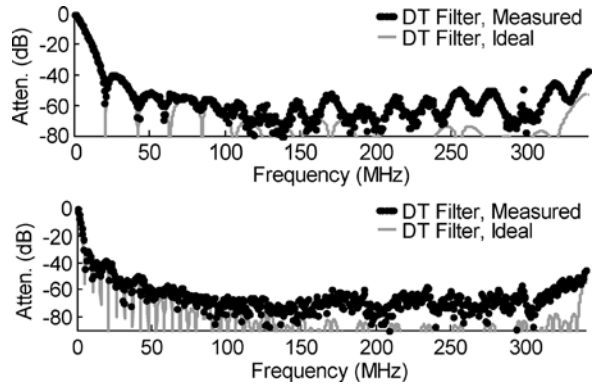

Fig. 18. Ideal and measured filter responses of the DT filter when f_{CLK} is 340 MS/s. The top plot is of the filter described by (8) (16-tap FIR, $f_{conv} = 21.25\ \mathrm{MS/s}$) and the bottom plots is of similar filter, but with 64 equal taps in the FIR filter ($f_{conv} = 5.3125\ \mathrm{MS/s}$).

plots the down-converted power of a swept single-tone RF input. The top and bottom plots show the measured responses when a 16-tap (8) and a 20-tap (11) DT filter are configured, respectively.

$$y(n) = \frac{1}{192}\left[3x(n-1) + 3x(n-2) + 4x(n-3) + 3x(n-4) + 3x(n-5) + \cdots + 3x(n-20)\right] + \frac{2}{3}y(n-5) \quad (11)$$

The "no filter" measurements represent the attenuation provided by the baseband amplifier poles. Although the tap lengths of the two filters differ, f_{conv} is set to 5 MS/s in both configurations by choosing f_{CLK} of 80 MS/s and 100 MS/s for the 16-tap and 20-tap filters, respectively. The 20-tap filter benefits from a higher unwanted pass-band frequency of 100 MHz, instead of 80 MHz, at the cost of higher power consumption. When combined with amplifier pole attenuation, both configurations attenuate aliasing interferers and adjacent channels at frequencies higher than f_{conv} by more than 30 dB. The difference between the measured and ideal FIR zero locations are likely caused by systematic capacitor mismatch (e.g. no dummy capacitors on the edge of the array) and timing mismatch of the sampling clocks.[9]

Fig. 18 plots the measured frequency response of the embedded filter for a higher f_{CLK} of 340 MS/s. The top and bottom plots show the response of 16-tap (8) and 64-tap FIR filters with equal tap coefficients and IIR charge-sharing after every 4 and 16 samples, respectively. The measured response accurately resembles the ideal response at low frequencies, but deviates at higher frequencies due to a combination of clock jitter and settling issues.

C. Packet Tests

We verify the entire receiver by measuring error rates using IEEE 802.15.4 and IEEE 802.11 compliant packets. Matched filter demodulation with digital phase correction is performed off-chip. The IEEE 802.15.4 tests are performed as required by the specifications [16], except that only the 20 byte payload is analyzed for bit errors.[10] As shown in the last two rows of Table I, f_{conv} is set such that the specified interferers are centered at f_{conv} or $2 \cdot f_{conv}$. This frequency plan demonstrates that the DT filter sufficiently attenuates interferers when they alias completely onto the desired signal. The IEEE 802.11 test parameters are chosen to be similar to the specified DSSS PHY requirements [18]. F_{conv} is set equal to the chip rate and the interferer is set to the channel frequency that is closest to $2 \cdot f_{conv}$. The desired signal is IEEE 802.11 compliant at a 1 Mbps (11 Mchip/s) data rate and framed with a 1024 octet payload. The results of packet testing are summarized in Table I. The receiver achieves a measured sensitivity of -99 dBm and $+30$ dB and $+33$ dB adjacent and alternate channel interferer rejection with packets compliant to the 915 MHz band of IEEE 802.15.4. It achieves -92 dBm sensitivity and $+33$ dB and $+39$ dB adjacent and alternate channel interferer rejection with packets compliant to the 2450 MHz band of IEEE 802.15.4. This measured performance exceeds the requirements of the IEEE 802.15.4 standard. In IEEE 802.11 tests, the receiver achieves -83 dBm sensitivity and rejects a $+20$ MHz, $+41$ dB unframed interferer that is 802.11 coded and modulated at 1 Mbps (11 Mchip/s).

V. Conclusion

The analog DT filter embedded within a SARfilter ADC enables a flexible and scalable wireless receiver that can adapt to the needs of many standards and bands and to its operating environment. The receiver's flexibility is made possible by a wideband front-end and a SAR ADC with an embedded software-configurable DT filter. This embedded filter replaces separate baseband filter stages and greatly simplifies the design of the baseband chain. The design of the SARfilter ADC is inherently well-suited for nanometer CMOS processes, because it consists primarily of switches and capacitors. These benefits make the flexible SARfilter ADC wireless receiver a promising RF architecture for integration into a modern-day wireless transceiver SOC.

[9]All of the sampling and charge-sharing clocks are routed by a digital auto place and route (APR) tool that does not guarantee equal RC delays on all of the lines.

[10]Omission of the 6 byte header from error analysis results in <0.2 dB error in measured sensitivity.

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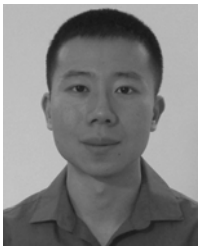

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