

CMOS DLL Based 2V, 3.2ps Jitter, 1GHz Clock Synthesizer and Temperature Compensated Tunable Oscillator.

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Abstract - This paper describes a low voltage, low jitter clock synthesizer and a temperature compensated tunable oscillator. Both of these circuits employ a self-correcting Delay Locked Loop (DLL). The DLL provides multiple clock phases that are combined to produce the desired output frequency for the synthesizer and provides temperature compensated biasing for the tunable oscillator. With a 2V supply the measured RMS jitter for the 1GHz synthesizer output was 3.2ps. With a 3.3V supply RMS jitter of 3.1ps was measured for a 1.6GHz output. The tunable oscillator has a 1.8% frequency variation over an ambient temperature range from 0 to 85°C. The circuits were fabricated on a generic 0.5µm digital CMOS process.

I. INTRODUCTION

Traditionally phase locked loops (PLL) have been used for clock synthesis. The synthesizer and tunable oscillator outlined in this paper employ a DLL. A DLL provides greater stability than higher order PLL's and requires only one capacitor in its first order loop filter. Additionally, a DLL offers better jitter performance than a PLL because phase errors induced by supply or substrate noise do not accumulate over many clock cycles [1].

The self-correcting DLL incorporated in the synthesizer and tunable oscillator overcomes problems of false locking associated with conventional DLLs. The self-correcting circuit detects when the DLL is locked, or is attempting to lock, to an incorrect delay and can then bring the DLL back into a correct locked-state. This DLL does not require the VCDL control voltage to be set on power-up, it can recover from missing reference clock pulses and because the delay range is not restricted it can accommodate a variable reference clock frequency.

The synthesizer outlined in this paper operates over a wide range of input reference clock frequency and provides a low jitter output at a multiple of nine times the reference frequency. The jitter measurements of 3.2ps RMS and 20ps pk-pk, for a 2V supply and 1GHz output frequency, show that the core DLL has better jitter performance than recently reported DLLs [2], [3].

The tunable voltage controlled oscillator, VCO, is targeted for use in a transceiver where the receive and transmit clocks

are plesiochronous. It is possible to tune the VCO around a centre frequency while still maintaining good temperature independence. In some applications it may also act as a replacement for a fractional-N type synthesizer. This circuit is similar to the oscillator described in [4] but it uses a lower jitter DLL in place of the PLL and can operate over a wider frequency range while still maintaining good temperature independence and low jitter.

II. ARCHITECTURE AND CIRCUIT DESIGN

A. Self-correcting DLL

A simplified block diagram of the self-correcting DLL is illustrated in Figure 1. This circuit comprises of a voltage controlled delay line (VCDL), a phase detector (PD), a charge pump, a first order loop filter and a lock detect circuit. The VCDL, consisting of cascaded variable delay stages, is driven by the reference input clock, *ckref*. The VCDL final stage output, ϕ_9 , and the *ckref* falling edges are compared by the PD to determine the phase alignment error. The PD output is integrated by the charge pump and loop filter capacitor to generate the delay stages control voltage, *vcntl*.

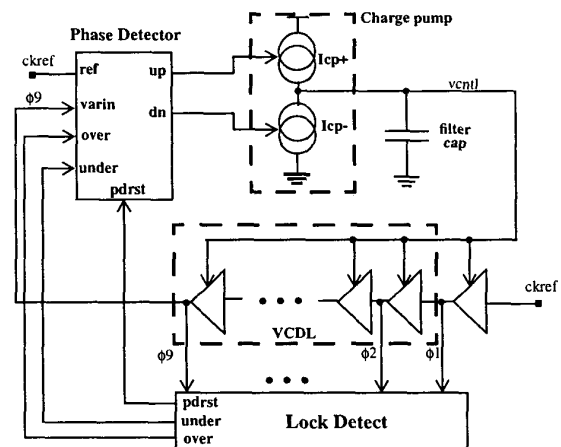


FIGURE 1. DLL architecture.

The VCDL output phases, $\phi(1:9)$, are latched by the lock detect circuit. The state of these phases is decoded to indicate the VCDL delay. Figure 2 illustrates a false locking scenario

for a DLL employing a nine stage VCDL. The ck_{ref} and ϕ_9 falling edges are aligned and in a conventional DLL this would be treated as a correctly locked loop. However in this case the DLL is locked incorrectly to two ck_{ref} periods of delay.

Three control signals are produced by the lock detect circuit: “over” to indicate that the VCDL delay is greater than 1.5 reference clock periods, “under” to indicate that the delay is less than 0.75 clock periods and “pdrst” to reset the phase detect circuit when the VCDL delay has reached 1.25 clock periods. The VCDL delay range is sufficient to trigger these control signals over all process, voltage, and temperature combinations. If none of the three control signals is active then the phase detect has control of the loop and the DLL is either in correct lock or approaching correct lock.

If the DLL is in lock and it is brought out of lock by some missing reference clock pulses or a step in the input reference frequency then the DLL can inadvertently try to lock to an incorrect delay. The DLL is allowed to attempt to reach the undesired lock delay until it triggers either an “over” or an “under” signal at which time the lock detect circuit takes control of the DLL loop.

The circuit used to decode the nine stage VCDL outputs is capable of detecting incorrect delays up to 8 periods of the reference clock. This is not a limitation of the design as any delays above this would be below the range of the VCDL. It follows that this error detection logic can detect an incorrect lock delay up to $N-1$ periods of the reference clock, where N is equal to the number of VCDL output phases.

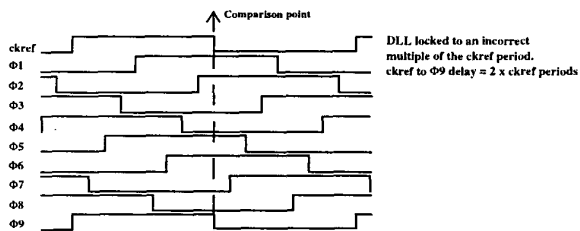


FIGURE 2. False locking in a DLL.

B. Clock synthesizer.

The clock synthesizer employs the DLL structure shown in Figure 1 to generate the multiple clock phases that are then combined to produce the output clock. To generate the output clock the DLL output phases, $\phi(1:9)$, are first combined in an optimized AND-OR structure with symmetrical propagation delays. Figure 3 illustrates the combination of the ϕ_1 , ϕ_4 & ϕ_7 phases to generate the nck_1 clock (which runs at three times the input reference clock frequency). Using similar logic the ϕ_2 , ϕ_5 & ϕ_8 phases produce the nck_2 clock and the ϕ_3 , ϕ_6 & ϕ_9 phases produce the nck_3 clock. These three clocks, nck_1 , nck_2 & nck_3 are phase shifted by one ninth of the reference clock period. These clocks are then combined in an AND-OR

structure to produce an output clock, nck_4 , having nine times the reference clock frequency. This design produces a 1.008GHz output clock frequency for a 112MHz reference clock frequency. The high bandwidth available at the chip outputs is utilized (determined by the external pull-up resistor and load capacitance) to produce the 1GHz clock as shown in Figure 3. The AND function of the clock generation is performed in the chip core and the analog OR function is performed in the I/O buffer area. External load resistors set the output swing and match the output impedance to that of the test equipment

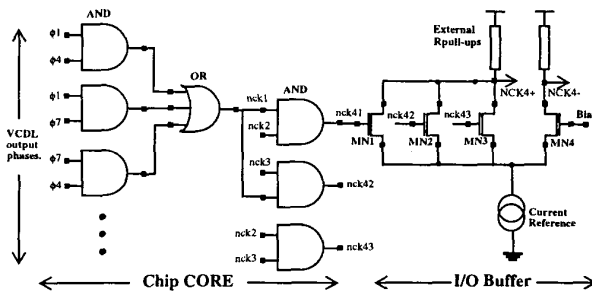


FIGURE 3. 1GHz clock generation schematic.

C. Tunable oscillator with temperature compensation.

The temperature compensated oscillator utilizes the control loop voltage, $vcntl$, of the DLL (Figure 1) to compensate for any temperature and supply voltage induced frequency fluctuation. Figure 4 illustrates how the stage delays of the VCDL and VCO are controlled by $vcntl$. The final VCO stage has an additional tuning voltage, $tune$, which sets the VCO frequency. The VCDL in the DLL tracks temperature and process variations in the circuit. The VCO is composed of the same delay stages as the VCDL and its temperature (and process) variations will therefore be the same apart from some minor random mismatch effects and thermal gradients across the die. $vcntl$ thus compensates for the VCDL and VCO temperature fluctuations.

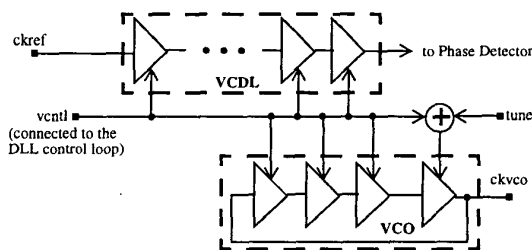


FIGURE 4. Tunable VCO control architecture.

The voltage controlled resistor, VCR, is similar to that in [5] but includes an extra device MN_4 . In the last stage of the VCO this is connected to the control voltage “tune”, Figure 5.

In all other stages it is connected to ground. The extra current required in the final VCO stage is provided by an extra controlled current source MP5.

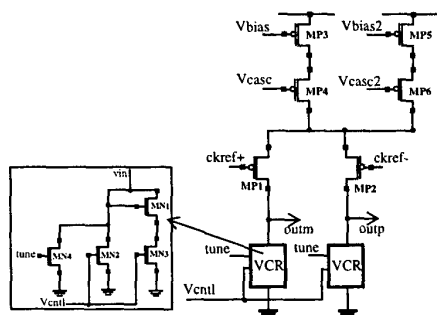


FIGURE 5. Tunable VCO stage block diagram.

D. Circuit layout.

The synthesizer and temperature compensated tunable oscillator were fabricated on a standard $0.5\mu\text{m}$, triple metal, single poly, digital CMOS process. The synthesizer has an active area of 0.6mm^2 and the temperature compensated tunable oscillator has an active area of 0.7mm^2 , Figure 6.

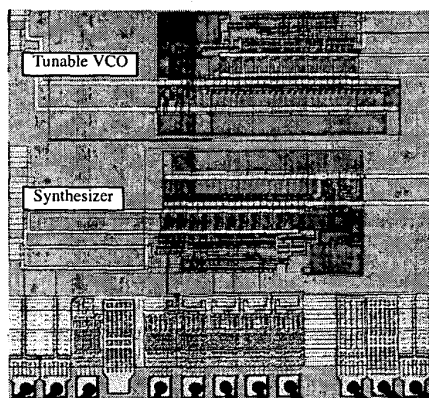


FIGURE 6. Die Photo of the Synthesizer and Tunable Oscillator.

III. TEST RESULTS

Figure 7 shows a histogram of the edge jitter on the 1GHz synthesizer output clock for a supply of 2V. RMS edge jitter of 3.2ps and peak-to-peak edge jitter of 20ps were measured. Similar results were obtained for various output clock frequencies between 600MHz and 1GHz. The jitter measurements of 3.2ps RMS and 20ps pk-pk, for a 2V supply and 1GHz output frequency, show that the DLL core exhibits better jitter performance than that reported for the higher voltage DLLs (3.3V supply, $0.35\mu\text{m}$ CMOS, 4ps RMS jitter) in [2] and (5V supply, $0.7\mu\text{m}$ CMOS, 10ps RMS jitter) in [3]. With the supply reduced to 1.8V the RMS jitter was measured at

4.9ps for an output frequency of 720MHz. Figure 8 illustrates this 720MHz synthesizer output. With a 3.3V supply RMS jitter of 3.1ps was measured on a 1.6GHz output. Mismatched propagation delays and inter-block routing in the frequency multiplication block (Figure 3) resulted in 100ps inter-period jitter. Table 1 summarizes the DLL synthesizer characteristics.

Figure 9 illustrates the temperature compensated tunable oscillator frequency variation with temperature. Varying the ambient temperature from 0 to 85°C resulted in a total frequency variation of 1.8% for a 400MHz output frequency. Figure 10 shows the variation of frequency with the tune voltage. As can be seen from the plot the relationship is close to linear for tune above 0.7V. It is possible to tune the frequency around a centre frequency in the range from 200MHz to 500MHz by selecting an appropriate input reference frequency. This ensures that this scheme can be used for a wide variety of applications. The measured jitter on the 400MHz output was 29ps RMS and 180ps pk-pk. Table 2 summarizes the characteristics of the temperature compensated tunable oscillator.

TABLE I-Measured Synthesizer Characteristics.

1GHz Edge jitter (pk-pk)	< 20ps
1GHz Edge jitter (RMS)	3.2ps
1GHz inter-period jitter	100ps
Power supply	1.8-3.3V
Current consumption @ 2V:	
Synthesizer	20mA
Output Driver	7mA
Output Clock frequency range	600MHz to 1GHz
On chip loop filter capacitor	20pF
Active area	0.6mm^2
Process	$0.5\mu\text{m}$ CMOS

TABLE II-Measured Tunable oscillator Characteristics

400MHz frequency variation over temperature range 0 to 85°C	1.8%
Frequency tuning range	200MHz to 500MHz
400MHz Edge Jitter (RMS)	29ps
400MHz Edge Jitter (pk-pk)	180ps
VCO supply sensitivity (open loop)	0.83%/V
Power supply	3.3V
Current consumption @ 3.3V:	
DLL + Tunable VCO	42 mA
Output Driver	6mA
Active area	0.7mm^2
Process	$0.5\mu\text{m}$ CMOS

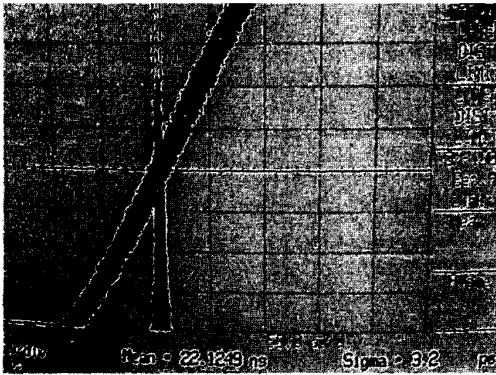


FIGURE 7. 1GHz synthesizer jitter measurement.

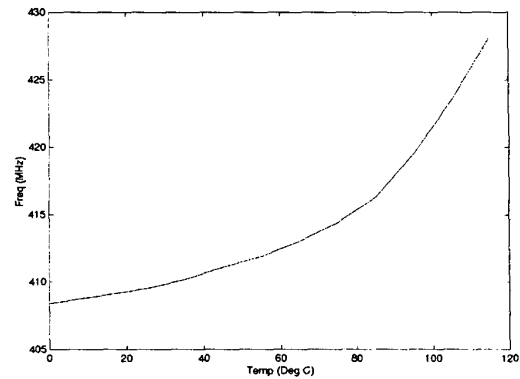


FIGURE 9. Oscillator frequency variation with temperature.

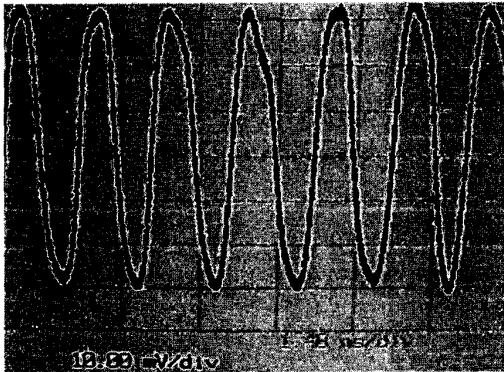


FIGURE 8. 720MHz synthesizer output for VDD=1.8V.

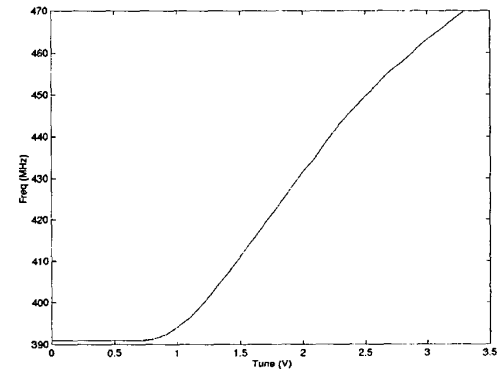


FIGURE 10. Oscillator frequency variation with tune voltage.

IV. CONCLUSIONS

In this paper a robust self-correcting low jitter DLL was used as the basis for a low voltage high frequency synthesizer and a tunable temperature compensated oscillator. The DLL does not require the VCDL control voltage to be set on power-up. The DLL can recover from missing reference clock pulses and it can track step changes in a variable reference clock frequency. The synthesizer has significantly lower edge jitter than the traditional PLL type synthesizer [6] and other reported DLL circuits [7], [8]. The tunable oscillator provides a temperature stable tunable frequency that varies by just 1.8% over the 0 to 85°C temperature range.

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