11.5 A 100MS/s 10.5b 2.46mW Comparator-less Pipeline ADC Using Self-Biased Ring Amplifiers

Yong Lim[1,2], Michael P. Flynn[1]

[1]University of Michigan, Ann Arbor, MI,
[2]Samsung Electronics, Yongin, Korea

Pipelined ADCs require accurate amplification; however traditional OTAs limit power efficiency since they require high quiescent current for slewing. In addition, it is difficult to design low-voltage OTAs in modern, scaled CMOS. The ring amplifier [1-4] provides an intriguing alternative to traditional OTAs. This work improves the power efficiency and practicality of the ring amplifier by introducing a self-biasing scheme and by eliminating the comparators.

The ring amplifier is comprised of three inverter stages (Fig. 11.5.1(a)), stabilized in a feedback configuration. To prevent oscillation, [3] splits the second stage into two separately biased AC-coupled inverters. The bias voltages V_{RP} and V_{RN} are tuned to ensure that the 3rd-stage transistors M_{CP} and M_{CN} enter deep sub-threshold as V_{IN} approaches the desired virtual ground voltage, so that the output-stage resistance increases dramatically, and forms a dominant pole that stabilizes the amplifier. (A related consideration for stability [3] is that the peak overdrive voltage applied to the output transistors should decrease during each successive oscillation period.) The ring amplifier has high gain, thanks to its three stages. Furthermore, the ring amplifier can slew very efficiently because the 3rd-stage inverter acts as a pair of digital switches during slewing. A drawback, especially considering process and supply voltage variation, is that the bias voltages V_{RP} and V_{RN} must be set within a small voltage window. If the quiescent overdrive voltages are too high, then the ring amplifier can oscillate because the output resistance of the third inverter stage is never sufficiently large to create positive phase margin. On the other hand, if the quiescent overdrive is too low, then once the ring amplifier settles the 2nd-stage inverters operate in triode resulting in a low overall three-stage gain. This paper presents a self-biased ring amplifier that is robust to transistor variation. Furthermore, a comparator-less pipeline ADC structure uses the characteristics of the ring amplifier to replace the sub-ADC in each pipeline stage.

Our self-biased ring amplifier structure (Fig. 11.5.1(b)) replaces the two AC-coupled 2nd-stage inverters with a single self-biased DC-coupled inverter, and eliminates the two external biases and the switches. We implement the 3rd-stage inverter with high-V_{TH} devices, which present a much higher output resistance for a given gate-source voltage. An important change is that a resistor, R_B, placed between drains of the 2nd-inverter transistors, dynamically sets the last-stage gate voltages, V_{CP} and V_{CN}. This dynamic biasing maximally drives the last-stage transistors when the ring amplifier is slewing, and provides an offset voltage to set the last-stage transistors in deep sub-threshold when V_{IN} is close to the virtual ground. An important advantage of this resistor-based offset over the previous use of a reference voltage is that the offset tracks variation of the power supply voltage (V_{DD}).

The first inverter is optimized for low noise and power efficiency. A diode-connected transistor M_{NR} lowers the effective power supply voltage of the first inverter, composed of M_{P1} and M_{N1}. The reduced inverter power supply allows us to use a larger W/L ratio for M_{P1} and M_{N1}, so that a higher transconductance is achieved with a given current consumption, thereby resulting in a lower thermal noise without an increase in the static power consumption. This technique is only applicable to the first inverter because its output does not require rail-to-rail swing.

Since the self-biased ring amplifier is essentially a cascade of inverters, we use an auto-zero offset canceling technique to set a bias point without any external bias. The auto-zero self-biasing scheme in a 1.5b flip-around MDAC gain stage is shown in Fig. 11.5.2 (The actual implementation is pseudo-differential). During Φ_1, input signal is sampled onto the C_1 and C_2 capacitors, and the amplifier offset is sampled on C_C. An auxiliary loading capacitor, C_{LA}, connected to the output during auto-zeroing stabilizes the ring amplifier and also samples the input offset voltage. C_{LA} is required because the next-stage sampling capacitors are disconnected during the Φ_1 sampling phase. C_{LA} is made twice as large as the loading from the next stage because the feedback factor during auto-zero/sampling is larger than that during the gain phase. However, the use of C_{LA} does not increase the dynamic power consumption since the sampled voltage on C_{LA} stays almost constant for every cycle.

Significantly, we also use the sampled offset voltage stored on C_{LA} to mitigate the gain error caused by the parasitic capacitance across the feedback auto-zero switch S_{AZ1}. As shown in Fig. 11.5.2, we form this switch as the series combination of two switches, S_{AZ1} and S_{AZ2}, instead of single switch. During the sampling phase Φ_1, both S_{AZ1} and S_{AZ2} are on and S_{AZ8} is off to achieve auto-zeroing. Then in the gain phase Φ_2, S_{AZ1} and S_{AZ2} are disconnected and S_{AZ3} connects the intermediate node V_{AZ} to the sampled offset voltage on C_{LA}. This method isolates the S_{AZ1} source-drain parasitic from changes in the output voltage during slewing and settling. By holding V_{AZ} constant at the auto-zero voltage during amplification, the parasitic capacitance is effectively grounded.

We exploit the characteristics of the ring amplifier to eliminate the comparators in a 1.5b-per-stage pipeline (Fig. 11.5.3). Our scheme uses the direction of the amplification to replace the sub-ADC comparators in the subsequent stage. At the beginning of the amplification phase, the output, V_{CP}, of the second inverter hits ground when the amplification result is higher than V_{CM}, and hits V_{DD} when the amplification result is lower than V_{CM}, then goes near to the self-bias voltage. This information is captured by a clock-gated low-threshold NOR gate and a low-power set flip-flop shown in Fig. 11.5.3(a). The flip-flop is preset low at the end of the sampling phase and goes high when the amplification result is expected higher than V_{CM}. The opposite situation is captured by the same circuit of the other pseudo-differential path. When the amplification result is close to V_{CM}, neither of the flip-flops is set. The flip-flop information is decoded by a simple logic circuit (Fig. 11.5.3(b)), and used as the next-stage coarse ADC result. The auto-zeroing ensures the correct decision direction. The threshold is set by the NOR window and the output slew rate. The pulse V_{CP} (Fig. 11.5.3(c)) is low while the amplifier is slewing positively, but NOR is not immediately enabled thereby setting a threshold relative to V_{CM}. The accuracy of the threshold is well within the redundancy of the 1.5b-per-stage pipeline. The switches S_{R1} and S_{R2} in Fig. 11.5.2 empty the capacitor before the sampling phase to ensure the amplification of the previous stage starts from V_{CM} in every cycle.

The self-biased ring amplifier is used in all stages of a 100MS/s, 10.5b pipeline ADC, implemented in 1P9M 65nm 1.2V CMOS (Fig. 11.5.4). The ADC is composed of a pseudo-differential flip-around ring amplifier based SHA with bootstrapped input switches, nine pseudo-differential 1.5b MDAC stages, and dummy loading for the last stage. Pseudo-differential CMFB in [1] is implemented in every stage. The MDAC references are set at 0.1V and 1.1V thanks to the wide swing of the ring amplifier. The SHA stage also provides the first MDAC digitization. To further optimize the power efficiency, the seven last MDAC stages are scaled down by half compared to the first two MDAC stages.

The ADC has a measured (Fig. 11.5.5) SNDR, SNR and SFDR of 56.3dB (9.06b), 56.7dB and 67.6dB, respectively, for a Nyquist frequency input sampled at 100MS/s and consumes 2.46mW, which results in a Figure-of-Merit of 46.1fJ/conv-step. The power consumption is measured for a Nyquist input and includes the clock buffer, digital correction, and references power. The prototype is more than 3× faster and has a 2× better FoM than [2], which uses a similar pipeline ADC structure (Fig. 11.5.6). The measured INL and DNL from the 10b output are +0.30/-0.34 LSB and +0.75/-0.81 LSB respectively. The SNDR remains stable up to V_{DD} of 1.28V, proving that the self-bias effectively tracks the power supply voltage variation. Figure 11.5.7 shows a die micrograph. The ADC occupies 0.1mm².

Acknowledgements:
The authors thank Berkeley Design Automation for simulation software.

References:

[1] B. Hershberg, *et al.*, "Ring Amplifiers for Switched-Capacitor Circuits," *ISSCC Dig. Tech. Papers*, Feb. 2012.
[2] B. Hershberg, *et al.*, "A 61.5dB SNDR Pipelined ADC Using Simple Highly-Scalable Ring Amplifiers," *VLSI Circ. Symp. Dig. Tech. Papers*, June 2012.
[3] B. Hershberg, *et al.*, "Ring Amplifiers for Switched Capacitor Circuits," *IEEE J. Solid-State Circuits*, Dec. 2012.
[4] B. Hershberg and U.-K. Moon, "A 75.9dB-SNDR 2.96mW 29fJ/conv-step Ringamp-Only Pipelined ADC," *VLSI Circ. Symp. Dig. Tech. Papers*, June 2013.

 978-1-4799-0920-9/14/$31.00

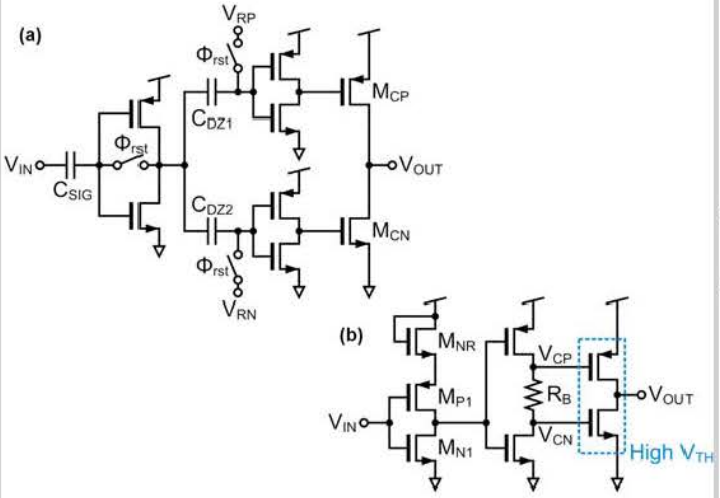

Figure 11.5.1: (a) Conventional ring amplifier, (b) self-biased ring amplifier.

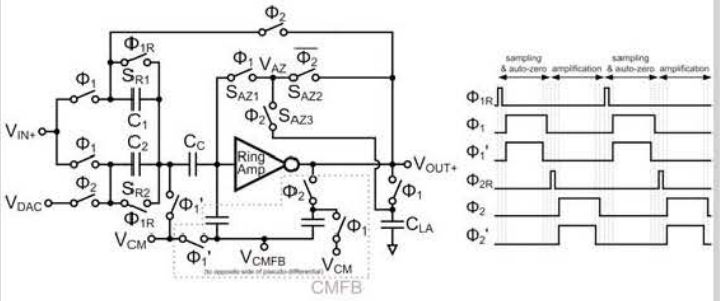

Figure 11.5.2: Ring amplifier flip-around MDAC gain stage with auto-zero scheme.

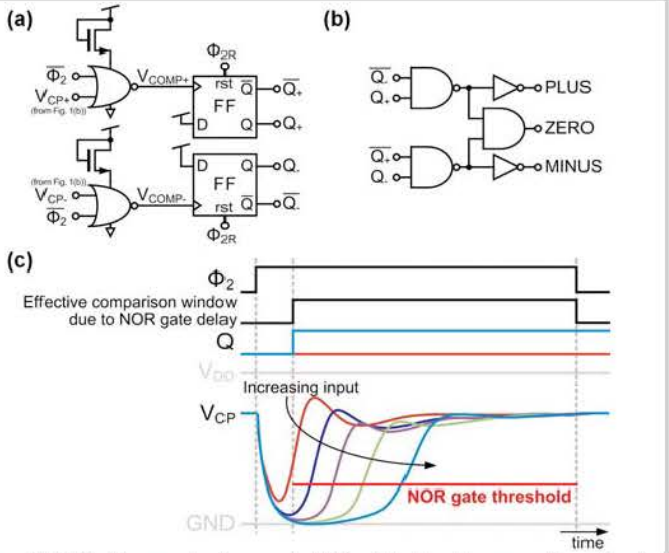

Figure 11.5.3: Comparator-less sub-ADC, (a) direction-sampling circuit, (b) decoding logic, (c) sampling operation with time gating threshold.

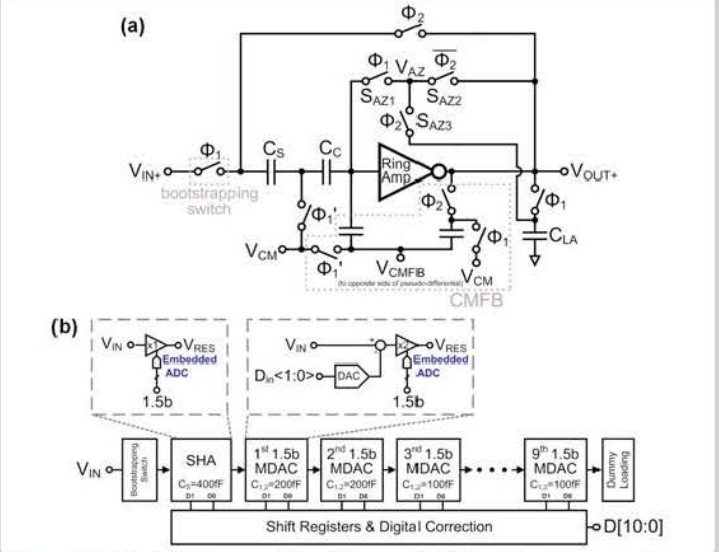

Figure 11.5.4: (a) Ring amplifier flip-around SHA with auto-zero scheme, (b) ADC structure.

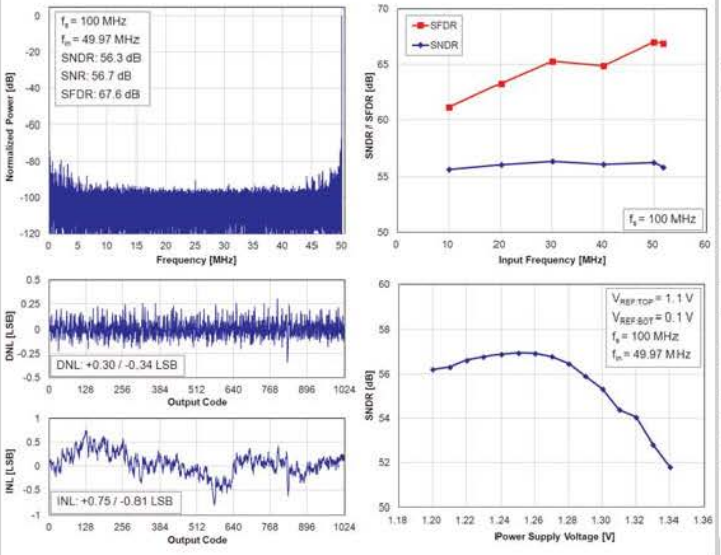

Figure 11.5.5: Measurement results.

	This Work	ISSCC2012 [1, 3]	VLSI2012 [2, 3]	VLSI2013 [4]
Resolution	10.5bits	15bits	10.5bits	15bits
Analog Supply	1.2V	1.3V	1.3V	1.3V
Amp. Structure	Self-biased ring amplifier only	Ring amplifier + split-CLS	Ring amplifier only	Coarse + fine ring amplifier
Sampling Rate	100MSPS	20MSPS	30MSPS	20MSPS
Technology	65nm 1P9M CMOS	180nm 1P4M CMOS	180nm 1P4M CMOS	180nm 1P4M CMOS
Active Area	0.097mm^2	1.98mm^2	0.50mm^2	1.98mm^2
Input Range	2V_{pk-pk} differential	2.5V_{pk-pk} differential	2.2V_{pk-pk} differential	2.5V_{pk-pk} differential
SNDR at Nyquist	56.3dB	~73dB (from [3] graph)	~57dB (from [3] graph)	-
SFDR at Nyquist	67.6dB	~85dB (from [3] graph)	~72dB (from [3] graph)	-
ENOB at Nyquist	9.06bits	~11.83bits	~9.18bits	-
Total Power	2.46mW	5.1mW	2.6mW	2.96mW
FoM (with the best result)	46.1fJ/conv-step	45fJ/conv-step	90fJ/conv-step	29fJ/conv-step
FoM (with Nyquist freq.)	46.1fJ/conv-step	70fJ/conv-step	149.4fJ/conv-step	-

Figure 11.5.6: Performance comparison with conventional ring amplifier based pipeline ADCs.

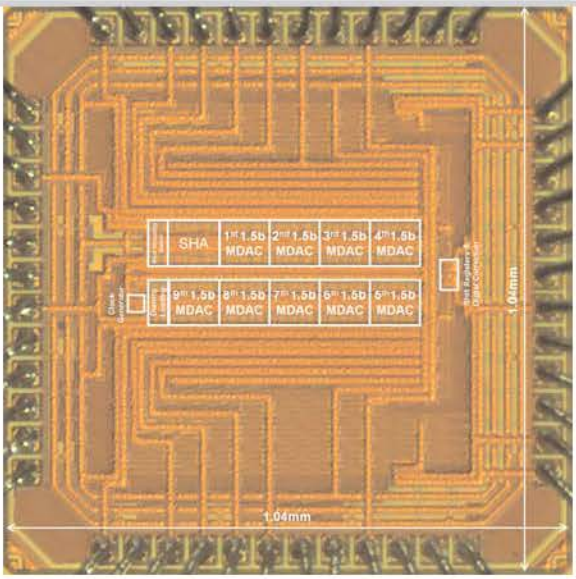

Figure 11.5.7: Die micrograph.

978-1-4799-0920-9/14/$31.00 ©2014 IEEE