A 400-Msample/s, 6-b CMOS Folding and Interpolating ADC

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Abstract— A 400-Msample/s, 6-bit CMOS folding and interpolating analog-to-digital converter (ADC) is described. A low-impedance current-mode approach is adopted. Current-division interpolation incorporated within the folders allows fast operation and is compatible with low supply voltages. This interpolation scheme, together with a short aperture comparator, gives good performance for input frequencies up to one-quarter of the sampling rate without using a sample and hold. For simplicity, the ADC uses only a single clock and its complement. The device is implemented in a 0.5-μm BiCMOS technology using only CMOS devices. The converter occupies 0.6 mm^2 and dissipates 200 mW from a 3.2-V supply.

Index Terms—Analog-to-digital conversion, CMOS, folding.

I. INTRODUCTION

FAST LOW-RESOLUTION converters have application in hard-disk-drive read channels, local-area-network interfaces, and communication circuits. Sampling speeds of up to 400 Msamples/s are now required. In all these applications, there are severe constraints on power consumption and die area. Bipolar transistors usually simplify analog circuit design; however, for reasons of cost and integration, CMOS is the technology of choice.

Variations of the flash technique are usually chosen for fast low-resolution converters. The flash technique is conceptually straightforward and offers good performance. A 200-Msample/s, 400-mW CMOS, 6-bit flash converter was reported [1]. Recently, a 400-Msample/s, 200-mW CMOS [2] device and a 350-Msample/s BiCMOS [3] device were described. Interpolation is used in a 6-b, 175-Msample/s flash analog-to-digital converter (ADC) [4]. The major disadvantage of the flash architecture is that the number of comparators grows exponentially with resolution; this has implications for area and power consumption.

In essence, folding is a technique to reduce the number of comparators used in the flash architecture. Concepts similar to folding date back to the earliest data converters [5]. Abel and Kurtz describe an early folding converter [6]. In many ways, the operation of shaft encoders (i.e., angle-to-digital converters) is similar to folding. Interpolation and *coarse-converter/fine-converter* synchronization are also used in some of these systems [7].
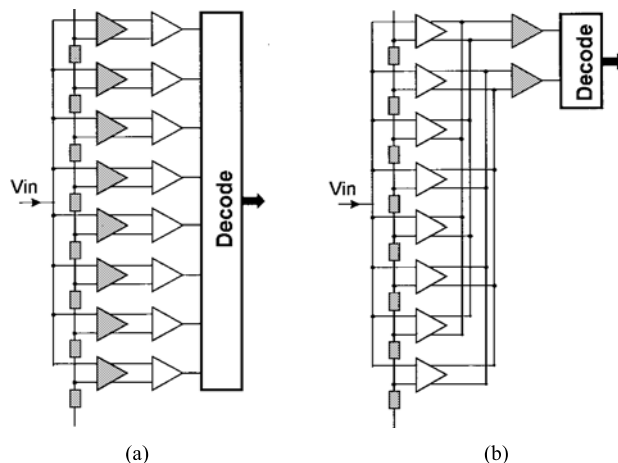
Fig. 1. (a) A 3-bit flash and (b) a 3-bit flash modified so that only two comparators are used.

Bipolar folding and interpolating converters with resolutions in the 6–12-bit range have been reported [8]–[10]. A 100-mW, 100-MHz 6-bit device for use in magnetic recording read channels was described [11]. A 6-bit, 4-Gsample/s folding converter is implemented in a 26-GHz heterojunction bipolar transistor process [12]. The lower transconductance and relatively poor matching of MOS transistors makes MOS technology less suitable for this type of converter architecture. Nevertheless, CMOS folding converters, with resolutions of 8–10 bits and sampling speeds of up to 100 MHz, have been reported [13]–[15].

In this paper, we show that the folding-and-interpolating technique is useful for fast, low-resolution CMOS converters. Section II is a brief introduction to folding. A low-voltage folding-and-interpolating scheme is described in Section III. A short-aperture comparator is described in Section IV. In this design, cascodes and biases are used sparingly. Only a single clock and its complement are used. Last, some experimental results are presented.

II. REVIEW OF FOLDING

Folding can be understood in the context of a flash-type converter. We begin with a very simple converter and show how it is modified to include folding. As an example, a simplified 3-bit converter is shown in Fig. 1. A 3-bit flash-type converter compares the input signal with seven, or sometimes eight, reference levels. A decoder converts the thermometer-code comparator output to a binary representation. The first stage is an amplifier and the second is a latching comparator.
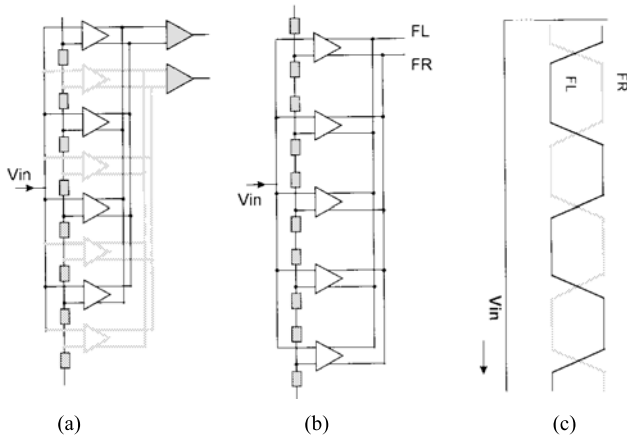
Fig. 2. (a) In this figure, a simple folder is highlighted. (b) A practical folder has an odd number of amplifiers. (c) The differential outputs are plotted.
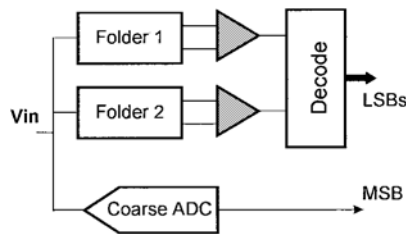

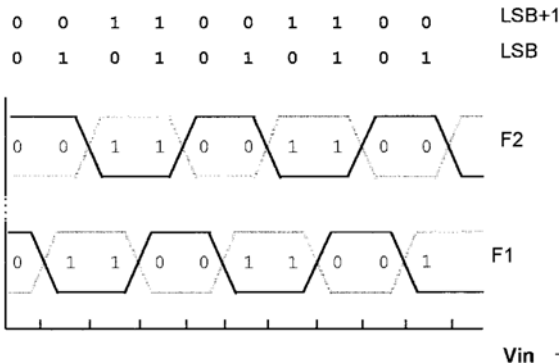Fig. 3. A more complete diagram of a 3-bit folding converter.

Fig. 4. The figure shows the cyclic code generated by the two comparators. The 2-bit decoded binary value is also shown.

A flash converter has a separate comparator for each possible code. This parallelism is what gives the technique its speed. However, at any time, only a few comparators (those around the transition of the thermometer code) provide useful information. We can exploit this redundancy to reduce the number of comparators. In Fig. 1(b), the 3-bit ADC is redrawn to have just two comparators. In this conceptual diagram, the combined output of four amplifiers drives each comparator.

This combination of amplifiers is known as a folder. In practice, a folder consists of an odd number of amplifiers. In Fig. 2(a), the 3-bit ADC is redrawn with two folders, each comprising five amplifiers. A single folder is highlighted [Fig. 2(b)], and its differential outputs FL and FR are plotted [Fig. 2(c)]. The polarity of the differential output signal changes each time the input voltage reaches a reference-voltage value. In this way, the input signal is "folded" at each reference voltage.
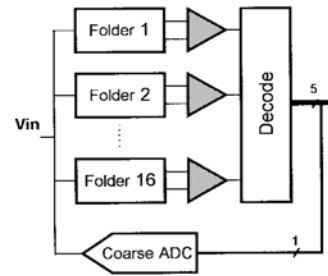

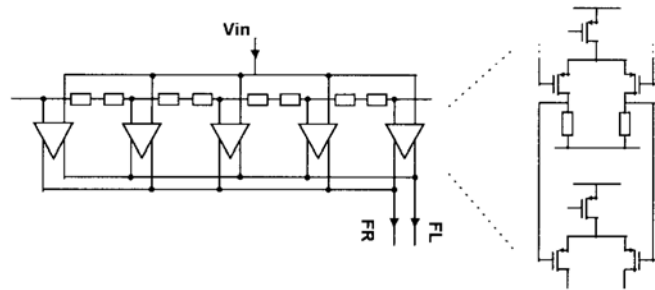Fig. 5. Block diagram of the 6-bit converter.

Fig. 6. The folder is made of five two-stage amplifiers. The reference ladder is shared among all the folders.

Folding reduces the number of comparators, but some information is lost. For this 3-bit converter example, the two comparator outputs are decoded to give the two least significant bits (LSB's) of the 3-bit conversion (Fig. 3). A separate coarse converter is required to decide the most significant bit (MSB).

Fig. 4 shows how the differential output signals from the two folders vary with input voltage. The polarity of a folding signal changes with each crossing of a reference voltage. The reference-voltage taps for the two folders are offset, so the two sets of folding signals are similar but shifted. The figure also shows the corresponding comparator outputs and the decoded binary value. This comparator output is sometimes referred to as a cyclic thermometer code.

III. THE FOLDER

Compared with the flash architecture, the number of comparators in a folding converter is reduced by the number of useful folds. In the 3-bit example, we fold by four, reducing the number of comparators to two. The choice of the degree of folding is a tradeoff between the reduction in the number of comparators and the increased speed of the folding signals. If the input is a full-scale sinusoid of frequency F_{in}, and there are N useful folds, then the frequency of the folded signals approaches $(\pi/2)N \cdot F_{in}$. (The $\pi/2$ appears because the maximum slope of a sinusoid is $\pi/2$ greater than that of a triangular waveform.)

In this 6-bit implementation, we fold by four, so that 16 comparators are required. In Fig. 5, 16 folders, producing 16 offset folding signals, drive 16 comparators. The cyclic thermometer code generated by the 16 comparators is decoded to give the five LSB's of the conversion.[1] A separate 1-bit coarse ADC determines the MSB.

[1] A cyclic code contains one more bit of information than a thermometer code of the same length.

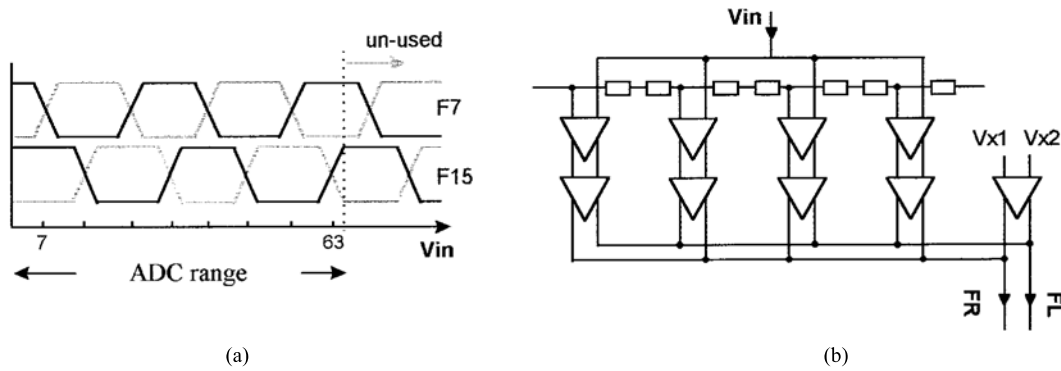(a)   (b)

Fig. 7.   (a) The contribution of the fifth amplifier goes unused. (b) This redundancy is used to reduce the number of preamplifiers.
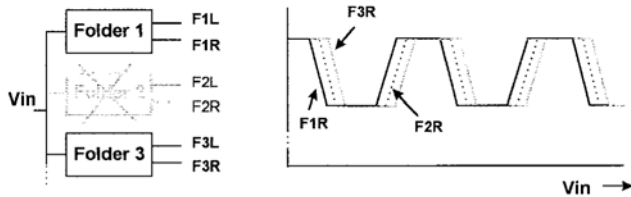

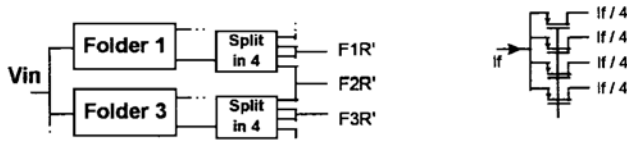Fig. 8.   Interpolation can be used to eliminate half or more of the folder blocks.

Fig. 9.   Interpolation with current-mode folder signals. A current split-in-four block is shown on the right.

Fig. 6 shows an individual folder block. To provide adequate transconductance, the amplifiers are implemented in two stages [13]. The first stage (preamplifier) is a simple amplifier. For simplicity, resistor loads are used instead of active loads. In addition, linear resistors offer better transient performance for the overall converter. The outputs of the second stage, and of the overall folder, are differential currents. To maximize speed, a low-impedance, or current-mode, approach is adopted.

As noted earlier, each folder should have an odd number of amplifiers. Fig. 7(a) shows two of the 16 differential folded signals and also indicates the converter input range. In all cases, the reference voltage for the fifth amplifier lies outside the converter range, so this fifth amplifier is normally not exercised. We can use this redundancy to reduce preamplifier power consumption. The fifth preamplifier is replaced with a fixed voltage. In Fig. 7(b), the fixed voltages $V\chi 1$ and $V\chi 2$ drive the fifth amplifier. In practice, a single preamplifier generates a DC bias that is shared among all the fifth amplifiers in all the folders.

The 16 folding signals are similar in shape but are offset from each other. Because of this similarity, we can derive some of these signals by interpolation. This is illustrated in Fig. 8. The differential folding signals F2L and F2R can be approximated by the average of the F1 and F3 differential folding signals. In this way, we can eliminate half of the folders. Not only does interpolation save power and area but

it also tends to reduce differential nonlinearity (DNL) errors caused by input offsets of the folders [16].

In folding converters where the folders produce a voltage output, interpolation can be realized with resistors [7]. In this case, the folder outputs are currents, and interpolation is implemented with a current-division technique [13]. This concept is illustrated in Fig. 9 (for clarity, only one of the differential signals is shown). The outputs from folder 1 and folder 3 feed to two "split-in-four" blocks. A quarter of the folder 1 output is added to a quarter of the folder 3 output to represent the interpolated signal F2R′. Two quarters of the folder 1 output are summed to form F1R′, and similarly, two quarters of the folder 3 output are summed to from F3R′. In practice, a current division or splitting block can be implemented with an array of identical MOS transistors [13]. If we use four parallel transistors, then a quarter of the current flows through each MOS device. This technique has two problems: it adds an extra node to the signal path, reducing the bandwidth of the folder circuit, and does not work readily at low supply voltages.

To avoid these problems, we integrate current division within the folder. Both the folder and its amplifiers are modified (Fig. 10). The first stage, or preamplifier, remains the same. The differential pair of the second stage is now composed of two sets of four devices, and a quarter of the current flows through each. Two sets of three wires collect the current-divided outputs of the amplifiers. The two sets of folder outputs deliver three divided differential folding currents 1/4, 1/4, and 1/2. There are no extra nodes in the signal path, so the circuit is fast. For the same reason, the circuit is compatible with low-voltage operation.

Fig. 11 shows how the modified folder is incorporated within the ADC. There are eight folder blocks, which generate eight sets of differential, current-divided, folded signals. These signals form the 16 differential current inputs to the 16 current comparators.

IV. COMPARATOR

As we saw earlier, the folding signals change fast, much faster than the ADC input. A fast comparator with a short aperture is required. Variations in the comparator input after the decision "snap-shot" time should not influence the overall decision. In addition, the comparator clocking should be simple.
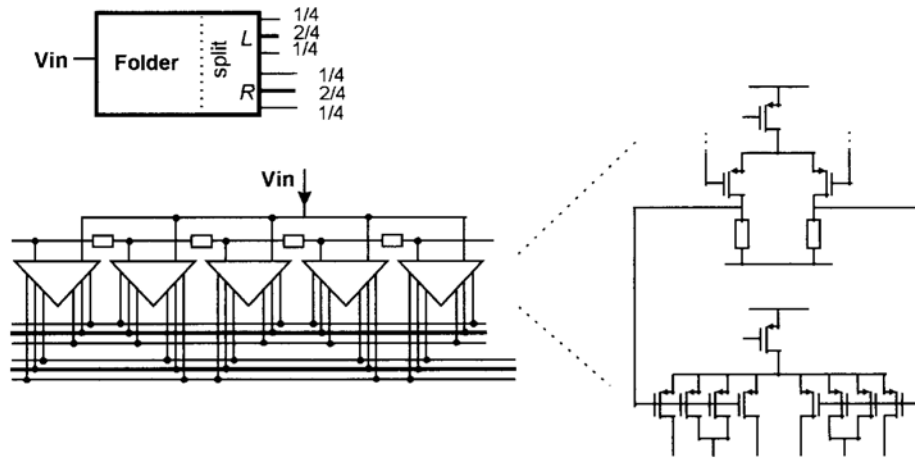
Fig. 10. The folder is modified to include current division. The modified amplifier is on the right. A block diagram for a modified folder is also shown.
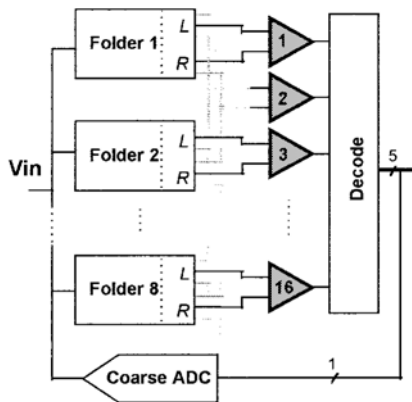

Fig. 11. ADC block diagram.

An emitter-coupled-logic-like structure is used (Fig. 12). The differential comparator output appears across the two load resistors R1 and R2. M7 and M8 are cross-coupled latching transistors. The switches M3–M6 steer current either directly to the resistors or to the latching devices. A low impedance input is assured by two NMOS cascode devices M1 and M2. The circuit has two modes: *tracking and latching.*

When Clk is low, switches M3 and M6 are on. The comparator is in tracking mode and the differential output voltage (OutL, OutR) follows variations in the comparator input. When Clk goes high, *latching* begins. The direct path to the resistors is broken. Instead, the two currents are summed together and power-up the cross-coupled latching transistors (M7 and M8). The regenerative action of M7 and M8 quickly forms a decision. This decision is based on the output voltage at the very end of the tracking phase.

This structure has some important advantages. Because currents are summed to drive the latching devices, the input signal has very little effect after latching begins. Because there is always a path for the current to flow, the folders are little disturbed when the comparators change from tracking to latching. Last, because the output swing is small, the comparison is fast.

While this comparator is fast and has a short aperture time, it does pose some design challenges. As we see in Fig. 13,

the output is not a full CMOS signal and is valid for less than one-half clock cycle. In addition, the output node is sensitive to loading and must be buffered. A simple source follower performs this function. A more serious problem is that the first stage is very sensitive to kickback from subsequent stages; this can cause unwanted memory or hysteresis effects.

The second stage buffers and latches the first-stage output (Fig. 14). In essence, it contains two differential amplifiers that drive an unclocked set–reset latch. The switches to ground (M1 and M2) at the outputs of the differential amplifiers perform an important function. During tracking, they prevent the amplifiers from changing the state of the latch, effectively disconnecting the latch from the first stage. Furthermore, at the beginning of the latching phase, both amplifier outputs are at ground, so hysteresis effects are reduced.

A comparator is "metastable" when its output falls between the logic high and logic low threshold voltages. The probability of comparator indecision or metastability is related to comparator gain. An additional latching stage (another SR latch) is added to increase the overall comparator gain (Fig. 15). The three comparator stages work in a master–slave fashion; the first two stages sample the input currents on the rising edge of Clk. Half a clock cycle later, the state of the SR latch is clocked into the final stage.

V. COARSE ADC AND DECODER

A more complete block diagram of the converter is given in Fig. 16(a). As we saw earlier, the cyclic thermometer code generated by the comparators in a folding ADC is more complex than the thermometer code of a flash ADC. However, because the number of comparators is reduced, the size of the decoding block tends to be smaller. The decoding logic also suppresses "bubbles" in the cyclic code [13].

Care is taken to match the delay through the coarse ADC and the delay through the rest of the circuitry (i.e., the fine converter). The same comparator structure is used. However, even small timing differences can cause large errors, and there may also be a DC offset between the two circuit blocks. A synchronization ("sync") circuit suppresses these mismatches.
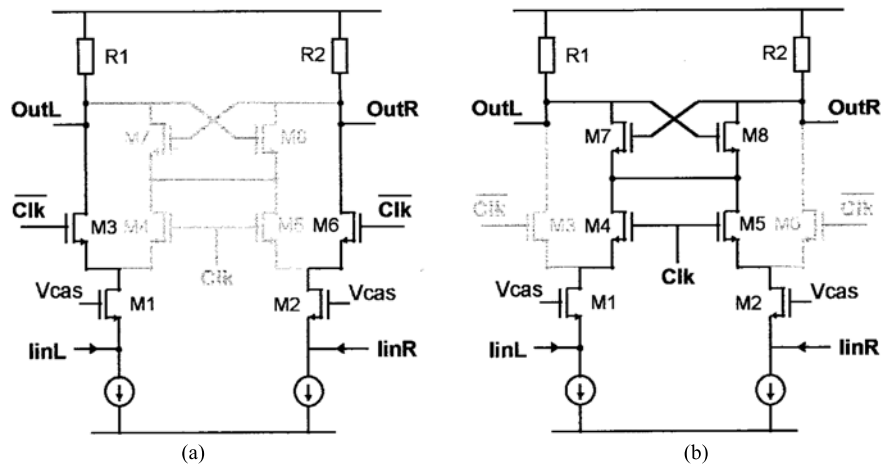
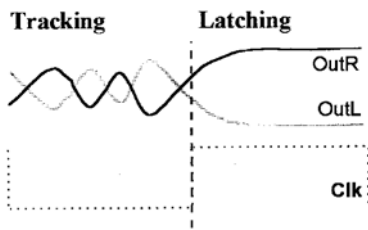Fig. 12. The comparator core (a) tracking and (b) latching.

Fig. 13. Output voltage of comparator first stage during tracking and latching.
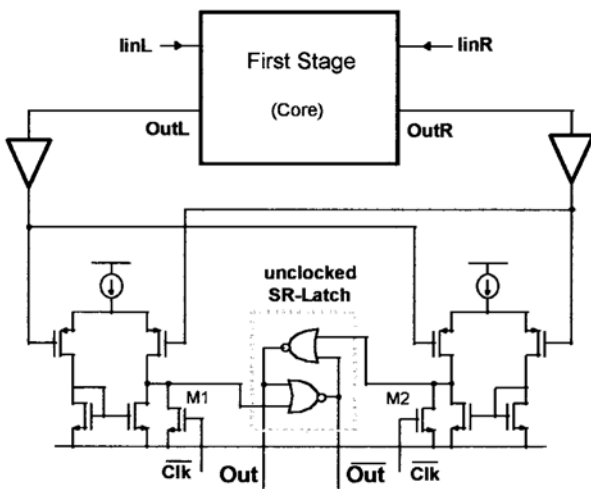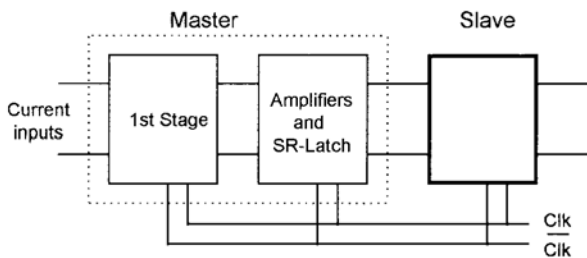

Fig. 14. Comparator second stage.

Fig. 15. Three comparator stages.

Although usually drawn separately, the sync block is really an integral part of the coarse ADC. Instead of a single

comparator, the 1-bit coarse ADC has two comparators, offset by 1/8 full scale, at either side of the MSB transition voltage. In Fig. 16, these signals are labeled MSB_Lo and MSB_Hi. MSB-1 is the most significant of the five bits generated by the folding section. If there is no mismatch, then the state change of MSB should coincide exactly with the half-scale state change of MSB-1. To suppress mismatches, we use MSB-1 to decide when the state change of MSB should occur. When MSB-1 is zero, the sync block selects MSB_Lo as the converter MSB. When MSB-1 is one, MSB_Hi is selected as the MSB value. Because the MSB transition is fixed by MSB-1, this scheme can tolerate a relative offset of up to ±1/8 full scale in the MSB_Lo or MSB_Hi decisions.

VI. TEST RESULTS

A prototype 6-bit converter was fabricated in a 0.5-μm BiCMOS technology. Only CMOS transistors are used. The minimum transistor gate length is 0.42 μm. The resistor ladder is implemented using gate polysilicon. The larger resistors are implemented with 250 Ω/sq. unsilicided polysilicon. The power dissipation, including the power dissipation of the resistor ladder, is 200 mW from a 3.2-V supply.

The device is packaged in a 64-pin thin quad flat package ceramic package. During evaluation, the ADC was mounted in a low-inductance socket. At 400 Msample/s with a 1-MHz full-scale (2.3 V) sinusoidal input, the measured signal-to-noise-and-distortion ratio (SNDR) is 33.6 dB or 5.3 effective bits (maximum DNL = 0.9 LSB). The measured total harmonic distortion (THD) is −44 dB. Fig. 17 shows the corresponding fast Fourier transform (FFT). Fig. 18 shows the variation of SNDR with input frequency. With a full-scale 100-MHz input, the SNDR drops to 29.2 dB (THD = −33.6 dB). When the sampling frequency is increased to 450 MHz, the measured SNDR drops to 32.9 dB or 5.2 effective bits (THD = −40.5 dB), again with a 1-MHz full power input.

Using the technique described in [14], at 400 Msample/s with a 51-MHz input, no metastability was observed in 2× 10^8 samples. The circuit has an area of 0.6 mm^2. Excluding pad and package capacitance, the converter has an input capacitance of 1.4 pF. A die photo is given in Fig. 19. The experimental results are summarized in Table I.
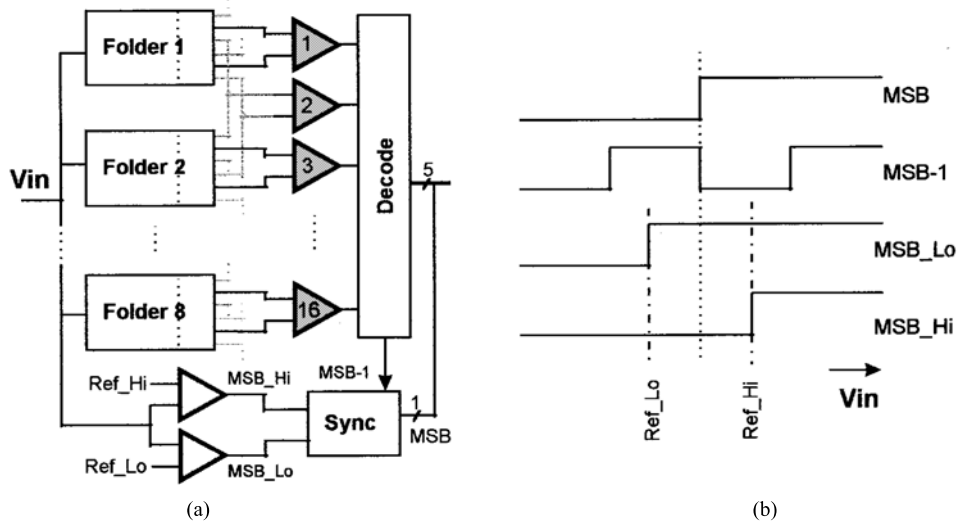
Fig. 16. (a) ADC block diagram with detail of coarse ADC. (b) Coarse ADC waveforms.
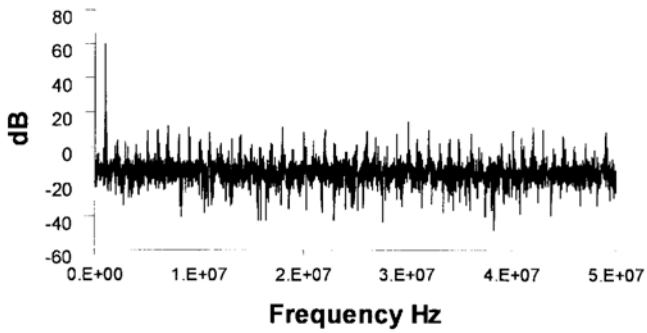

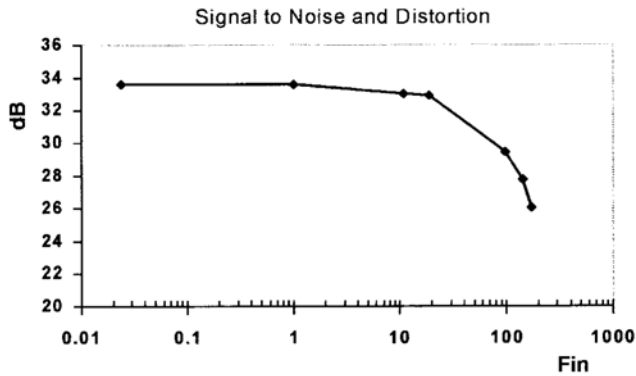Fig. 17. FFT for 1-MHz sinusoid sampled at 400 Msample/s (decimated).

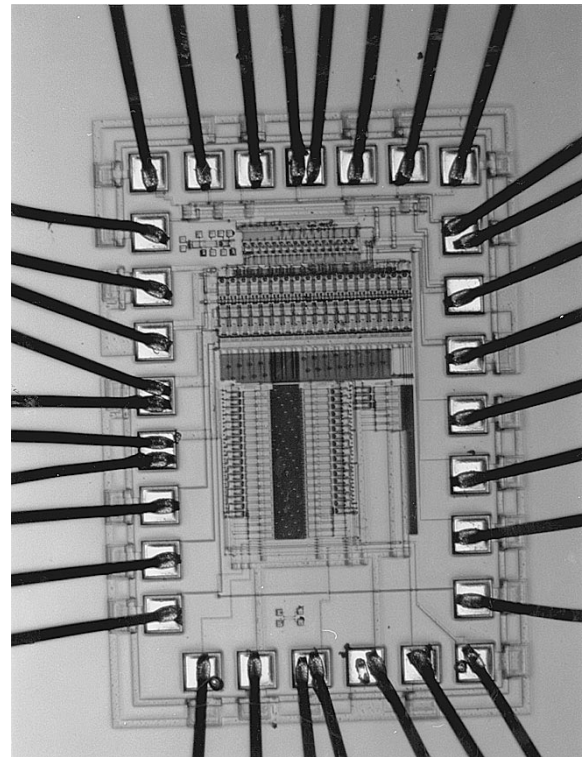Fig. 18. SNDR versus input frequency at 400 Msample/s.

Fig. 19. Die photo.

VII. CONCLUSION

The folding technique is useful for low-resolution fast CMOS analog-to-digital converters. A simple current interpolating scheme together with a short-aperture comparator give good performance. As with all folding converters, the dynamic performance can be further improved if the input signal is sampled and held.

TABLE I
PERFORMANCE SUMMARY

Technology	0.5mm BiCMOS (CMOS only)
SNDR (1MHz sine-wave)	33.6dB @ 400Msample/s
	32.9dB @ 450Msample/s
Supply voltage	3.2V
Power	200mW
Area	0.6μm²
Input capacitance	1.4pF

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