A Bidirectional Neural Interface Circuit With Active Stimulation Artifact Cancellation and Cross-Channel Common-Mode Noise Suppression

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***Abstract*—This work presents a bidirectional neural interface circuit that enables simultaneous recording and stimulation with a stimulation artifact cancellation circuit. The system employs a common average referencing (CAR) front-end circuit to suppress cross-channel environmental noise to further facilitate use in clinical environment. This paper also introduces a new range-adapting (RA) SAR ADC to lower the system power consumption. A prototype is fabricated in 0.18 μm CMOS and characterized and tested *in vivo* in an epileptic rat model. The prototype attenuates stimulation artifacts by up to 42 dB and suppresses cross-channel noise by up to 39.8 dB. The measured power consumption per channel is 330 nW, while the area per channel is $0.17\ \mathrm{mm}^2$.**

***Index Terms*—Closed-loop stimulation, low power, neural recording, noise cancellation, SAR ADC.**

I. Introduction

STUDIES have shown that neurostimulation, or direct current stimulation of neural tissue, significantly lessens symptoms in patients with neurological disorders. A 2-year study of a responsive neurostimulation system (NeuroPace) observed an average seizure reduction of 50% in 191 epilepsy patients [1]. Likewise, deep brain stimulation (DBS), a popular neurostimulation technique for treatment of various neurological diseases, has improved the quality of life for many patients worldwide [2]. Further adoption of neurostimulation as mainstream clinical treatment will be enabled in part by miniaturization of the electronics used to deliver stimulation current. A small form factor is important for implantable systems, while low power consumption is essential for long-term chronic deployment. Automated control of neurostimulation systems is also highly desired, as it would minimize patients' need for medical supervision and hospital visits. In an automated system, a closed-loop neural interface controls current stimulation to a particular brain region by monitoring the recorded neural signal from the neighboring neural tissue and adjusting stimulation parameters in a feedback fashion. Fig. 1 demonstrates the general concepts where a closed-loop controller detects seizure-related biomarkers at the onset of a seizure and triggers a current pulse train to suppress the seizure. Such systems have been proven to successfully lower seizure occurrence rate [3], [4].

Recent research on neural interface systems has focused on reducing system power consumption and footprint area [5]–[7]. However, this research has rarely addressed problems related to the noisy environment and the side effects of stimulation. Proper operation of a closed-loop neural interface microsystem requires simultaneous recording and stimulation. In practice, continuous monitoring during stimulation presents a challenge due to large saturating artifacts appearing with the signal, as described in more detail in Section II. Only a few published techniques, such as signal blanking or symmetrical differential stimulation and recording, attempt to mitigate this problem [8], [9]. However, limitations in sensing capability and electrode design make these techniques unsuitable for universal use. In addition, recorded signals can be corrupted by common-mode environmental noise, which can come from motion artifacts or can be coupled from the power lines. This coupled noise significantly reduces the signal-to-noise ratio (SNR) in the recording channel.

To combat these problems, we present a novel neural interface system architecture incorporating new signal conditioning front-end features [10]. A mixed-signal adaptive stimulation artifact cancellation circuit removes stimulation artifacts at the front-end of the recording channels to prevent preamplifier saturation. A noise removal technique called common average referencing (CAR), implemented at the front-end, removes cross-channel common-mode noise and improves channel SNR. In addition, a new range-adapting (RA) SAR ADC architecture provides more power efficient digitization of the neural signal. These features, as well as other relevant system-level details, are presented in this paper in the following way. Section II discusses the cause of stimulation artifacts and explains the stimulation artifact cancellation algorithm. Section III analyzes the sources of common-mode noise and introduces the CAR algorithm. Section IV describes the circuit implementation of the new architectural elements as well as the new RA SAR ADC. Sections V and VI show recording channel characterization and *in vivo* measurements, respectively. Finally, conclusion is drawn in Section VII.

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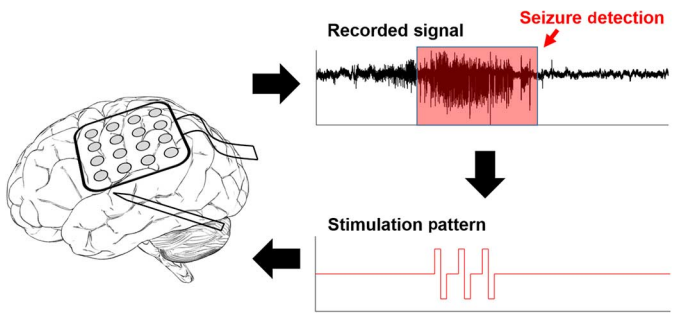

Fig. 1. Concept diagram of closed-loop stimulation for seizure suppression.

II. Stimulation Artifact Cancellation

A. Cause of Stimulation Artifacts

Stimulation artifacts inherently form at the recording interface during concurrent sensing and stimulation. Fig. 2 depicts simultaneous stimulation and recording and shows the corrupted recorded signal. We expect a stimulation-injected current to travel to a nearby neuron to affect its state by either triggering or inhibiting its spiking activity, while the recording probe monitors the neuron's activity throughout this process. Unfortunately, due to proximity of the recording and stimulation probes, a fraction of the stimulation current bypasses the neural tissue and directly couples onto the recording probe. Because the direct path is short and the stimulus current is usually larger than the neural extracellular ionic currents, the resulting stimulation artifact dominates the recorded signal. This leads to two problems. First, the large artifact current can saturate the sensitive preamplifier, causing signal loss and lowering the biomarker detection rate. An increased dynamic range (DR) might mitigate this problem but at the cost of high power consumption. Second, even if the artifacts do not saturate the amplifier, they might be mistaken for the biomarkers themselves, leading to a high false biomarker detection rate.

While there are many ways to alleviate the degraded performance, the most direct and best performing strategy is to cancel the artifacts as early as possible in the recording signal chain to prevent saturation and signal loss. Previous approaches to artifact cancellation include signal blanking and symmetric sensing. In signal blanking, the input to the recording amplifier is simply turned OFF during stimulation [8]. While this prevents the amplifier from saturating and temporarily losing its input voltage bias, any signal appearing during the off-period is lost. In symmetric sensing, the recording and stimulation electrodes are placed in a particular configuration to differentially cancel the artifact [9]. Here, the stimulation site is placed equidistantly between two differential recording sites so that the artifact equally couples onto each recording channel is rejected by the differential amplifier. While the neural signal is preserved in this scheme, it requires an inflexible electrode configuration that possibly hinders the effectiveness of the stimulation. Instead, our adaptive approach provides a universal architecture for artifact cancellation in a wide variety of applications that preserves the recorded neural signal while avoiding the shortcomings of previous works.

B. Adaptive Cancellation of Artifacts

Our approach to artifact cancellation circuit stems from the similarity in coupling between stimulating and recording probes of a closed-loop stimulation microsystem to the near-end crosstalk (NEXT) problem in wireline communication systems. In NEXT, a strong transmitter output couples to the input of the sensitive receiver amplifier and corrupts the received signal, increasing the system's bit-error rate [11], [12]. However, by utilizing the direct correlation between the transmitted signal and the observed artifact, a number of filtering techniques have been developed to cancel the artifacts. One such technique, called *adaptive noise cancellation*, learns the filtered crosstalk noise response of the channel and subtracts it from the recorded signal [13]. Due to its simplicity and general applicability, we apply a similar approach to cancel neural stimulation artifacts in an implantable neural interface [14].

Analysis of the algorithm begins with the simplification of neural tissue response to a linear time-invariant (LTI) filter. The recorded signal $y(t)$ can be expressed as a linear sum of the neural signal $x(t)$ and the artifact $a(t)$ as shown in Fig. 3. Furthermore, the artifact $a(t)$ can be expressed as a stimulation signal $s(t)$ filtered by the neural tissue response $b(t)$

$$y(t) = x(t) + a(t) = x(t) + b(t) * s(t). \tag{1}$$

Adaptive noise cancellation artificially recreates the response of the neural tissue in order to subtract it from the corrupted signal. To perform this task, an adaptive filter $\hat{b}(t)$ (in Fig. 3) learns the impulse response of the neural tissue. When stimulation $s(t)$ is fed through this filter, its output recreates the artifact $\hat{a}(t)$ and this recreated artifact is subtracted from the recorded signal to cancel the real artifact as shown in the following equation:

$$\begin{aligned}\hat{x}(t) &= ex(t) + a(t) - \hat{a}(t)\\ &= x(t) + b(t) * s(t) - \hat{b}(t) * s(t).\end{aligned} \tag{2}$$

By inspection of the equation above, when the fully trained filter $\hat{b}(t)$ approximates the neural response $b(t)$, the stimulation term *s(t)* is cancelled, and the recovered output signal $\hat{x}(t)$ approximately equals the original neural signal $x(t)$.[1]

A key block in adaptive noise cancellation is the learning algorithm of the adaptive filter. The least mean squares (LMS) learning algorithm, first presented by Widrow *et al.* and extensively used in telecommunications, is simple and reliable [15]. In LMS, the adaptive filter coefficients are updated every cycle to better approximate the desired response. The update quantity is derived by applying the steepest gradient descent approach to minimize power of the noise error $\hat{x}(t)$. As shown in [14], the online LMS algorithm predicts the coefficient update, needing only the value of the recovered output signal $\hat{x}(t)$ from the previous cycle and the stimulation input $s(t)$ as follows:

$$\hat{b}(t+1) = \hat{b}(t) + \mu s(t)\hat{x}(t). \tag{3}$$

[1]It is important to note that while the actual nonartifact neural response is also correlated to the stimulation signal, it is much delayed and not LTI; if the filter length is kept short enough, the real neural signal is not cancelled. The neural signal will thus be omitted in further explanation.

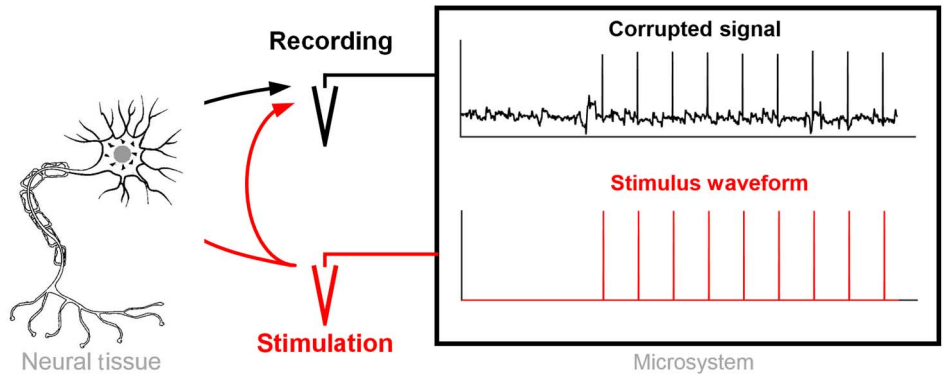

Fig. 2. Formation of stimulation artifacts and corruption of neural signal through direct coupling of stimulation signal to recording probe.

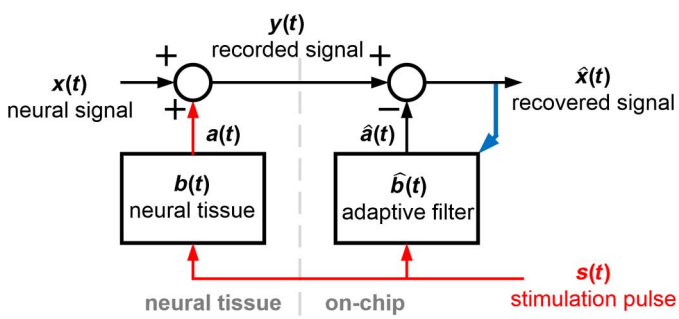

Fig. 3. System diagram of stimulation artifact addition and cancellation through adaptive filtering. The recorded signal $y(t)$ is the corrupted neural signal picked up at the tissue–circuit interface, while the recovered signal $\hat{x}(t)$ is the on-chip recovered neural signal.

The adaptation constant μ is an adjustable knob for the user to trade adaptation speed for accuracy. A simplified version, called sign–sign LMS, eases the hardware requirements by performing computation on a sign-bit signal representation, resulting in the following update equation [16]:

$$\hat{b}(t+1) = \hat{b}(t) + \mu((s(t) \times \text{sign}(\hat{x}(t))). \tag{4}$$

To show the effectiveness of the scheme, the algorithm is simulated with prerecorded neural data in Fig. 4. We artificially corrupt a known signal (here, a sinusoidal wave for clarity) with prerecorded artifact waveforms, added at predetermined times that are correlated to the stimulation waveform. As the algorithm runs for a few stimulation cycles, the filter output begins to resemble the added artifacts. In fact, the plotted impulse response of the adaptive filter at the end of simulation in Fig. 5 resembles a single added artifact, since the filtered artifact waveform is simply a pulse train convolved with a single eight sample long artifact-shaped sequence. Furthermore, the recovered signal shows a decrease in correlated crosstalk noise without significant distortion of the original uncorrelated signal.

The selection of the adaptive filter length was guided by maximizing the subtraction of artifact without removing the desired evoked neural potential. An analysis of typical electrocorticograph (ECoG) and local field potential (LFP) signals showed a 2 ms period between the stimulation pulse and earliest neural response, and during this time period, the artifact can be safely removed. Because the filter is sampled at the ADC frequency of 4 kHz, an 8 tap filter is sufficient to attenuate most artifacts while preserving the nonartifact neural response.

III. Common-Mode Noise Rejection

As studied in [17], various environmental noise sources such as power lines and fluorescent lights capacitively couple onto the electrodes, the electrode wires, and the preamplifier inputs, potentially causing large amplitude common-mode noise. This noise can be cancelled through differential recording, where noise in two neighboring channels is rejected as common-mode signal. Inconveniently, differential recording requires the user to double the number of electrodes and may also remove important signals shared between the channels. As a compromise, a large single reference electrode is often used to subtract the reference noise from multiple channels without introducing localized neural signals. Unfortunately, because of the impedance mismatch between the recording and reference electrodes, line noise couples differently to the positive and negative inputs.

Instead of relying on a single electrode to provide an accurate reference signal, we can create a new reference signal from the existing channels. Ref. [18] creates this new reference signal in a software postprocessing scheme called CAR. CAR has become a common step in signal conditioning in neuroscientific literature [19], [20]. As shown in Fig. 6, the new reference signal is computed by averaging neighboring channels and subtracting this average from every channel. If used properly, the average holds most of the common-mode noise and little of neural signal, thus providing a clean, stable reference signal.

While it has been previously implemented as a software postprocessing step, we implement CAR at the recording front-end. By cancelling the noise before final amplification and digitization, the DR constraints of the analog circuitry can be greatly relaxed. Challenges include unintended signal cancellation if the CM signal itself is of importance—this can be alleviated by averaging a sufficient number of channels so that the average contains a minimal amount of localized neural signal. Analysis of experimental neural data (in Fig. 7) shows that even a 4 channel CAR (CAR-4) can substantially improve SNR, while the use of 16 channel CAR (CAR-16) only slightly further increases SNR. This relatively small number of needed channels allows us to minimize the circuit area for CAR as described

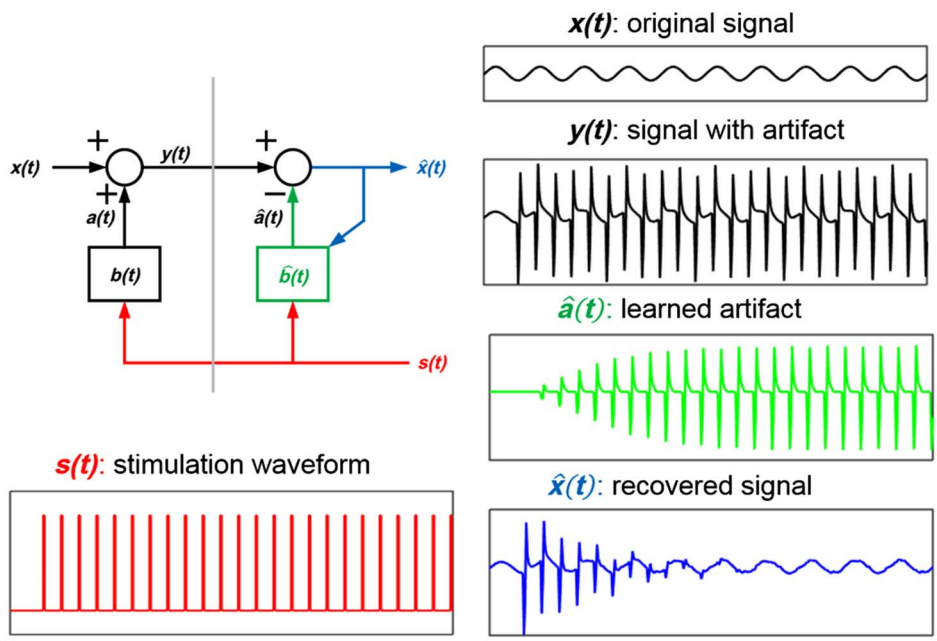

Fig. 4. Simulation of the stimulation artifact cancellation algorithm with artificial neural data showing the system learning the response of the tissue.

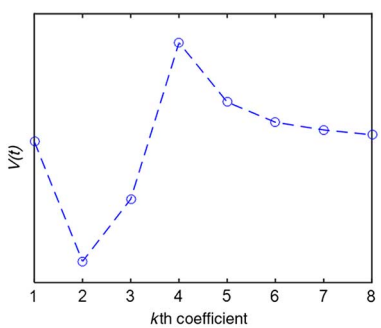

Fig. 5. Final impulse response of the adaptive filter after training resembles the artifact waveform.

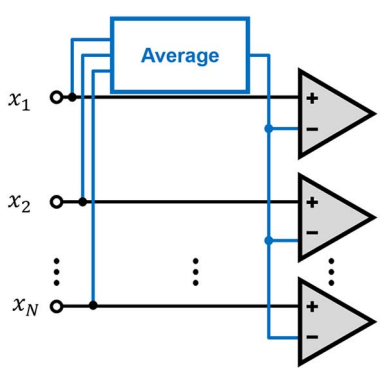

Fig. 6. Top-level diagram of CAR algorithm.

in Section IV-B. The common average reference can also be contaminated by a single very strong, or perhaps broken, channel. For this reason, the user should be able to eliminate that channel from the average calculation so that the noise does not bleed into other channels.

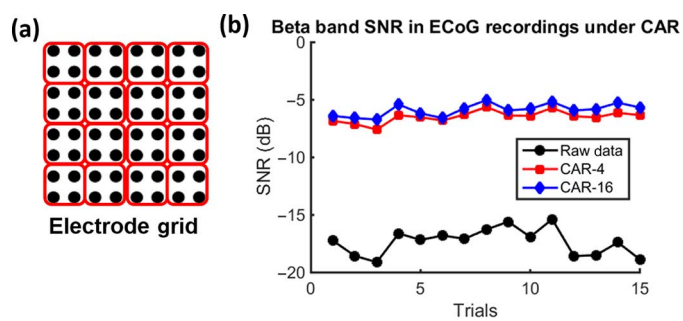

Fig. 7. (a) CAR-4 4 channel groupings mapped onto an ECoG electrode grid. (b) Comparison in SNR of ECoG recordings between raw data, active CAR-4, and active CAR-16 algorithms.

IV. Circuit Implementation

The proposed system architecture, shown in Fig. 8, consists of eight recording channels and four stimulation channels. Each recording channel consists of a preamplifier with a gain of 100, a programmable gain amplifier (PGA) with gain ranging from 1 to 10, and an ADC. The bandwidth of the preamplifiers is deliberately limited to a range of 1 Hz to 2 kHz to pass ECoG and LFP signals, which are most commonly used for neuromodulation control. The sampling rate of the ADC is set at 4 kS/s to properly sample the neural signals without aliasing. The resolution of the ADC is set to 10 bits to maintain the channel input-referred noise below 5 μV_{rms} (i.e., below the biological noise limit) while providing the ADC differential input DR of 1 V. The recording channels are split into two groups of four channels. In each group, every channel can be referenced to an average formed from any combination of these channels. The CAR circuit is placed after the preamplifier and before the PGA to remove the noise before final amplification and digitization. A stimulation artifact cancellation filter is implemented for every individual channel, as we cannot expect a similar coupled

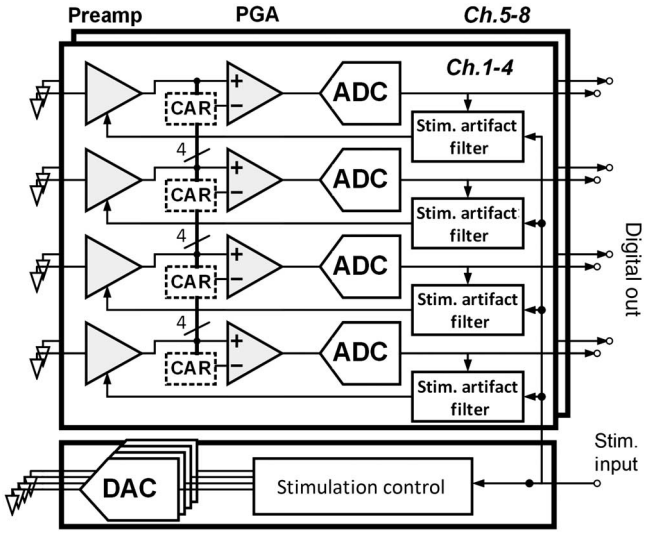

Fig. 8. Top-level system architecture.

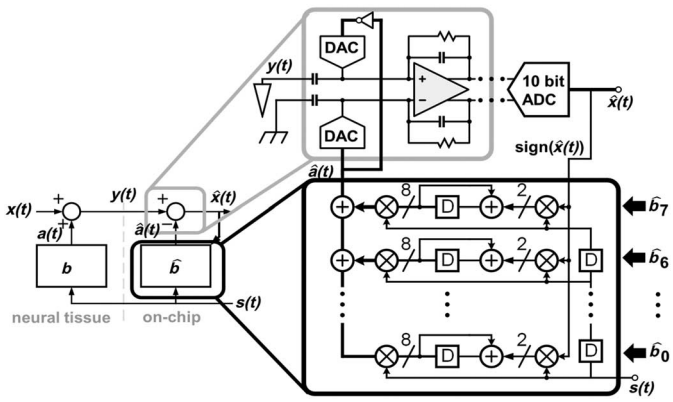

Fig. 9. Schematic of stimulation artifact cancellation circuit. Analog subtraction is framed in gray, while the adaptive filter is framed in black.

stimulation artifact for each channel. The stimulation data input is fed into the stimulation control block and also to the bank of stimulation artifact cancellation filters. Lastly, the stimulation channels themselves consist of current digital-to-analog converters (DACs) and digital timing and control circuitry. The current DAC resolution of 7 bits and DR up to 8 mA are enough for most neuromodulation applications.

A. Stimulation Artifact Cancellation Circuit

The stimulation artifact cancellation scheme is implemented with the mixed-signal circuit shown in Fig. 9. First, the single-bit stimulation input $s(t)$ is fed through the digital adaptive filter. The filter output, or the digitally recreated artifact $\hat{a}(t)$, is converted into a differential analog signal using two DACs. This analog artifact replica is then subtracted from the corrupted neural signal at the preamplifier input to prevent signal saturation in the channel. Finally, the sign of digitized recovered signal $\hat{x}(t)$ (from the 10 bit ADC) and single-bit stimulation signal $s(t)$ are fed to the adaptive filter to train its coefficients.

A pair of capacitive DACs converts $\hat{a}(t)$ into a differential analog signal. The DAC's 8 bit resolution is chosen to reduce

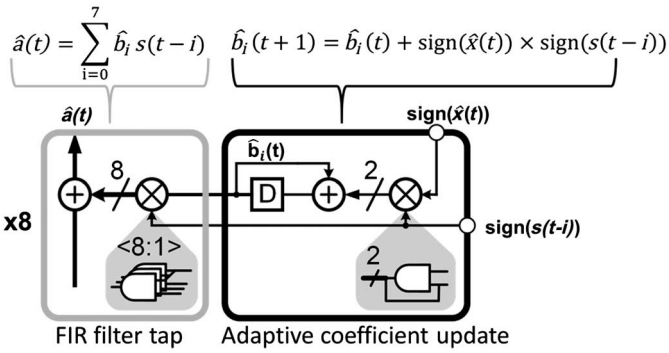

Fig. 10. Schematic of a single filter tap implementing LMS update and filter multiply and accumulate.

artifacts by up to 42 dB. From data analysis, this is sufficient to prevent channel saturation in most situations. While an increase in resolution would only result in a marginal increase in power consumption (less than 1 nW per channel for every additional bit), the area of the DAC would increase exponentially with extra resolution, since the LSB capacitor size is limited by mismatch. The 8 bit DAC resolution allows us to keep the area of the DAC below 12% of the complete channel layout area. A further advantage is that the capacitive DAC architecture offers the ability to scale the DAC LSB size, which corresponds to the μ step size of the learning algorithm in (4), by adjusting the capacitive DAC reference voltage.

A standard 8 tap LMS digital adaptive filter nominally requires 16 multipliers and 15 adders to perform necessary computations, significantly contributing to the system power consumption and area. To minimize this overhead, we propose a simplified parallel architecture that eliminates computation elements by utilizing the sign–sign LMS algorithm in (4) that takes advantage of the simplified single-bit inputs.

First, the adaptive filter coefficients are updated by the following matrix combination:

$$\begin{bmatrix} \widehat{b_0}(t+1) \\ \widehat{b_1}(t+1) \\ \vdots \\ \widehat{b_7}(t+1) \end{bmatrix} = \begin{bmatrix} \widehat{b_0}(t) \\ \widehat{b_1}(t) \\ \vdots \\ \widehat{b_7}(t) \end{bmatrix} + \mathrm{sign}((\widehat{x}(t)) \begin{bmatrix} s(t) \\ s(t-1) \\ \vdots \\ s(t-7) \end{bmatrix}. \quad (5)$$

The sign of the error (or recovered) signal $\hat{x}(t)$ is represented by the MSB of the recorded signal, and it is taken directly from the ADC output. The single-bit stimulation input, which represents a stimulation pulse with 1 and a lack of stimulation with 0, is fed from the stimulation circuit and is appropriately delayed by a shift register for each of the eight taps. The eight coefficient updates in (5) are then computed in parallel. Fig. 10 shows the hardware implementation of a single filter tap and coefficient update. On the right-hand side of Fig. 10, the single-bit $s(t-i)$ input is multiplied by the sign of $\hat{x}(t)$. This multiplication, performed only with a single AND gate and a direct node connection, yields a 2 bit number representing -1, 0, or $+1$. This product is then added to the 8 bit $\hat{b}_i(t)$ coefficient, computed and stored in the previous cycle, creating a new updated coefficient $\hat{b}_i(t+1)$.

Next, the $\hat{b}(t)$ coefficients are fed to the FIR filter to compute the artifact replica using the following FIR filter matrix multiplication:

$$\widehat{a}(t) = \left[\widehat{b_0}(t)\ \widehat{b_1}(t)\ \cdots\ \widehat{b_7}(t)\right] \begin{bmatrix} s(t) \\ s(t-1) \\ \vdots \\ s(t-7) \end{bmatrix}. \quad (6)$$

The computation above is implemented with eight multipliers and seven adders. Similar to the coefficient update described above, the multiplication and addition is performed in parallel for each tap, using a total of eight multipliers and seven adders. However, the single tap FIR filter multiplication is implemented with only eight AND gates, as shown in Fig. 10 on the left-hand side, since it uses a single-bit stimulation signal $s(t-i)$ as the second operand. Finally, the seven 8 bit ripple-carry adders sum the multiplier outputs to create $\hat{a}(t)$.

In summary, the full adaptive filter uses only 15 ripple-carry adders and no full multipliers. Because the filter runs at the very low ADC sampling frequency (4 kHz), the gates are minimum-sized to further reduce power consumption. Since most logic gates are active only when nonzero bits appear in the stimulation waveform, the average power consumption at conventional stimulation rates is below 11 nW and is almost negligible in comparison with the power consumption of the rest of the system.

B. CAR Circuit

CAR is implemented at the input of the second-stage amplification to relax the DR of the PGA. The circuit implementation is shown in Fig. 11. Preamplifier outputs from four neighboring channels are fed into a capacitive averaging network, one per channel. An advantage of this approach is that it is passive and does not add to the total power consumption. Moreover, the switchable capacitor array allows full reconfigurability in case undesirable channels should be disconnected. The additional capacitors increase the area of the recording channel by less than 3% if the number of references is kept at 4 (sufficiency of this number of references is shown in Section III). Furthermore, these capacitors can be placed above the active circuitry to further save area. The averaged output is fed into the input of the PGA with opposing polarity alongside the original preamplifier connection to effectively subtract the CAR signal. To maintain the proper functioning of the averaging when changing the number of reference channels, input and feedback capacitors are connected or disconnected to maintain constant gain. Also, the output impedance of the preamplifiers must be low enough, so that the changing preamplifier output load due to switching capacitors does not significantly affect the bandwidth.

C. Range-Adapting SAR ADC

To further lower the average power consumption of recording channels, we also propose a new adaptive ranging technique for SAR ADCs. Typical recording channels must have a high

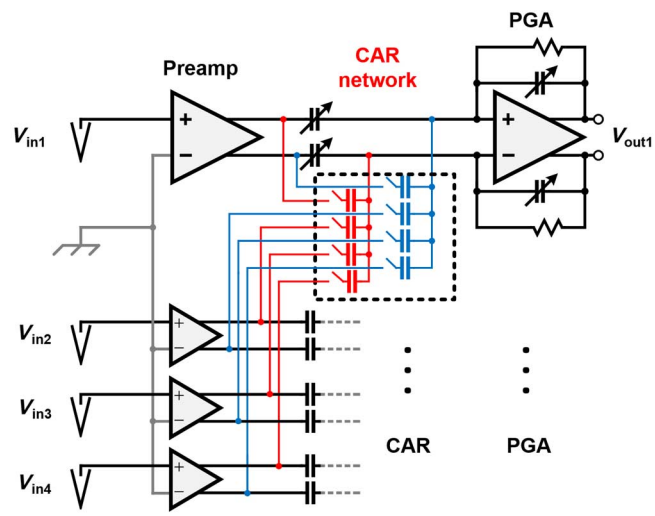

Fig. 11. CAR circuit implementation: the averaging CAR network is implemented for each channel in the group as shown for channel 1.

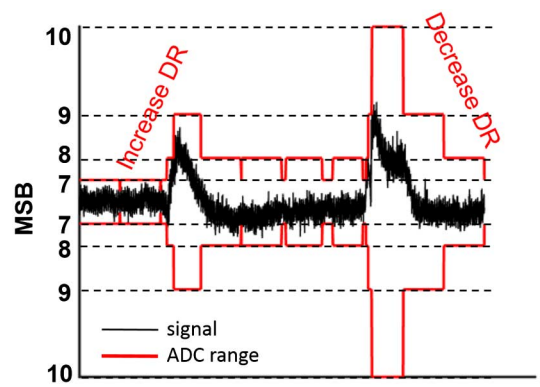

Fig. 12. Example of RA SAR ADC range (MSB) following the shape of a neural signal.

DR to process large signal amplitudes due to artifacts or periods of high neural activity. However, because high-amplitude activity in neural signals is relatively sparse, this high DR is often underutilized. By adapting the DR of the ADC to the signal, we can minimize the effective number of bits evaluated by the SAR algorithm and save power. Such system can be also applied to other types of sparse signals where the activity is low for majority of the time.

1) RA Algorithm: The RA algorithm adjusts the ADCs DR in two ways, as seen in Fig. 12. DR is automatically increased when a sample is detected to be out of range. DR can also be decreased between sampling cycles with an off-chip controller. Such a controller, e.g., can predict periods of low activity and reduce the range accordingly. In our simple implementation, a timer is set to decrease the DR by a single bit every 200 ms. Any algorithm which would adjust the range to fit the approximate envelope of the signal may be considered desirable; however, such algorithm should not alter the ADC's range at every sample since every range calculation requires extra logic power and it can dominate ADC power consumption.

2) RA SAR Switching Scheme: The RA algorithm is easily implemented in an SAR ADC with a modified capacitor DAC

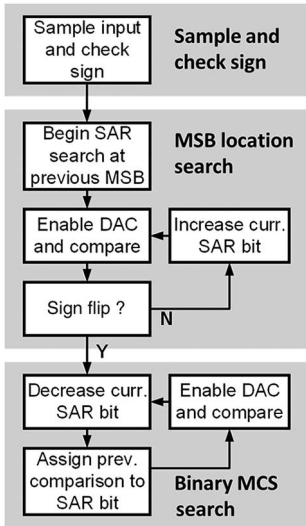

Fig. 13. RA SAR algorithm logic flowchart.

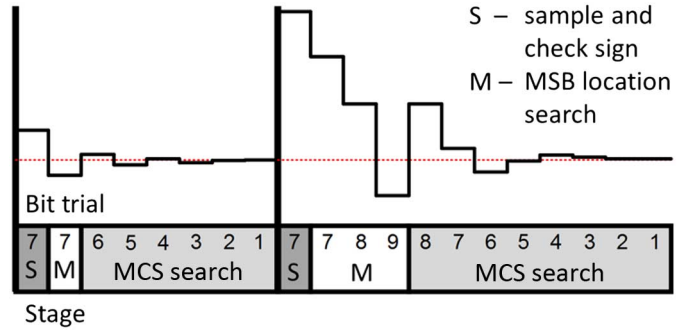

Fig. 14. Comparator input voltage during RA SAR A-to-D conversions for in-range and out-of-range samples, respectively. The conversion phases and bit cycles (bit) are also shown.

switching scheme by taking advantage of a specific application-adapted binary search, similar to [21]. Our scheme is divided into three phases outlined in Fig. 13, namely: 1) sample and sign check phase; 2) MSB range search; and 3) binary LSB search. Fig. 14 shows two conversion examples for an in-range and out-of-range samples by tracking the comparator input voltage. First, stage (1) finds the sign of the sampled voltage. The sign determines which direction the capacitive DAC changes the comparator input voltage for each SAR bit. Only in stage (2), does the algorithm search for the location of MSB. The search algorithm makes its initial guess based on the previous sample MSB location which is stored in between samples (bit 7 for both cases in the example). The DAC assigns the previously found sign bit to the current MSB location, and the comparator checks if the polarity has changed. If it does not change, the algorithm performs additional trials by increasing the MSB location, switching in the appropriate capacitors in the DAC, and observing the comparator result. When the comparator output finally changes, or when the maximum MSB is reached, the algorithm keeps the found MSB and moves on to stage (3). At this time, operating in stage (3), the ADC performs the traditional binary search from the current MSB to determine the remaining bits. In our scheme, the merged capacitor switching (MCS) scheme is used to minimize capacitor switching and power consumption [22].

The proposed RA SAR switching scheme has two key advantages. First, the range-checking phase prevents the ADC from losing any sample information, as the capacitor switching is performed without losing any charge on the top plate. Second, if the range-checking phase accepts the initial MSB location guess and does not have to perform additional trials, the ADC does not have to switch its comparator and DAC capacitors for all the bits in the ADC. This, on average, greatly reduces the power consumption of the ADC comparator and the capacitor DAC. As previously mentioned, [21] also presents an RA SAR ADC algorithm which, in contrast, begins the search at previous sample's LSB. Our proposed RA SAR algorithm is better suited for signals which exhibit low amplitudes but are not smooth and maintain high variance relative to maximum amplitude, as it is often the case in neural recordings.

3) ADC Power Consumption: Fig. 15 demonstrates the possible power reduction in an RA SAR ADC. Fig. 15(a) plots the minimum number of comparisons in the case of correct initial range guess for every code in the 10 bit ADC. Note that the minimum initial guess is kept at the sixth bit because neural signals rarely maintain lower amplitudes. The biggest power reduction when compared to a traditional MSC SAR ADC scheme is observed for small input signals. This is due to the reduced number of significant bits checked by the RA algorithm.

A code histogram of previously recorded neural data is overlaid to show that a great majority of the signal does fall in the power-saving range. In fact, simulations showed a 25% reduction in the average number of comparisons. In Fig. 15(b), the capacitive DAC switching energy per code is plotted for the MCS and RA switching schemes. Similar to the previous analysis, the greatest power savings are found in the middle codes. A 72% reduction in average DAC power consumption is observed.

4) ADC Circuit Implementation: The SAR ADC is implemented in differential fashion and employs bottom-plate input sampling to reduce parasitic error (Fig. 16). The ADC also uses an asynchronous architecture. At the beginning of every sample, the sampling clock triggers a self-timing delay loop that first clocks the comparator. When the comparator makes the decision, it activates the SAR logic and sends a signal through an inverter-based delay line to give time for settling of the capacitive DAC and to retrigger the comparator for the next bit conversion cycle.

The SAR logic executes the RA algorithm. The stages of the algorithm are controlled by the "direction select" flip-flop and logic. In stage (1), the comparator output Q is stored onto the "sign detect" flip-flop. After that, the "direction select" state tells the SAR logic to assign the sign bit to the current MSB location stored in a finite-state machine (range FSM). The range FSM is a 5 bit one-hot counter that saves the MSB location in between ADC samples and it increases or decreases its value as required by the RA algorithm. A mux, controlled by the range FSM and the "direction select" flip-flop, selects the

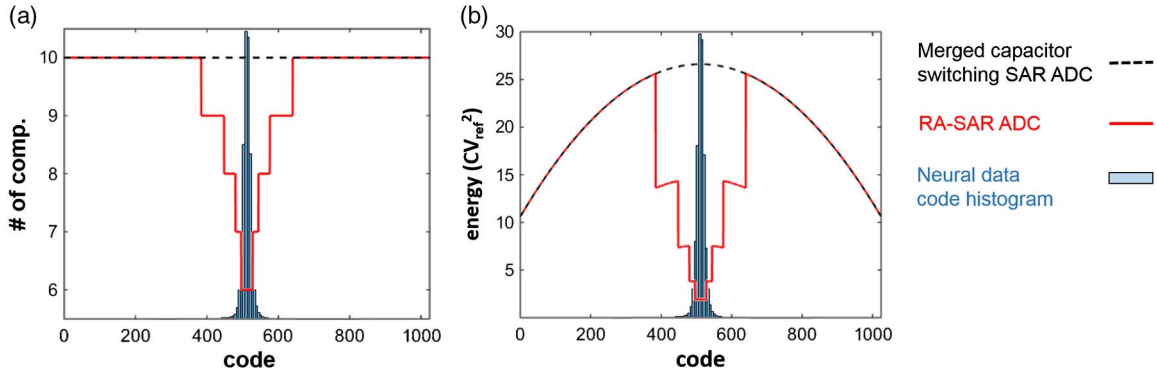

Fig. 15. (a) Simulated minimum number of comparisons and (b) capacitive DAC switching energy for 10 bit RA SAR ADC as compared to a MCS SAR ADC. Overlaid neural data code histogram shows most data falls within the most efficient code range.

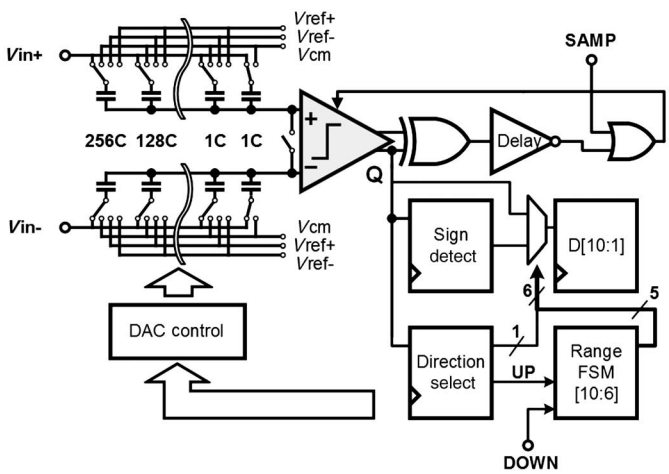

Fig. 16. RA SAR ADC architecture schematic.

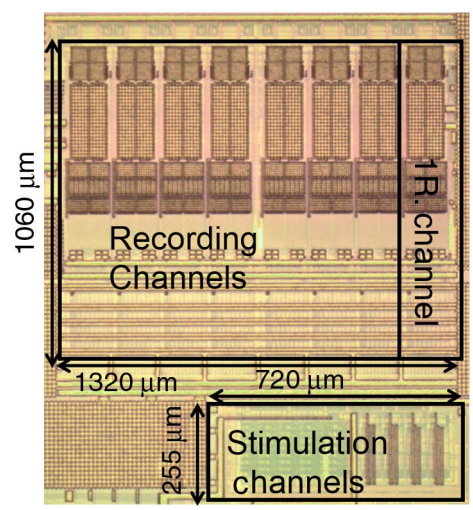

Fig. 17. Chip microphotograph.

SAR flip-flops that will be assigned the sign bit. As the logic detects the comparator polarity change at the end of stage (2), the "direction select" flip-flop changes its state and begins the MCS search of stage (3), finds the remaining bits, and stores them into the 10 bit SAR flip-flops. In between the samples, the range FSM can be externally triggered by the DOWN control input to decrease the initial MSB location to be used in the next sample conversion.

V. Measurements

A. System Performance

The prototype is fabricated in 0.18 µm CMOS. Fig. 17 shows the chip microphotograph. The total area of the recording circuit is $1.4\,\mathrm{mm}^2$ or $0.17\,\mathrm{mm}^2$ per channel, while the area of the stimulation circuit is $0.18\,\mathrm{mm}^2$. Fig. 18(a) shows the measured frequency response of the recording channel for four gain settings: 100, 200, 500, and 1000. Each of the gain settings maintains a bandwidth of 1 Hz to 2 kHz. Fig. 18(b) shows the input-referred noise of the full recording channel at the ADC output with a shorted input. The total measured input-referred noise is $3.05\,\mu\mathrm{V}_{\mathrm{rms}}$ between 1 Hz and 2 kHz. The measured power consumption per recording channel is $0.33\,\mu\mathrm{W}$.

B. CAR Circuit Measurements

An *in vitro* experiment with a 4 channel recording was conducted to test the functionality of the CAR circuit. The 4 channel waveforms were constructed from a synchronized 60 Hz noise signal. A prerecorded neural signal was then added to one of the channels. The top plot in Fig. 19 shows the channel with merged 60 Hz noise and the prerecorded signal. When CAR is switched ON for the 4 channel group, as shown in the bottom of Fig. 19, the averaged reference reduces the recorded 60 Hz power by −36 dB, effectively increasing the recording channel SNR by the same amount.

C. ADC Measurements

The average power consumption of the ADC is 89 nW when measured at 4 kS/s for a full-range sinusoid input. To test the functionality of the RA algorithm, the channel input signal amplitude is swept while monitoring the power consumption of the full ADC and DAC. Fig. 20 shows a significantly reduced DAC energy consumption for low-amplitude inputs (by more than a factor of 4). The shape of the plot is similar to the predicted DAC energy consumption from Fig. 15. This amounts

This article has been accepted for inclusion in a future issue of this journal. Content is final as presented, with the exception of pagination.

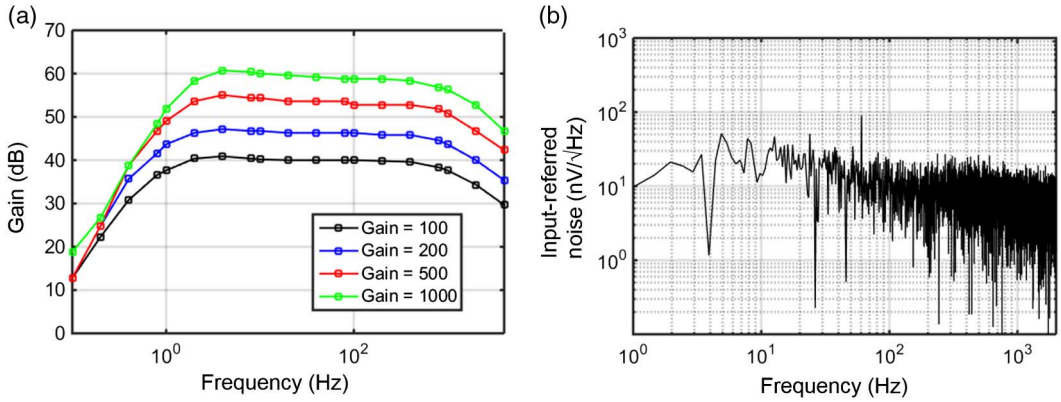

Fig. 18. (a) Recording channel frequency response for four gain settings measured at ADC output. (b) Input-referred noise of the full recording channel.

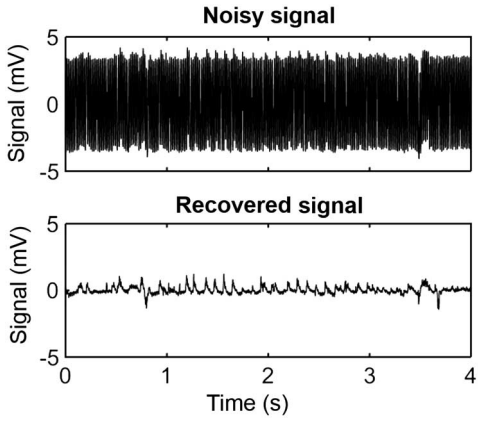

Fig. 19. Full channel recording before and after activating the CAR-4 circuit, showing the common-mode (60 Hz) noise reduction in *in vitro* recording.

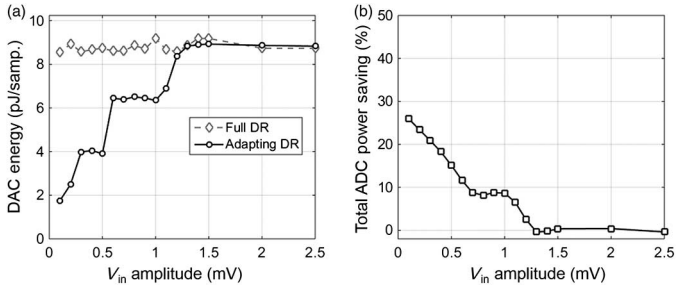

Fig. 20. ADC measurements showing (a) capacitive DAC energy consumption per sample for enabled/disabled adapting DR algorithm for amplitude-swept sinusoid input and (b) ADC total power savings.

to total ADC power consumption saving of more than 25% for low-amplitude inputs.

VI. *In vivo* Measurements

A series of *in vivo* tests were performed to test the system functionality in a real application. Recordings were taken during the stimulation of a rat hippocampus as the rat was under chemically induced seizures.[2] Seizures were induced

[2]The *in vivo* experiments were performed at the Netoff Epilepsy and Neuroengineering Laboratory, University of Minnesota under the approval from the Institutional Animal Care and Use Committee.

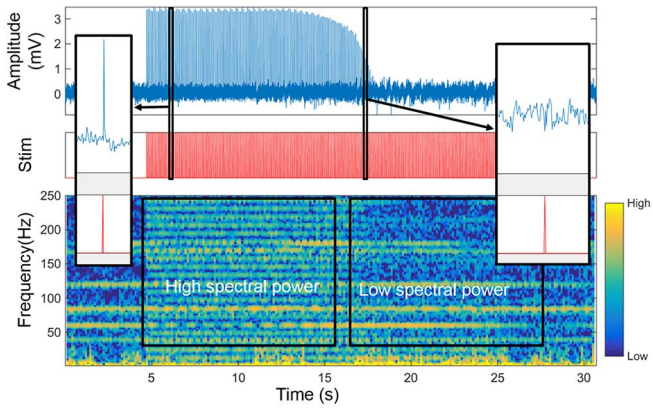

Fig. 21. *In vivo* experimental results showing stimulation artifact cancellation learning process for 12 Hz 600 μA biphasic stimulation. Top plot shows the raw time-domain plot of the recording output, middle plot shows the stimulation timing, and the bottom plot shows the recorded output spectrogram.

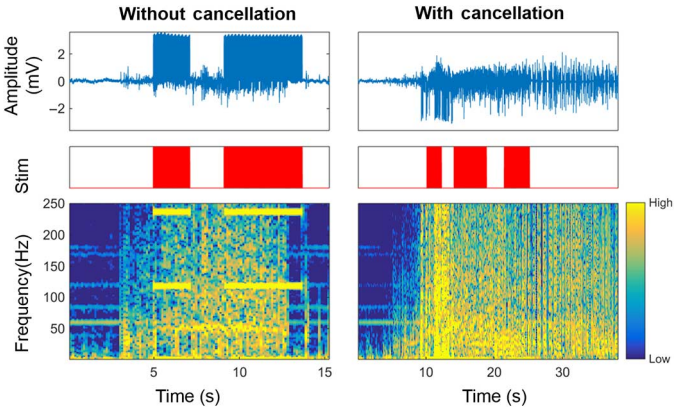

Fig. 22. Neural recordings of 120 Hz 600 μA biphasic stimulation during seizure activity (a) without activate artifact cancellation and (b) with active artifact cancellation.

following the injection of 4 aminopyradine unilaterally into the CA3 region of the hippocampus. The stimulation was then applied to the ventral hippocampal commissure (VHC) which bilaterally innervates the CA3 regions where the seizures are induced. A recording electrode was placed in the CA1 region of the hippocampus, close to the injection region. In this setup,

TABLE I
PERFORMANCE SUMMARY AND COMPARISON WITH OTHER RECENT WORKS

	[21]	[22]	[23]	This work
Technology	0.18 μm	0.13 μm	65 nm	0.18 μm
Area (per recording ch.) (mm^2)	~0.42	~0.625	0.025	0.17
Rec. power (μW/ch.)	7.35	4.2	2.3	0.33
BW (Hz)	~0.5–7k	0–320	1–0.5k	1–2k
IR noise (μV_{rms})	5.23	2	1.32	3.05
Stimulation artifact cancellation	No	No	No	Yes
CAR	No	No	No	Yes

the recording electrode has a clear recording of the seizure activity and the proximity of the recording and stimulation electrodes results in large stimulation artifacts that test the artifact removal algorithm.

In initial experiments, recordings were taken when stimulating the tissue as the artifact cancelling algorithm trained the filter weights. In Fig. 21, a 12 Hz 600 μA biphasic pulse stimulation train is applied and the response is recorded in time and time–frequency domain. As the stimulation begins in the fifth second, large artifacts clearly dominate the recorded waveform. Because the artifacts are being clipped at the start of stimulation, the reduction in artifacts is not apparent until the 15th second as the filter weights become large enough to successfully reduce the recorded artifacts. When the filter weights approach their steady-state values, the artifacts are reduced to the below-noise level. In a latter experiment, shown in Fig. 22, we stimulated the brain with and without cancellation as the seizures were episodically occurring. The noncancelled artifacts from the 120 Hz stimulation clearly dominate the seizure activity both in time and frequency domain. After the cancellation filter is turned ON, the artifacts disappear below the visible seizure signal, clearly showing the improved signal quality as the seizure signal becomes unobstructed by the artifact peaks. Across trials, artifacts are suppressed on average by at least 24 dB; however, this number could be even higher if not for the high biological noise masking the suppressed artifacts. Note that the full learning process needs to be performed only once after implantation, as the neural tissue response does not change significantly during chronic use of stimulation.[3]

VII. CONCLUSION

We present a new bidirectional neural interface circuit for closed-loop stimulation. The microsystem introduces novel architectural features to combat environmental noise such as stimulation artifacts and cross-channel common-mode noise, allowing overall proper closed-loop control. The circuit also includes a new RA SAR ADC to reduce power consumption. The system was fully characterized and verified *in vivo*. Table I summarizes and compares few key specifications with previously published works highlighting the state-of-the-art performance. Our work maintains a relatively low area and low noise in comparison with the published ECoG recording ICs in [23]–[25]. However, at lower power consumption, the system implements new functionality which enables the use in a wider variety of applications.

[3]When the filter coefficients reach a steady state, the adapting algorithm can be turned OFF to maintain their constant value. It can also be periodically turned ON to adapt coefficients to a slowly changing neural tissue response.

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