Chapter 16
Pipeline and SAR ADCs for Advanced Nodes

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16.1 Introduction

The energy efficiency of ADCs has improved by orders of magnitude over the past two decades. Even though process scaling degrades the analog characteristics of transistors, by exploiting, scaling the energy efficiency of recently reported ADCs is approaching fundamental limits [1]. These improvements have been achieved through innovative circuit ideas and through the evolution of ADC architectures. In particular, the SAR ADC architecture has benefitted tremendously from scaling. SAR ADCs are among the most efficient stand-alone converters and form excellent building blocks for more complex architectures including pipeline and highly interleaved ADCs. This chapter builds on material that first appears in [2–4].

Section 2 presents a stand-alone SAR ADC that achieves outstanding efficiency and also shrinks the area needed for a SAR ADC. This architecture uses a charge-injection cell-based DAC to avoid problems associated with residual settling in conventional SAR ADCs. Further, reuse of the charge-injection cells allows a very small die area. The small size and efficiency make the charge-injection cell SAR ADC an ideal building block for hybrid and interleaved ADCs.

We concentrate on pipeline ADCs for the remainder of the chapter. These combine sub-ADCs of moderate resolution with high-performance amplifiers to construct a high-resolution pipeline. In Sect. 3, we present a simple argument that in a two-stage pipeline the first stage should have higher resolution. However, this high-resolution first stage is difficult to achieve with flash-based sub-ADCs. The SAR-assisted pipeline ADC allows a high-resolution first stage that enables a very efficient two-stage pipeline.

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We focus on the amplifier part of the pipeline for the remainder of the chapter. In Sect. 4, we argue that a ring amplifier can supersede the workhorse-cascoded telescopic OTA in the switched-capacitor residue amplifier of a SAR-assisted pipeline ADC. In Sect. 5, we present a SAR-assisted pipeline ADC that uses a ring amplifier to achieve outstanding energy efficiency.

16.2 Charge-Injection Cell-Based DAC SAR ADC

SAR ADCs are not only highly effective by themselves but also form critical building blocks of pipeline ADCs and interleaved SAR ADC arrays. Interleaving of SAR ADCs delivers very high sampling speeds and good energy efficiency. However, interleaving of multiple SAR ADCs poses significant challenges due to the large area needed. A particular problem is that interleaving artifacts are exacerbated by die size [5]. Compact and efficient SAR ADCs facilitate highly interleaved ADCs and also serve as efficient building blocks for pipeline and $\Sigma\Delta$ ADCs. One approach to improving SAR ADC performance is the multiple-bit-per-cycle SAR ADC, but this has the disadvantage of significant extra complexity since extra quantizers and capacitor DACs are needed [6, 7]. Furthermore, multiple-bit-per-cycle SAR ADCs need increased die area. The charge-injection cell-based DAC SAR ADC (ciSAR ADC) [3] is a very compact SAR ADC architecture and achieves excellent energy efficiency.

Interrupted settling makes the ciSAR ADC faster, simpler, and more linear for high-speed operation. This is because the ciSAR architecture avoids the distortion suffered by conventional fast SAR ADCs due to insufficient DAC settling. Figure 16.1 illustrates how residual settling compromises the linearity of a conventional SAR ADC. Settling from a previous step continues into the present SAR step, leading to distortion in the conversion. As shown in the example, the residual background settling skews trip points downward. Redundancy in the SAR algorithm can alleviate this problem, but redundancy requires extra SAR steps and more complicated SAR logic. On the other hand, in ciSAR, thanks to interrupted settling, settling for any given SAR step stops *completely* at the end of that step. Returning to the example in Fig. 16.1, we see that with interrupted settling, there is no longer distortion of the trip points.

Modular *charge-injection cells* (CICs), as shown in Fig. 16.2, are the key to interrupted settling. Initially, the input signal is sampled onto two differential integration caps, C_{int+} and C_{int-}. During the SAR operation, the DAC+ and DAC- nodes of these capacitors are connected to the CIC cells and to a comparator. During the binary search, the CICs subtract fixed quanta of charge from the C_{int+} and C_{int-} capacitors. The binary search of the SAR ADC is based on the set-and-down method [8], since the CIC cells can only subtract charge. A unique advantage is that CIC cell can be reused for different SAR steps. Thanks to this reuse, the number of CIC cells can be far fewer than the number of levels in the SAR ADC. For example, in [3] only eight identical CICs are needed for a prototype 6-bit ADC.

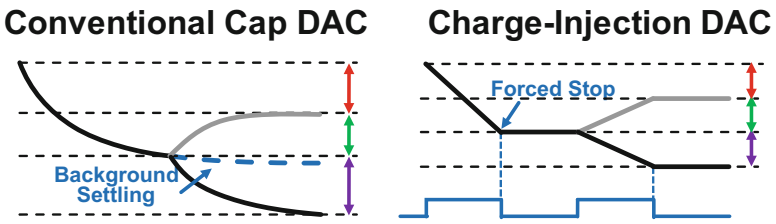

Fig. 16.1 Interrupted settling (*right*) avoids distortion due to limited bandwidth [3]

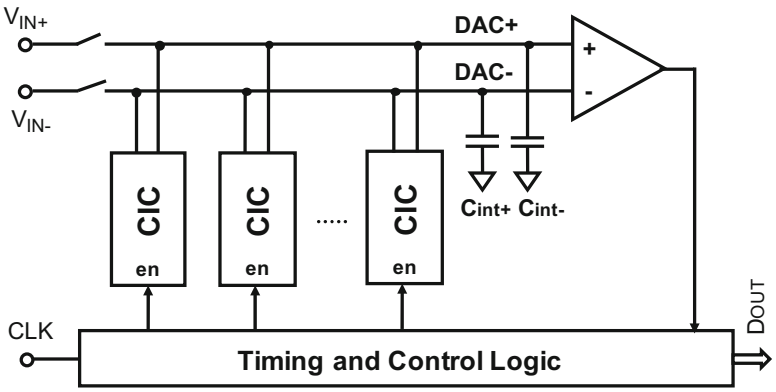

Fig. 16.2 ciSAR architecture with eight CIC cells for a 6-bit ADC [3]

The charge-injection DAC is fundamentally different to a conventional capacitor DAC because it is based on unidirectional transfer of charge instead of bi-directional charge sharing. When enabled, a CIC cell injects a fixed amount of charge onto the integration caps. Unidirectional switches isolate the charge source in the CIC cells from the DAC outputs with high output impedance for unidirectional charge transfer. A CIC only transfers charge from its charge reservoir to the C_{int+} and C_{int-} when it is enabled. Furthermore, the high output impedance makes the transferred charge independent of the voltage on the C_{int+} and C_{int-} capacitors. When a CIC cell is disabled, all charge transfer is halted and settling is interrupted. This interrupted settling eliminates any residual settling in subsequent cycles enabling better linearity, especially in high-speed operation, as shown in Fig. 16.1.

Figure 16.3 shows an implementation of the CIC cell. The CIC cell consists of a charge reservoir, switches, and control logic. The capacitance of M3, operating in triode region, along with parasitic capacitance at its drain node forms the charge reservoir. Initially, M4 resets the voltage in the charge reservoir to ground. During operation, switches M1 and M2 connect the reservoir to either DAC+ or DAC-. These switches operate in saturation for unidirectional transfer. Three logic gates (G1∼3) control these transistors based on signals from the SAR control logic and the comparator. Figure 16.3 also shows a timing diagram.

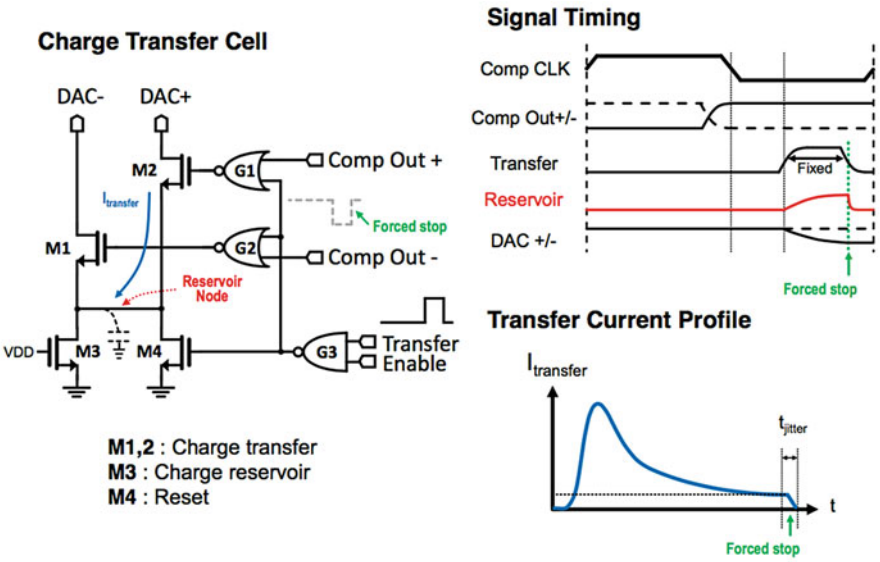

Fig. 16.3 Charge transfer cell, timing diagram, and transfer current profile [3]

The profile of the charge transfer (Fig. 16.3) also facilitates interrupted settling. At the beginning of the charge transfer cycle, one of the charge transfer switches (i.e., either M1 or M2) is strongly on. However, during the transfer, the voltage on the reservoir node rises reducing the gate-source voltage of the conducting NMOS switch (M1 or M2) and causing the current to fall. The current continues to fall until it drops to the level of the small bias current supplied by M3. This falling current profile greatly reduces the sensitivity to jitter in the timing control signal, since the current flow is always small when charge transfer is halted. As CIC cells are only active for a short duration, we use the remaining time to prepare for the next charge transfer.

A prototype ciSAR needs only eight CICs [3]. CIC cells in a ciSAR ADC are reused multiple times in a SAR conversion both to save area and improve linearity. During the MSB cycle, these eight CICs are used twice in two successive phases to deliver 16 units of charge. CIC cell reuse not only halves the DAC area but also halves the driver power for the control signals. CIC cell reuse also improves ADC linearity because the same cells are reused. CIC cell reuse in the prototype [3] only slows down the overall ADC sampling rate by only 15%.

16.3 Combining SAR and Pipeline

16.3.1 The Advantages of the Two-Stage Pipeline

A large first-stage resolution is very beneficial to the performance of a pipeline ADC [2, 9, 10]. A large first-stage resolution reduces power consumption and also attenuates noise and nonlinearity contributions of the subsequent stages to the overall ADC performance [9, 10]. The front-end stages dominate the ADC power consumption because these must be the most accurate and must dissipate more opamp power to achieve sufficiently accurate settling. The accuracy required from subsequent stages decreases exponentially, and so the power dissipated by them is relatively low.

On the other hand, a large first-stage resolution is difficult to implement with a flash-based sub-ADC because of the power and area needed for a large number of accurate comparators. A further challenge is that a high first-stage resolution demands an active front end to reduce aperture and sampling errors related to unavoidable differences in the sampling instants of the MDAC and sub-ADC (i.e., *clock skew* in Fig. 16.4). The SAR-assisted pipeline technique facilitates a large-stage sub-ADC resolution and removes the sampling mismatch between the MDAC and the sub-ADC.

We now consider a simple 3-bit MDAC stage (Fig. 16.4) to examine some of the benefits of a large first-stage resolution [2]. We model the opamp with a

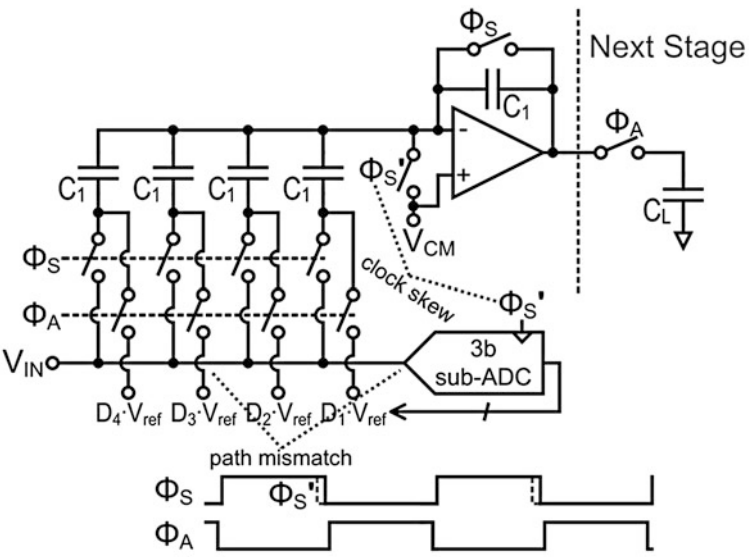

Fig. 16.4 Example of 3-bit SC MDAC [2]

transconductance G_m, and $C_{L,tot}$ is the total output load of the opamp. If we assume a first-order step response, then the output of the first-stage MDAC at the end of hold phase is

$$V_{\text{res}} = V_{\text{ideal}} + V_{\text{err}} \text{ and } V_{\text{err}} = (V_{\text{ideal}} - V_{\text{initial}})\, e^{-\frac{T\beta G_m}{C_{L,\text{tot}}}} \quad (1)$$

where T is the available time for settling and β is the feedback factor.

A simple argument shows the power advantages of an increased first-stage gain. The feedback factor β ($\approx 2^{1\text{-M}}$) is approximately halved with every 1-bit increase in resolution, M, of the first-stage MDAC. A 1-bit increase in the resolution of the first stage also indicates a 1-bit decrease in the required resolution of the subsequent stages. Therefore, the worsened feedback factor, β, is approximately offset by the increased tolerance for settling error, V_{err}. On the other hand, a 1-bit decrease in the required resolution of the subsequent stages also approximately halves the output load capacitance, $C_{L,tot}$. This reduction in $C_{L,tot}$ decreases the required opamp transconductance, G_m, which in turn directly translates into a reduction in the opamp power consumption. However, this power improvement with increasing first-stage MDAC resolution ceases when output self-parasitics of the opamp dominate $C_{L,tot}$.

The linearity of a pipeline ADC improves as the first-stage resolution increases [9]. This is because an increased first-stage resolution lowers nonlinearity due to capacitor mismatch. Furthermore, the large gain of a high-resolution stage decreases the nonlinearity and noise contributions of the subsequent stages.

16.3.2 The SAR-Assisted Pipeline

The SAR-assisted pipeline ADC architecture [2] is an energy-efficient hybrid architecture for moderately high-resolution analog-to-digital conversion. The SAR-assisted pipeline ADC couples two SAR ADCs with a residue amplifier (i.e., Gain), as shown in Fig. 16.5. The two SAR ADCs work as high-resolution sub-ADCs in each of the two pipeline stages. The SAR-assisted pipeline ADC has several advantages compared to both conventional pipeline ADCs with flash sub-ADCs and conventional SAR ADCs [2]. As discussed, we improve the linearity of the overall ADC and reduce opamp power consumption as we increase the resolution of the first-stage sub-ADC [9]. A SAR sub-ADC is very attractive because it uses less power than a flash sub-ADC. Another important benefit of a SAR-based first stage is that SAR sub-ADC and MDAC share the same sampling mechanism, thereby removing the need for a separate front-end sample and hold circuit.

For the same overall ADC resolution, the SAR-assisted pipeline architecture also has advantages compared to the conventional SAR architecture. In particular, for moderately high resolution (e.g., 12 bits), comparator noise performance is challenging in a conventional SAR ADC. On the other hand, the comparator

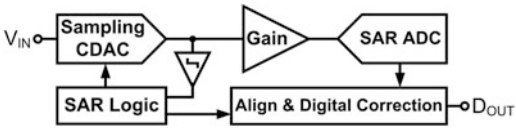

Fig. 16.5 Two-stage SAR-assisted pipeline [2, 4]

noise requirement is greatly relaxed in the SAR sub-ADCs of a comparable-resolution SAR-assisted pipeline ADC. A further advantage is that pipelining removes the speed bottleneck of the conventional SAR architecture. Finally, thanks to redundancy and digital correction, the SAR-assisted pipeline ADC tolerates settling errors of the first-stage SAR CDAC, provided these remain within the error correction range of the stage redundancy.

16.4 The Ring Amplifier

The cascoded telescopic OTA-based SC residue amplifier has been the workhorse of conventional pipeline and SAR-assisted pipeline ADCs [2, 11]. However, the conventional OTA structure consumes a lot of power and suffers from a limited output swing. This restricted output swing forces a stage gain smaller than suggested by the first-stage resolution and the redundancy of the pipeline. Because of this, SAR-assisted pipelines often need to reduce the reference voltages to the second stage [2], but this consumes extra power. Another alternative is to use an R-2R DAC in the second-stage SAR ADC [11]. Dynamic amplifiers are a lower-power alternative to OTAs in a pipeline ADC [12, 13, 15, 16]. Through time-domain integration, a dynamic amplifier offers low power amplification of the residue. An advantage is that this integration filters noise [14]; however, the inaccurate open-loop gain with dynamic amplification requires gain calibration in the pipeline. Not only does calibration increase both the complexity of design and test cost, it also reduces robustness to changes in process, supply voltage, and temperature (PVT) [13].

The ring amplifier [17, 18] is an energy-efficient alternative to an OTA that intrinsically has a high output swing. The high gain of the ring amplifier allows closed-loop operation without the need for calibration of gain. [4] introduced a fully differential ring amplifier enabling a fully differential switched-capacitor stage. Slew-based charging makes ring amplifiers energy efficient. Recent ring amplifiers are robust to PVT variation [4, 18] because they do not need external biasing.

The original ring amplifier [17], Fig. 16.6a, is a three-stage inverter-based amplifier with an offset-canceled first stage. The ring amplifier is stabilized by last stage moving to the subthreshold region as the ring amplifier virtual ground (i.e., V_{IN} in Fig. 16.6) approaches the desired common-mode voltage. This is done with the help of split second-stage inverter amplifiers with separate floating input offset voltages. During auto-zero, the floating input offsets of the second-stage inverters are applied to capacitors C_2 and C_3 via an external bias voltage, V_{OS}.

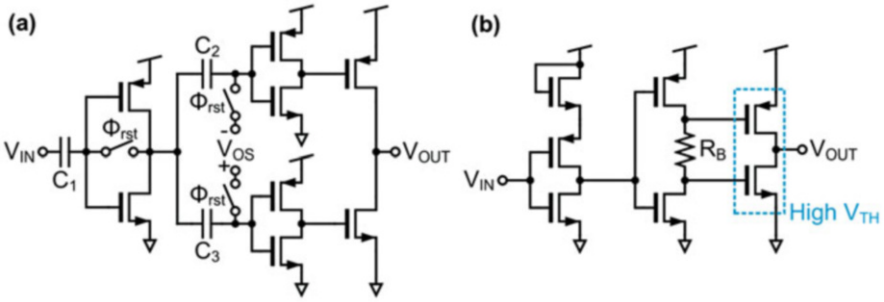

Fig. 16.6 (**a**) Original ring amplifier [17] and (**b**) the self-biased ring amplifier [18]

Operating the third stage in subthreshold results in a high output resistance, thereby forming a dominant pole at the output and stabilizing the amplifier. Ring amplifiers [4, 17, 18] have several intrinsic advantages compared to OTAs. First, even with a low supply voltage, a ring amplifier easily produces high gain from its three cascaded gain stages. Second, as mentioned earlier, slew-based charging is very energy efficient. Third, because the last stage is a simple inverter, ultimately operating in subthreshold, ring amplifiers can handle a near rail-to-rail output signal swing.

The self-biased single-ended ring amplifier introduced in [18] and shown in Fig. 16.6b is more robust to PVT changes and uses less power than the original ring amplifier circuit. The improved robustness and the removal of external biases make this ring amplifier more practical. One of the innovations in [18] is the use of high threshold voltage NMOS and PMOS transistors in the last stage, which extends the stable range since high threshold voltage FETs have an order-of-magnitude higher output resistance for a given gate-source voltage. Another technique that helps stabilize the design is the addition of resistor, R_B, between the gates of third-stage NMOS and PMOS transistors, as shown in Fig. 16.6b. The voltage drop caused by the second-stage inverter current flowing through R_B dynamically applies different voltages to the gates of the last inverter stage, as V_{IN} approaches the desired common-mode voltage. On the other hand, the gates of the NMOS and PMOS transistors of the last stage are still driven rail to rail when V_{IN} is away from the common-mode voltage, ensuring a high slew rate. An advantage compared to the ring amplifier in [17] is that the combined three stages are auto-zeroed for improved PVT tolerance.

The ring amplifiers in [17, 18] are single-ended circuits and therefore inherit the drawbacks of single-ended structures. The well-known disadvantages of single-ended circuits include limited common-mode and supply rejection. Furthermore, single-ended circuits do not reject even order harmonics as differential circuits do. As shown in Fig. 16.7, a pseudo-differential structure along with a common-mode feedback (CMFB) circuit [17, 18] to some extent alleviates these problems. The switched-capacitor CMFB in Fig. 16.7 consists of the common-mode sensing

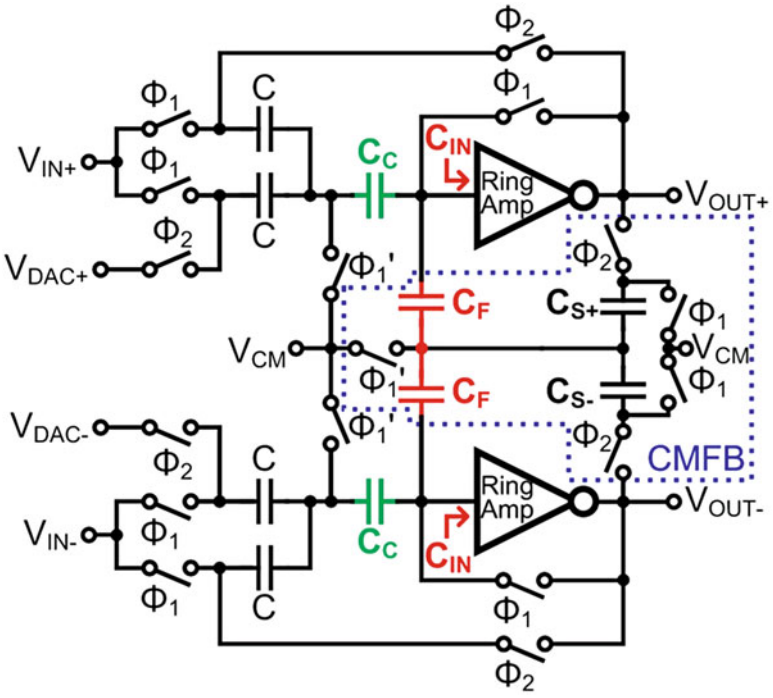

Fig. 16.7 Pseudo-differential MDAC gain stage with two ring amplifiers in [18]

capacitors C_{S+} and C_{S-} and feedback capacitors, C_F. V_{CM} is the common-mode voltage reference. A limitation is that this pseudo-differential CMFB reduces the effective gain of the ring amplifier because C_F forms a capacitive divider at the input of the ring amplifier. The effective gain is reduced from the nominal ring amplifier gain, A_V to $A_V \bullet C_C/(C_C + C_F + C_{IN})$, where C_C is the auto-zero offset storage capacitor and C_{IN} is the input parasitic capacitance of the ring amplifier.

As shown in Fig. 16.8, [4] introduces a fully differential ring amplifier that avoids the problems of the single-ended ring amplifier structure. In the fully differential ring amplifier, a single differential pair replaces the first stages of a pair of single-ended ring amplifiers [18]. Reuse of current by the NMOS and PMOS differential pairs increases the transconductance, thereby reducing the dominant thermal noise of the ring amplifier. To further save power, when not needed, the first stage is powered down via an enable signal Φ_{EN}.

Effective biasing and CMFB are important for reliable operation of the ring amplifier. Biasing and CMFB are shown in Fig. 16.8. The auto-zero forces the ring amplifier input and output voltages to be close to values that lead to the highest amplifier gain. There are separate CMFB loops to set the common mode of the first stage and the common mode of the overall ring amplifier. During the auto-zero phase, a CMFB loop, consisting of PMOS devices M4, M5, and M6

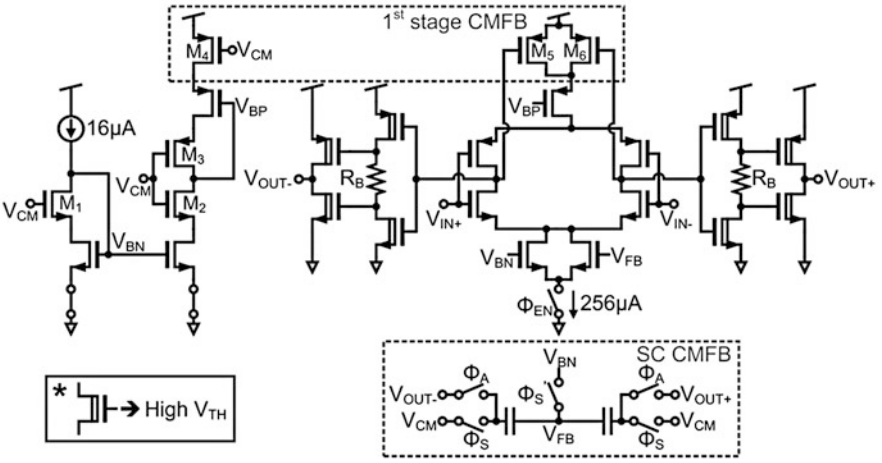

Fig. 16.8 Fully differential ring amplifier, along with bias and CMFB [4]

operating in triode [19], coarsely regulates the output common mode of the first stage. A separate switched-capacitor CMFB circuit forces the output common mode of the entire ring amplifier to V_{CM} during the amplification phase.

The second and third stages of the ring amplifier are based on inverters. Similar to the single-ended self-biased ring amplifier [18], resistors, R_B, apply (Fig. 16.8) dynamically offset voltages to the PMOS and NMOS gates of the third stage. Furthermore, high-threshold voltage devices in the second stage increase gain. This is needed because dynamic biasing can cause the second-stage transistors to operate in triode region. Triode operation greatly reduces both the second-stage gain and also the gain of the entire ring amplifier. As with the third stage, the use of high threshold voltage transistors extends the output voltage range for which the second-stage transistors are operating in saturation. The simulated small-signal gain for a 65 nm CMOS prototype ring amplifier is greater than 80 dB for an output swing range from 0.1 V to 1.1 V and a 1.2 V supply.

16.5 SAR-Assisted Pipeline ADC with Ring Amplifier

A prototype 50MS/s 13-bit ring amplifier-based SAR-assisted pipeline ADC [4], shown in Fig. 16.9, employs a 6-bit first-stage SAR ADC and an 8-bit second-stage SAR sub-ADC. Different to conventional SAR-assisted pipeline ADCs [2, 11–16], an advantage is that the wide output range of the differential ring amplifier permits a full 32× gain residue stage. The wide output swing relaxes the noise constraints on the second-stage sub-ADC and therefore saves power. The overall ADC accepts a 2.4 $V_{pk\text{-}pk\ diff}$ (i.e., rail to rail) input. One bit of stage redundancy allows the

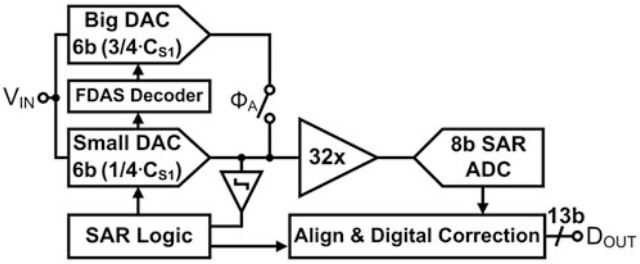

Fig. 16.9 50MS/s 13-bit SAR-assisted pipeline ADC with ring amplifier [4]

pipeline to tolerate first-stage sub-ADC errors. The output range of the residue is 0.3–0.9 V for ideal first-stage CDAC and comparator. The additional output range of the amplifier facilitates the 1-bit redundancy.

To reduce the switching energy of the first stage, SAR CDAC is split into two separate capacitor DAC arrays, *Big DAC* and *Small DAC*, as shown in Fig. 16.9. Splitting the CDAC into two separate capacitor arrays also reduces the INL and DNL errors due to the CDAC capacitor mismatch. The total differential sampling capacitance of the first-stage CDAC is 4 pF to satisfy the 13-bit kT/C noise requirement. Taking advantage of the fact that the 6-bit first-stage SAR sub-ADC needs only to meet 6-bit kT/C noise performance, *Small DAC*, which is part of the first-stage SAR ADC, uses only a quarter of the sampling capacitance, to reduce the SAR DAC power consumption. Merged capacitor switching (MCS) [20] further reduces the energy consumption of the SAR DAC. Asynchronous SAR operation [21] eliminates the need for a high-frequency ADC clock and reduces errors due to comparator metastability.

Both *Big DAC* and *Small DAC* sample the same input signal. *Big DAC* contains the remaining three quarters of the sampling capacitance and is only needed during residue generation. Based on the decision of the SAR, energy-efficient switching of *Big DAC* is achieved with the floated detect-and-skip (FDAS) CDAC switching technique, derived from [22]. Once the first-stage SAR conversion is complete, the residues of the Big and Small DACs are merged together and passed to the 32× residue amplifier.

Figure 16.10 shows a simplified single-ended depiction of the residue gain structure – the actual implementation is fully differential. Φ_A controls the amplification phase, and Φ_S and $\Phi_{S'}$ are sampling/auto-zero phase control signals. Auto-zeroing ensures that the output swing of the ring amplifier is fully utilized. A relatively large (4 pF) offset storage capacitor, C_{AZ}, minimizes folding of the auto-zero noise [23]. However, the fact that the sampled voltage on C_{AZ} stays constant means that the large C_{AZ} capacitance does not have a detrimental effect on power consumption. Furthermore, this large C_{AZ} capacitance has the advantage of stabilizing the ring amplifier during the auto-zero. This is because C_{AZ} presents a large load to the ring amplifier during auto-zero, thereby reducing both the dominant pole frequency and the slew rate.

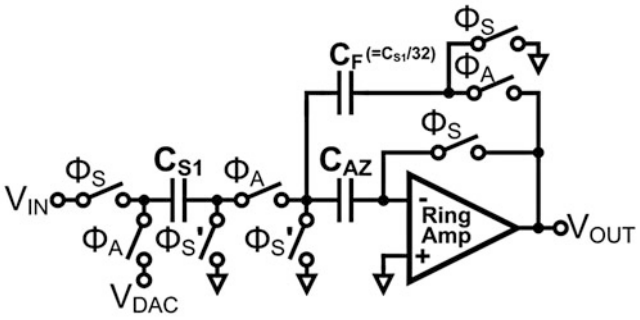

Fig. 16.10 Simplified single-ended depiction of residue gain stage structure [4]

1st stage	Tracking	Conversion	Residue transfer
Residue Amplifier	Auto-zero	Off	Residue amplification
2nd stage	Conversion	Reset	Tracking

Fig. 16.11 Simplified timing for SAR-assisted pipeline with ring amplifier [4]

Figure 16.11 shows a simplified timing diagram for the entire SAR-assisted pipeline ADC. To save power, the ring amplifier is powered down during the operation of the first-stage SAR ADC. Amplification begins after the completion of the first-stage SAR ADC conversion – this maximizes the time for residue amplification. In the prototype, an 8-bit second-stage SAR sub-ADC digitizes the amplified residue. The second stage, like the first-stage sub-ADC, uses MCS, bottom-plate input sampling, and asynchronous SAR logic. The second-stage 8-bit CDAC is reset to V_{CM} after the sub-ADC is finished so that residue amplification always starts from V_{CM}. This reset improves efficiency by halving the maximum slew rate required from the ring amplifier [18].

16.6 Conclusions

The last decade has seen a near three order-of-magnitude improvement in the energy efficiency of ADCs. Much of this can be attributed to the scaling-friendly nature of the SAR architecture. Furthermore, the SAR-assisted pipeline architecture enables SAR ADCs to dramatically improve the energy efficiency of moderately high-resolution pipeline ADCs. At the same time, the ring amplifier avoids the problems associated with OTAs in advanced CMOS nodes.

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