Low Power Wireless Sensor Networks for Infrastructure Monitoring

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ABSTRACT

Sensors with long lifetimes are ideal for infrastructure monitoring. Miniaturized sensor systems are only capable of storing small amounts of energy. Prior work has increased sensor lifetime through the reduction of supply voltage , necessitating voltage conversion from storage elements such as batteries. Sensor lifetime can be further extended by harvesting from solar, vibrational, or thermal energy. Since harvested energy is sporadic, it must be detected and stored. Harvesting sources do not provide voltage levels suitable for secondary power sources, necessitating DC-DC up-conversion. We demonstrate a 8.75mm^3 sensor system with a near-threshold ARM microcontroller, custom 3.3fW/bit SRAM, two 1mm^2 solar cells, a thin-film Li-ion battery, and integrated power management unit. The 7.7µW system enters a 550pW data-retentive sleep state between measurements and harvests solar energy to enable energy autonomy. Our receiver and transmitter architectures benefit from a design strategy that employs mixed signal and digital circuit schemes that perform well in advanced CMOS integrated circuit technologies. A prototype transmitter implemented in 0.13µm CMOS satisfies the requirements for Zigbee, but consumes far less power consumption than state-of-the-art commercial devices.

Keywords: Sensor neworks, low power, PLL, Zigbee.

1. INTRODUCTION

Infrastructure monitoring plays an important role in preventing hazards from building and bridge degradation. Large scale, dynamically changing, and robust sensor networks can be deployed in inhospitable physical environments such as remote geographic regions or toxic urban locations [1]. Monitoring bridges, for example, necessitates continuous monitoring of the concrete material to avoid degradation [2]. This way, the sensors predict bridge failure, and countermeasures can be taken to prevent costly disasters.

Figure 1, shows the main components of such a monitoring system. There are three factors that make a monitoring system viable: small size, low power, and reliable connection to the base station and/or other monitoring nodes.

Size obviously matters because we would like to avoid interfering with the normal operation of the infrastructure. Miniaturization reduces cost, making it possible to add multiple sensor nodes to gather data from different parts of an infrastructure.

Because sensors store limited amounts of energy and are often deployed in locations without access to dedicated power sources, the importance of two issues becomes more pronounced. First, intelligent ways to leverage the available solar [3], thermal [4], vibrational [5] energy to power the nodes are needed. Second, the system power must be reduced to prolong system lifetime. The data extracted from the sensor nodes is not useful unless sent to a base station for further processing. This necessitates wireless communication, and adequate energy in the microsystem's budget for data transmission. Adopting well-established wireless standards can make the network expandable and compatible with existing solutions [6].

In this paper, we investigate the components of an infrastructure monitoring sensor node. We propose methods to achieve the above-mentioned goals in terms of power, volume, and the data communication in a sensor node. We propose a highly-integrated electronic system which includes a commercial processor designed in the near-threshold regime [7]. The sensor system has a power management unit, memory, and solar cells to achieve an unprecedented level of integration. On the communication side, we propose a highly integrated transceiver based on the commercial 802.15.4 (Zigbee) standard that achieves low-power operation through the use of a novel fractional-N PLL and efficient power

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amplifier [8]. We demonstrate the viability of our approach by measurements from our latest chips, manufactured in state-of-the-art CMOS process.

Section 2 reviews the energy source for a monitoring system. Section 3 describes the memory architecture as the block that can dominate the system power in low-duty cycle applications. Section 4 describes the low-power microprocessor. In section 5, pressure and temperature sensors are explained. In section 6, we describe the wireless link. Finally, section 7 draws the conclusion of the paper.

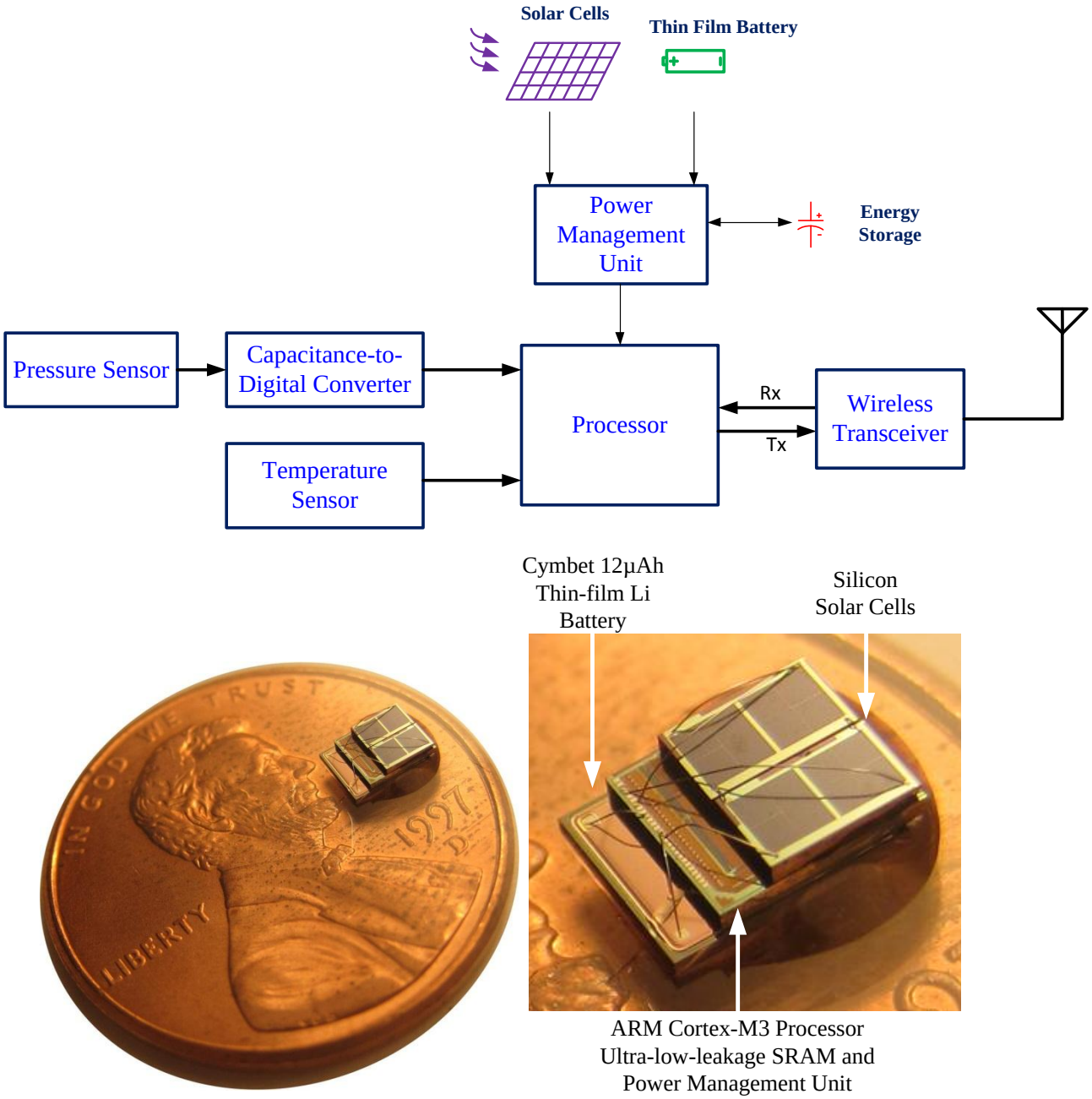

Figure 1. The 3-layer infrastructure monitoring sensor node contains a battery, electronics, and solar cells.

2. POWER MANAGEMENT

2.1 Power Sources

Different power sources such as RF [9], solar[10,11], and vibrational[12] power have been successfully used in sensor nodes. While batteries provide a reliable voltage to power the system, they suffer from limited capacity and in the long run must be recharged by other energy sources. Other sources are usually sporadic and generate voltages that are too low to power the system. Figure 2 shows the I-V curve of our CMOS solar cell. As can be seen from the graph, maximum power delivery occurs at around 500mV which is far below the 3.6V rechargeable Li-film battery voltage. Our system includes a compact thin-film battery to store energy. The battery is charged using the solar cells in standby. In active mode, this energy is used to perform measurement, DSP, and wireless transmission. As shown in the next section, the power management design enables us to tackle the limitations of the solar cell. Note that as shown in Figure 1, it is very important for the system to have temporary energy storage to accommodate components such as the radio which require a supply current that exceeds the battery's peak current limit.

2.2 The Switch-Capacitor up/down-converter

In order to leverage the solar energy the low voltage from the solar diodes need to be up-converted to the battery voltage (3.6V). The boost converters that are commonly used for voltage conversion need an external inductor and are not suitable for highly-integrated millimeter-scale sensor nodes [13,14]. Switched capacitor networks provide an alternative solution with no external components, while maintaining the same efficiency levels [15]. The schematic of our proposed switched capacitor network (SCN) is shown in Figure 3. Special care is taken in designing the clock since it dominates the converter power. It can also convert from 3.6 to 0.9V to supply the system in active and stand-by mode. Also, the system clock frequency is lowered in standby to save power. The SCN uses a novel on-demand clocking method that adaptively adjusts clock frequency with load current to achieve lower power (Figure 4).

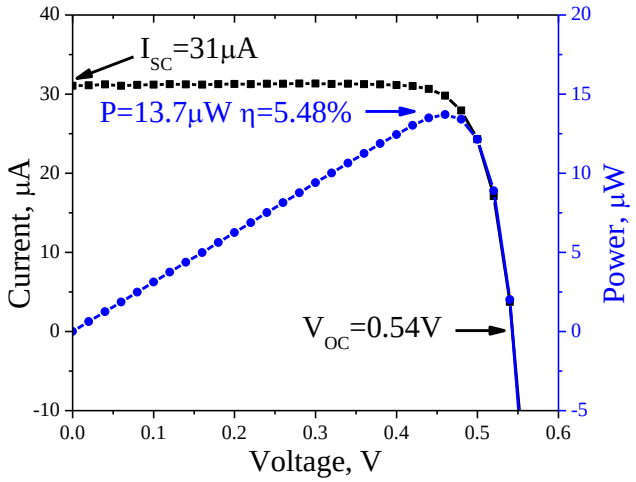

Figure 2. The CMOS solar cell I-V curve in our system can deliver up to 13.7μW to the rest of the system [7].

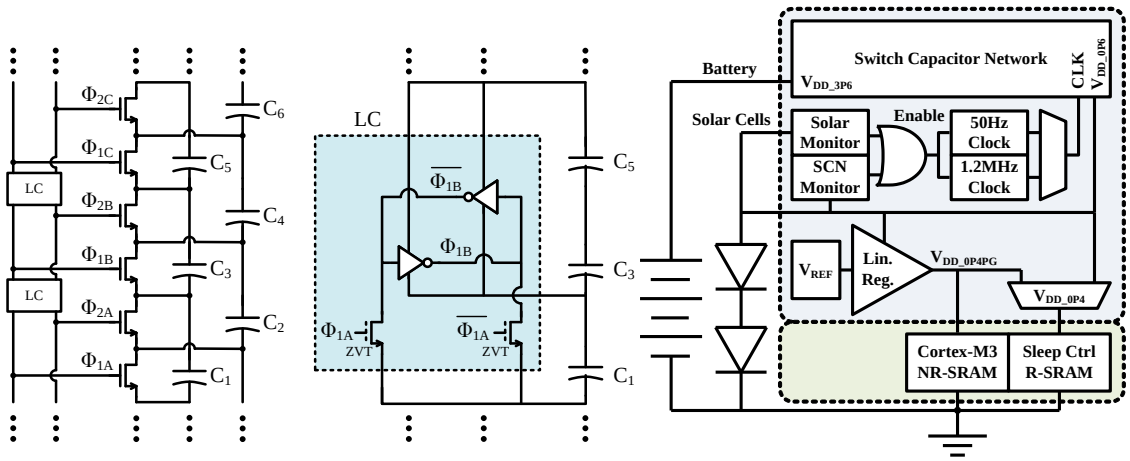

Figure 3. Our low-power switched capacitor network up-converts the 0.5V voltage of the solar cells to charge up the 3.6V Li-film battery[7].

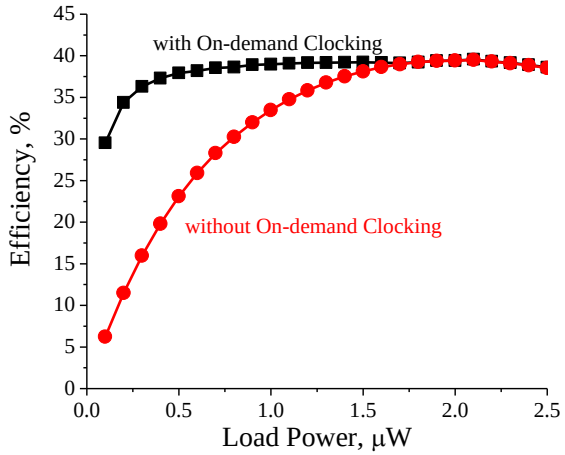

Figure 4. On-demand clocking improves the power management unit efficiency by 20% at low load levels [7].

3. MEMORY

In low-duty-cycle applications such as infrastructure monitoring, data retention in standby consumes the largest component of the system energy and should be minimized. Non-volatile memories such as Flash and Fe-RAM can store data for long periods with no standby power. However these circuits require additional processing steps that add to cost, and require high-power writes using complicated circuits [16,17]. Our system uses custom-designed Static Random Access Memory realized in standard CMOS process, and aggressively voltage scaling using sub threshold techniques to achieve low-power operation. The 5kB memory, is divided into a 3kB retentive SRAM (R-SRAM) and a 2kB non-retentive SRAM (NR-SRAM).

3.1 Retentive memory

The role of the R- SRAM is to store measurement data and processor program in sleep mode. In a typical monitoring scenario, the R-SRAM consumes over 80 percent of the total system energy in stand-by mode. This adds to the significance of lowering the SRAM power. Our R-SRAM uses a 10T configuration with a 6T writing and retention portion and a 4T read buffer (Fig.5). The use of IO devices in addition to length biasing greatly reduces leakage power. The bit-lines float in standby mode to reduce leakage by over 18% (Fig 5). These techniques bring the bitcell leakage down to 3.3fW.

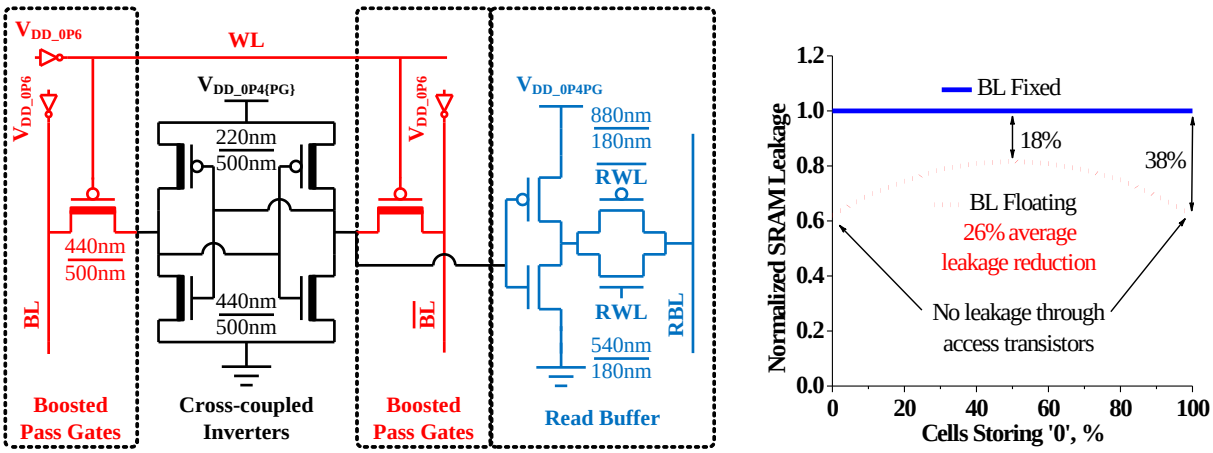

Figure 5. The low-power R-SRAM. The R-SRAM uses boosted pass gates and read buffers to achieve low power operation. Floating pass-gates reduces SRAM leakage by over 18% [7].

3.2 Non-retentive memory

The NR-SRAM is used for temporary storage during code execution. In order to eliminate its leakage from the system stand-by power, it is power-gated. It also uses a higher performance design to avoid creating a bottleneck in active mode. The cross-coupled inverters and pass gates use logic transistors for increased performance, since their standby mode leakage is controlled with power gating.

4. DIGITAL MICROPROCESSOR

The microsystem includes a commercial ARM Cortex-M3 processor to perform digital signal processing (DSP), data compression, and data logging on the sensor outputs. Numerous techniques were applied to reduce active and stand-by power while maintaining adequate noise margin. Based on statistical Monte Carlo analysis, complicated flip-flops and multi-input standard cells with large drive strength are removed to ensure functionality.

Microprocessor energy consumption is highly dependent on the choice of the supply voltage, V_{DD}. While lowering V_{DD} yields quadratic reductions in active power, it also results in longer execution times and higher leakage energy per computation. As a result, an optimal supply voltage exists at which energy per operation is minimized [18,19,20]. Our processor and SRAM operate at the minimal energy operating point where the sum of dynamic and leakage energy is minimized to 28pJ per cycle.

In standby mode, the microprocessor is power-gated to avoid excessive standby power. In order to further reduce the standby leakage, high V_{th} IO headers were used. In standby mode, the processor is power gated to avoid excessive leakage. As a result, the system standby power is dominated by the SRAM and not the processor.

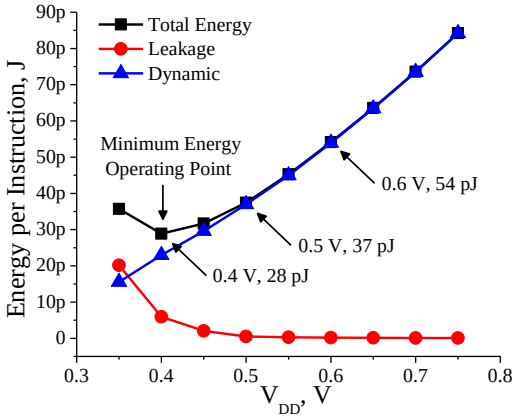

Figure 6. The choice of supply voltage drastically affects the microprocessor energy consumption. Our microprocessor was designed to operate at the minimum energy operation point [7].

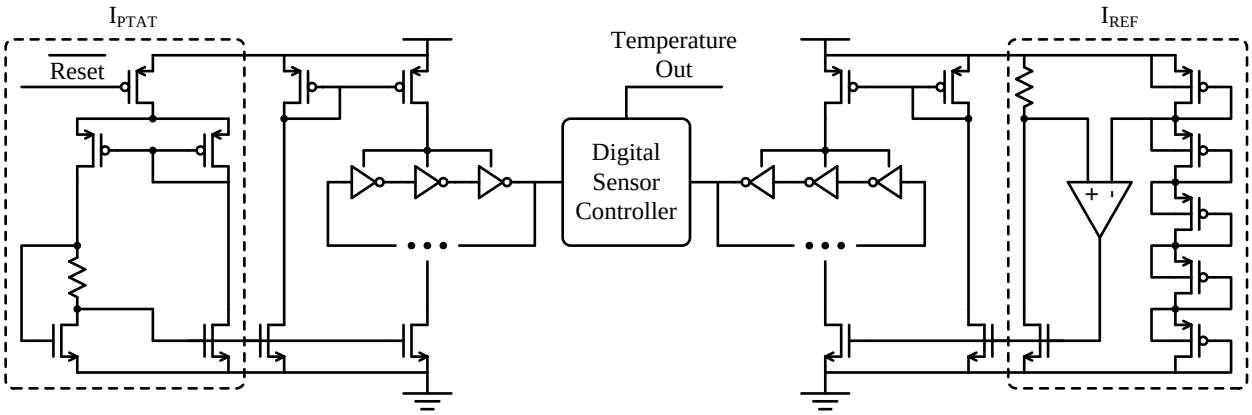

Figure 7. The temperature sensor uses a PTAT current source to supply the current and set the frequency of a ring-oscillator, which is converted to a digital number [22].

5. SENSORS

5.1 Temperature Sensor

The conventional technique in designing CMOS temperature sensors is to use a parasitic bipolar transistor [21]. While this method yields high accuracy, it consumes microwatts and therefore is above the power budget of the infrastructure monitoring sensor nodes. Our system uses a counter-based CMOS temperature sensor (Figure 7) that is more suited for low-power operation in modern technology nodes [22]. It consists of two ring oscillators. The first ring oscillator is controlled by a reference temperature-independent current source while the second one is controlled by a proportional to absolute temperature (PTAT) current. By subtracting the two counts an output that is independent of global variations is achieved. The sensor's compact design occupies only 0.05mm^2 and consumes 200-310nW while active. It achieves -1.6ºC/+3ºC accuracy over a temperature range of 0-100 ºC.

5.2 Pressure Sensor

Capacitance to digital converters (CDC) apply an excitation force to a pressure-sensitive capacitance to generate a voltage or current proportional to the sensed pressure. High pressure sensing accuracy can be achieved by replacing the resistor in an integrating amplifier with a switched version of the measured capacitor [23]. Successive approximation techniques have also been proposed as an alternative method for digitizing the capacitance [24]. However, none of the reported power levels are within the power budget of our system. We propose a 5.6µW ΣΔ CDC [11] that consumes 7.0 µW of active and 173pW of standby power (Figure 8). A sensitivity of less than 0.5mmHg makes it a suitable candidate for measuring strain on infrastructure as well as fluid pressure when the device is immersed in water. Various techniques

were used to bring down the CDC power. The 50 kHz clock generator operates at a lower 0.9V voltage which significantly reduces power consumption. This voltage is later up-converted to 3.6V to drive the switched capacitor resistors and comparator. To reduce leakage, the all CDC transistors are high-threshold, thick-oxide IO devices with a leakage power consumption that is three orders of magnitude lower than that of logic devices.

6. WIRLESS LINK

The monitoring sensors in an infrastructure monitoring network have to communicate with each other, and more importantly to the base station. While WLAN, Bluetooth, and other high-speed communication standards offer high data rate, their high power requirement and high external component count make them unattractive for sensor applications. The Zigbee standard, however, offers a sufficient bitrate and most Zigbee transceivers require only an external reference crystal oscillator and no external filters. The relaxed spectrum mask of Zigbee makes it fully realizable in CMOS, enabling integration with other system components, resulting in a compact and low cost microsystem.

We propose a fully integrated Zigbee transmitter (Figure 9) that uses a digital ΣΔ fractional-N PLL along with a self-calibrated two-point modulation scheme [8]. The transmitter delivers -2dBm of output power at a modulation rate of 2Mb/s. It consumes 17mW from a 1.2V supply and occupies an active area of 0.6mm^2.

The transmitter is comprised of a mostly-digital fractional-N PLL modulator and a two-stage power amplifier. A digital phase detector (PD) compares a reference clock and the divided-down output of a voltage-controlled oscillator. A digital integrator averages the PD output. The digital output of the filter is converted to an analog signal by a resistor string ΣΔ DAC. This analog signal drives the control input of the VCO.

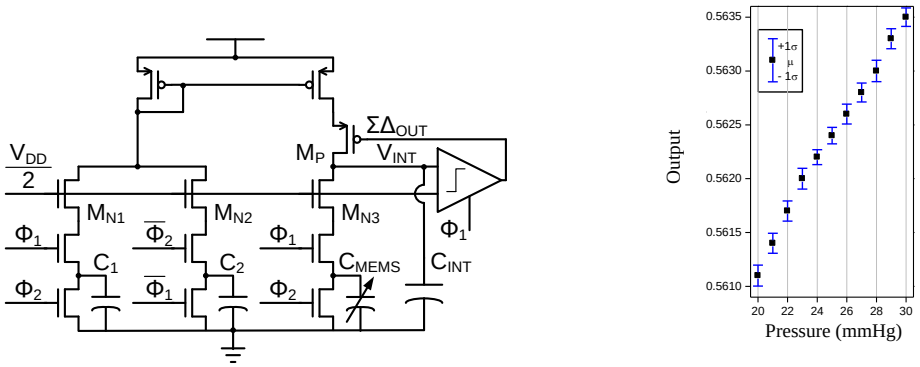

Figure 8. The capacitance to digital converter uses a delta-sigma modulator to generate a digital count proportional to the measured capacitance value. It achieves an accuracy of 0.5mmHg [11].

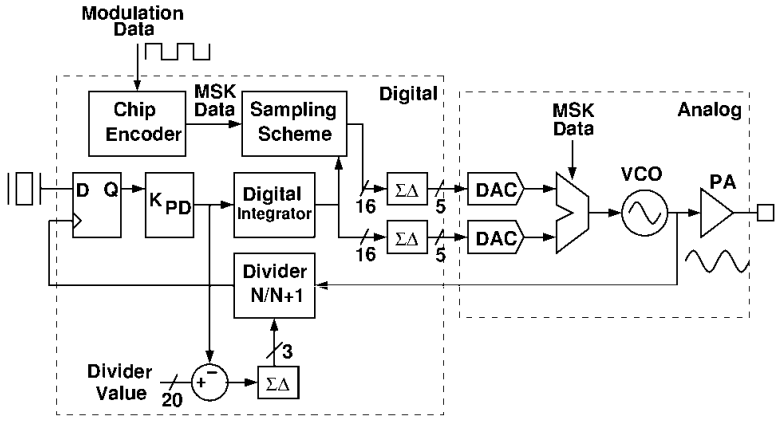

Figure 9. The integrated Zigbee transmitter enables us to achieve reliable data transmission while keeping the system power low [8].

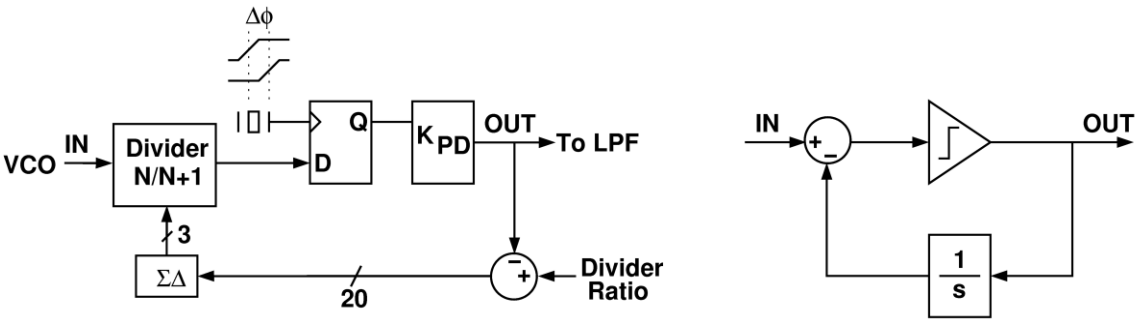

Figure 10. The digital phase detector uses digital flip-flops to detect the phase difference between the VCO output and the crystal reference. This scheme is similar to a delta modulator shown on the right [8].

6.1 Phase Detector

The phase detector (Figure 10) uses a digital flip-flop to convert phase the difference, $\Delta\varphi$, between the VCO and the reference clock. The role of the phase detector is to keep the phase difference between the reference and divider clocks small. In frequency domain, the phase detector consists of a quantizer in the feed forward path and an integrator in feedback path, forming a delta modulator. The delta modulator helps keep $\Delta\varphi$ to within one delay of flip flop. The quantization noise from the fractional-N $\Sigma\Delta$ modulator of the divider provides dithering for the phase detector.

6.2 Frequency Switching Scheme

Using a two-point self-calibrated frequency modulation scheme (Figure 11) we can achieve modulation rates much higher than the PLL bandwidth [25]. For 2-FSK VCO control signal comes from one of the two paths that correspond to the two frequencies, namely f^+ for the upper frequency of carrier and f^- for lower frequency of carrier signal. Once transmission starts, at the end of each bit, the value of VCO control signal is digitally stored. The difference, *Delta*, between the control word for f^+ and f^- is calculated and used to help the PLL modulate at high speed. This difference is added to the VCO control for frequency f^+ to improve the initial VCO control value for frequency f^-. After a few iterations, *Delta* converges to the correct VCO input difference for the required frequencies f^+ and f^- .When *Delta* converges, the frequency switching rate is independent of the bandwidth of the PLL because the correct input to the VCO is preset for each data bit. An example of settling behavior is shown in Figure 11, where after a few data transitions, VCO control inputs for the two frequencies that result in accurate output frequencies are determined. As shown in Figure 11, a digital IIR filter removes the sampling noise from the difference between f^+ and f^- and two control paths for the VCO are formed with DACs. An analog multiplexer switches between the two VCO control voltages generated by the DACs at each data transition.

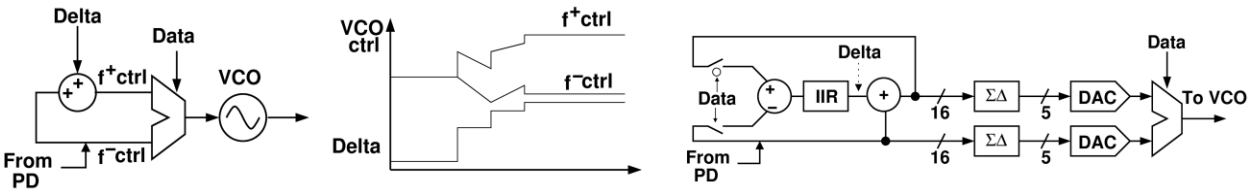

Figure 11. The two-point frequency modulation scheme, an example of settling behavior, and detail of modulation scheme [8].

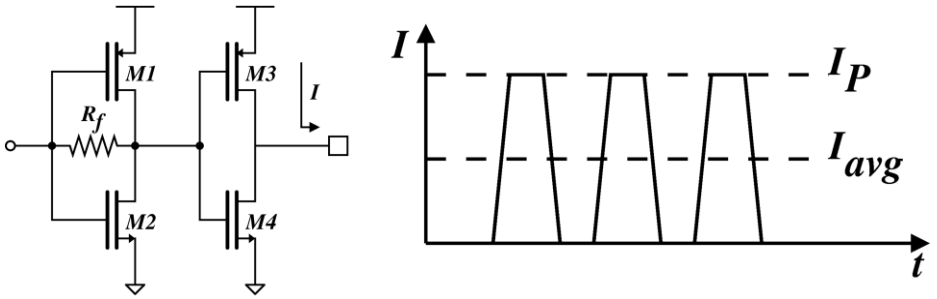

Figure 12. The two-stage resistor feedback inverter-based power amplifier [8].

6.3 Power Amplifier

CMOS technology is known to have limited power delivery capacity when it comes to power amplifiers (PAs). As we move to more advanced CMOS process nodes, the maximum supply voltage drops, limiting the number of transistors we can stack in analog blocks. As a result of this trend, simple inverter-based PA's are suitable candidates in highly integrated solutions. The PA used in this work is a two-stage inverter-based PA. The first stage is an inverter amplifier with resistive feedback. The first stage of the PA is self-biased. Due to the DC feedback path provided by R_f, the bias point of the first stage is set at the middle of the analog (high gain) swing range improving the linearity of the PA. The input impedance of the first stage is important because the PA directly loads the VCO. The second stage is sized to deliver 0dBm to a 50Ω load. This compact inverter-based PA eliminates the need for bulky matching components to drive the antenna. Drawing 4.5mA, the measured power efficiency of the PA is about 17%.

7. CONCLUSION

We demonstrate a miniature sensor node that is suitable for infrastructure monitoring. Its compact size of 8.75mm^3, together with its solar energy harvesting capability makes it a suitable candidate for such applications. Our proposed system includes a solar harvester, a digital microprocessor, a Zigbee transmitter, a thin-film battery, capacitance and temperature sensors, and retentive and non-retentive memories. The use of low-power techniques and the shifting of the design complexity toward digital domain enable us to lower the system active power down to 7.7µW and the transmitter power to 17mW. The Zigbee transmitter uses a self-calibrated two-point modulation fractional-N PLL and simple power amplifier to achieve power levels much lower than that of commercial transmitters.

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