

New techniques for efficient flexible wireless transceivers in nanometer CMOS

M. P. Flynn, D. T. Lin, M. Ghahramani and L. Li

Dept. of EECS, University of Michigan, 1301 Beal Ave., Ann Arbor, MI USA 48109-2122

ABSTRACT

Nanometer CMOS processes have proven to be surprisingly effective for analog and RF design. New design techniques have greatly improved the efficiency of ADCs and RF interfaces and also enabled new flexibility. Moving to techniques that are more digital in nature allows fast and easy changes in architecture and performance. Furthermore, from the standpoint of energy efficiency there can be fundamental advantages to processing signals in the digital domain. This paper discusses digital dominant nanometer CMOS transmitter and receiver schemes that are the basis of flexible efficient wireless transceivers for the MAST platforms.

Keywords: RF, receiver, transmitter, baseband, CMOS, mixed-signal.

1. INTRODUCTION

Modern electronic devices, such as cell phones and wireless sensor nodes, integrate several wireless transceivers to support the growing number of specialized wireless communication standards. The need to support several different wireless standards including Wi-Fi, ZigBee, GSM etc. increases the design complexity of the wireless transceiver circuits and increases the size, cost, and power consumption of the electronic devices that use these circuits. At the same time, advances in circuit fabrication technology favor digital circuits and make traditional analog transceiver circuits more difficult to design. Therefore, next-generation wireless transceivers must be sufficiently configurable to support many standards and implement circuit operations that are more digital in nature to better suit advanced IC technologies.

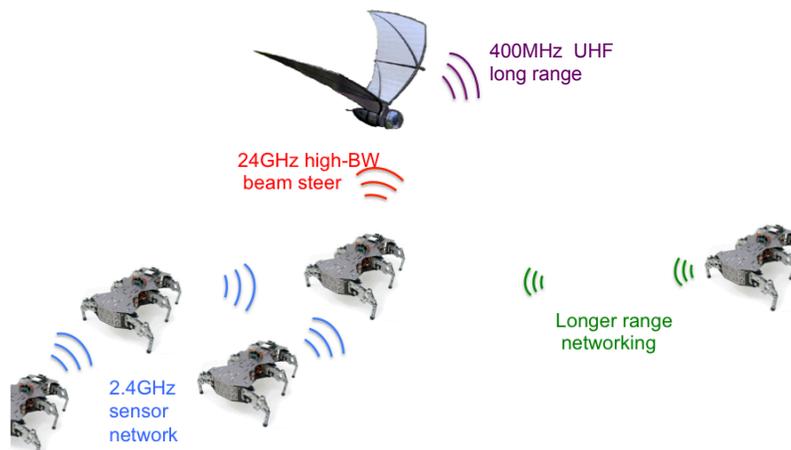


Figure 1. A variety of wireless communications standards support security and environmental monitoring applications.

Figure 1 shows a sample of the plethora of wireless communication schemes that might be applied in security or environmental monitoring applications. In the figure, mobile and fixed sensors are networked through communication over the 2.4GHz ISM band. The 2.4GHz band offers a good compromise between antenna size and communication range for small sensors. The IEEE 802.15.4 standard¹ and its derivative, Zigbee, have become popular choices for this type of networking. Wi-Fi (802.11)² can also be used and has the advantage of a higher data rate. Figure 1 also depicts a high frequency link for short-range very-high-bandwidth communication to a mobile flyer. Beam steering makes this link more robust to jamming and interferers and also makes more efficient use of transmit power. Long-range

communication is facilitated by a UHF link. Traditionally these many standards, even those that use the same RF band, such as 802.15.4 and Wi-Fi, require very different and distinct transceivers. Furthermore, these transceivers are typically designed for worst-case scenarios, and in principal a more flexible circuit could adapt its performance to minimize energy consumption for specific signal conditions. An important goal is the development of new transceiver schemes that can function with different types of communication and that can adapt to a changing wireless environment.

Most transceiver designs are based on the super-heterodyne technique pioneered by Edwin Armstrong in the 1920s. This architecture is resilient and efficient but not very flexible. As a highly flexible alternative, Mitola³ proposed the notion of a *software* radio. In a software radio, a very-fast, high-resolution ADC digitizes a wide band of spectrum. Channel selection and demodulation are performed entirely in software. Although highly flexible, a software radio is limited both by ADC performance and by the power required for high speed DSP. Recently, flexible *mixed-signal* receiver and transmitter schemes have been proposed that are as energy efficient as the traditional completely-analog approaches. Furthermore, these digital dominant mixed signal schemes are better suited to nanometer, digital-CMOS process technologies. As examples, a high frequency sampling receiver^{4,5} and a frequency-mixing and sampling receiver⁶ have demonstrated performance that meets the requirements of prevalent communication standards. However, these receiver designs can be further improved by optimizing across the entire architecture. Cartesian transmitters tend to be power hungry and the use of analog components makes them unsuitable for integration in modern digital processes. Many of the more-digital RF transmitters in the literature⁷ are inferior in performance to their analog counterparts and suffer from problems such as the generation of spurious tones. We have developed a low power digital-dominant phase-locked-loop (PLL) based transmitter⁸ and a flexible receiver⁹ with configurable filtering embedded in a SAR ADC that achieve comparable performance to analog counterparts.

Our transceiver design simplifies the analog circuits and shifts much of the analog functionality to digital circuits. Our proposed transmitter scheme also alleviates some shortcomings associated with traditional digital PLL-based transmitters. A significant challenge in the design of a receiver is the filtering of unwanted interfering signals. This filtering is traditionally implemented with analog circuits or off-chip discrete filters. A flexible but energy intensive alternative is to digitize the spectrum of interest with a fast, high-resolution analog to digital converter (ADC) and perform filtering with digital-signal-processing (DSP) techniques. As an energy-efficient yet flexible alternative, we introduce a flexible receiver that embeds a configurable discrete-time (DT) filter within the ADC. Furthermore, a wideband, inductor-less front-end ensures compatibility with a wide-range of carrier frequencies.

2. FLEXIBLE RECEIVER

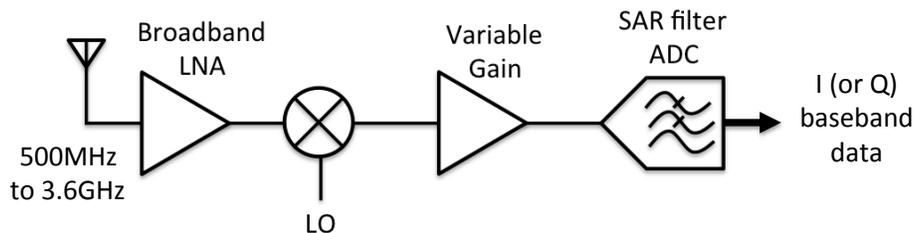


Figure 2. Simplified block diagram of the flexible receiver architecture showing I (or Q) channel.

Figure 2 shows a block diagram of the proposed flexible receiver architecture⁹. A wideband front-end amplifies and direct down-converts the RF signal to baseband. The baseband signal is amplified and then digitized and filtered by a filtering-SAR ADC. Unlike a conventional receiver, the combined filter-SAR ADC provides both channel filtering and digitization. With little analog circuitry compared to other ADC architectures, the SAR ADC architecture is ideally suited to nanometer CMOS and is very energy efficient. A traditional SAR ADC consists of a capacitive DAC that under control of a successive approximation register (SAR) performs a successive approximation of the analog input. The innovation here is to use the same capacitors to implement both *filtering* and *digitization*. The DAC consists of unit capacitors and switches. The implementation of an *analog DT* filter also consists of capacitors and switches, so we implement an analog DT pre-filter by modifying the ADC sampling process. Since the switches are programmable, the filter configuration is flexible and programmable and can be tailored to different wireless communication standards.

A prototype receiver is fabricated in 65nm CMOS and occupies an active die area of 0.24mm². The wideband front end supports carrier frequencies ranging from 500MHz to 3.6GHz. The DT filter is configurable to operate in a no filter

mode, a FIR only filter mode, or a FIR and IIR filter mode. The FIR tap lengths and tap weights are programmable from a set ranging from 16 to 64 taps and 0 to $6C_{\text{unit}}$, respectively. The baseband amplifiers have 5 configurable gain levels.

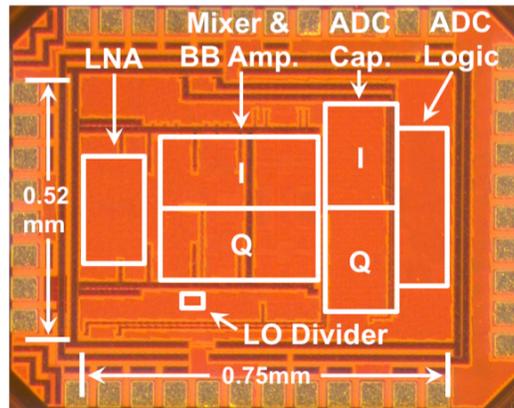


Figure 3. Die photo of the configurable wideband receiver. The major function blocks are identified.

This new architecture supports many communication standards and bands. By enabling variants of the configurable DT filter along with different sampling rates and filter parameters, we have demonstrated standard-compliant reception of IEEE 802.15.4 packets transmitted in the 915MHz and 2450MHz and also successful reception of IEEE 802.11 (Wi-Fi) packets.

3. FLEXIBLE TRANSMITTER

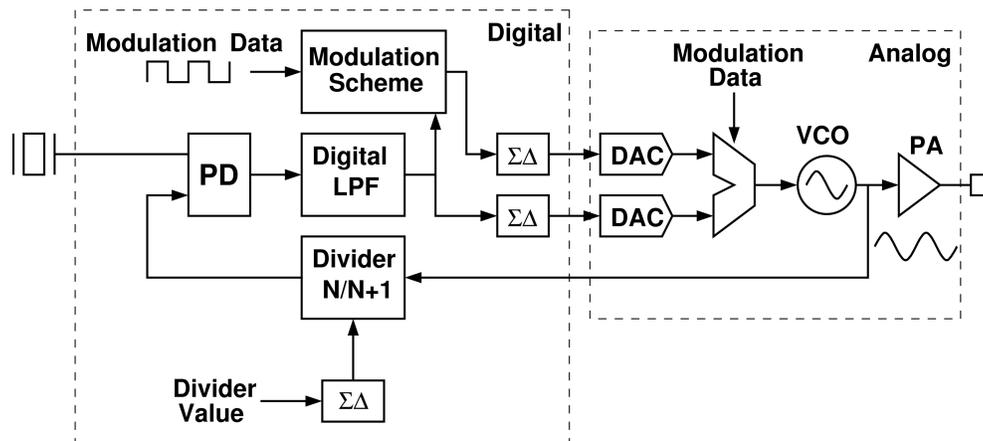


Figure 4. Block diagram of the digital PLL-based transmitter/modulator

Figure 4 shows the block diagram of a low power digitally-dominant PLL-based transmitter that is well-suited to integration in nanometer CMOS processes. Phase or frequency modulation can be achieved with a PLL by adjusting the feedback divider ratio. The fractional- N based PLL architecture enables non-integer divide ratios permitting small changes in output frequency or phase. The transmitter is comprised of a mostly-digital fractional- N PLL modulator and a simple power amplifier (PA). A digital phase detector compares the reference clock and the divided down voltage controlled oscillator (VCO) output. In this design, the phase detector is formed with a 1-bit over-sampled phase quantizer thus reducing the risk of spurious tones. A digital low-pass filter averages the phase detector output and sets the VCO control voltage. The output of the digital low-pass loop filter is converted to the analog domain by a resistor-string digital to analog converter (DAC). Only the DAC and VCO are analog circuits. Two control paths, incorporating two DACs and a digital sampler, enable frequency modulation at a rate much higher than the loop bandwidth. A simple PA delivers power to the transmit antenna. A variant of this architecture has been developed to implement almost any constant envelope modulation. A 2.4GHz prototype IC¹⁰ implements GMSK, OQPSK and BSK.

4. FLEXIBLE RECEIVER DEMONSTRATION SYSTEM

4.1 Overview

A complete wireless receiver system combines the custom multi-band, multi-standard 65nm CMOS receiver with a real-time baseband demodulator on an FPGA, to create a full-functioning flexible wireless demonstration system. The demonstration showcases a system built around a highly-integrated receiver IC that captures the RF input and outputs digital baseband bitstreams. The wideband front-end and SAR ADC with embedded configurable discrete-time (DT) filters ("SARfilter") of the receiver IC allow it to adapt to its environment and to different communication standards. The performance of this receiver is verified⁹ with both the 915MHz and 2450MHz bands of IEEE 802.15.4¹ and IEEE 802.11². A custom digital baseband demodulator implemented on a FPGA performs real-time digital phase correction, symbol timing acquisition, and demodulation. Additional custom FPGA logic interfaces the demodulator to a video driver, in order to create a complete hardware demonstration system that receives, demodulates, and displays images.

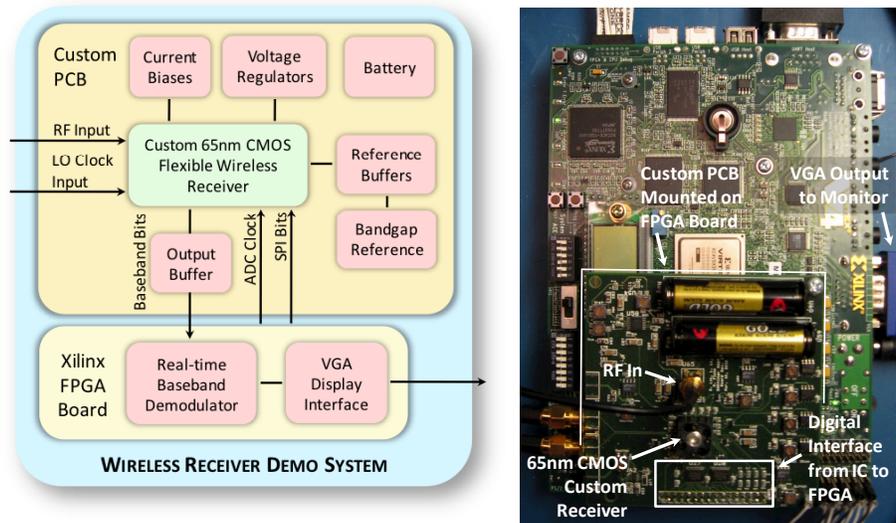


Figure 5. High-level diagram of the wireless receiver system and photo of complete system, based on custom flexible receiver IC. The baseband processing and display driver are implanted on a Virtex-4 development board.

The system is a complete wireless receiver system, as shown in Figure 5, except that an off-board clock source provides the mixer LO. The primary receiver functions are implemented by a custom 65nm CMOS integrated circuit. This receiver chip is mounted on a custom PCB daughter-board alongside off-the-shelf support components. This daughter-board is mounted on a Xilinx FPGA development board. Custom logic on the FPGA digitally corrects phase offset, acquires symbol timing information, and then demodulates the baseband bitstream output from the receiver. The demodulated data is buffered on the FPGA and then sent to a video driver for display through a VGA interface. The FPGA also provides the receiver with digital configuration bits over an SPI bus, and an ADC clock.

4.2 Printed Circuit Board (PCB)

The PCB is a custom four-layer FR-4 board. In order to make the system as compact as possible, external sources have been replaced with on-board, off-the-shelf components. Two AAA batteries power the system; the supplies are tapped from one or both batteries depending on the required voltage. A linear regulator supplies 1V to the three voltage domains on the chip: clock, analog, and digital. The three domains are isolated with pi filters. The current biases for the receiver are provided by current source ICs. The voltage references for the SAR ADC are generated by resistively dividing the output of a bandgap reference, then buffering the divided voltages with op-amps in unity gain feedback.

The LO clock is the only source that is not supplied by either an off-the-shelf surface mount component or the FPGA development board. An off-board clock source is currently used, but the PCB is designed to support future work on an oscillator based on switchable thin-film resonators¹¹. The board has an auxiliary linear voltage regulator to supply the transistors of the oscillator and a switching voltage regulator to supply a high-voltage bias to the resonators.

4.3 FPGA Development board

A Xilinx ML402 Virtex-4 (XC4VSX35) FPGA development board interfaces between the receiver and the user. The receiver IC captures an RF signal containing 802.15.4 2450MHz band demonstration-image packets and outputs I/Q modulated baseband data to a custom real-time digital baseband demodulator implemented on the FPGA. The demodulator digitally synchronizes the phase and symbol timing of the baseband bitstream, and then demodulates the corrected bitstream. As data containing the next image pixels are processed by the demodulator, the previously demodulated pixel color and location data are buffered and sent through custom interface logic to a video driver on the FPGA board. The video driver displays the image on a VGA monitor through an onboard VGA interface (Figure 5). This verifies the successful interoperation of a long chain of signal processing hardware spanning the entire receiver system. The FPGA also sets the control bits of the receiver IC. A digital clock manager (DCM) module on the FPGA converts a 100MHz crystal clock source on the development board to a 64MHz sampling and SAR clock for the ADC. With a 16-tap filter enabled, this clock rate results in an ADC conversion rate of 4MS/s

4.4 Initial Matlab Design

The baseband demodulation algorithm for the 2450MHz band of 802.15.4 was initially designed and evaluated in MATLAB, then ported to a real-time digital logic implementation on the FPGA. As the first demodulation step, the digital baseband demodulator corrects the phase offset in the I/Q waveforms. As an example of the correction process, sixteen symbols per channel of measured modulated baseband I/Q output from the SARfilter ADC, at 4MS/s per channel, are shown in Figure 6(a). The resulting internal signals of the demodulator are shown in (b), (c), and (d). The raw output exhibits a phase offset that results from the phase difference between the up- and down-conversion LO clocks, which is digitally corrected. A frequency offset can likewise be corrected with minor modifications to the correction procedure.

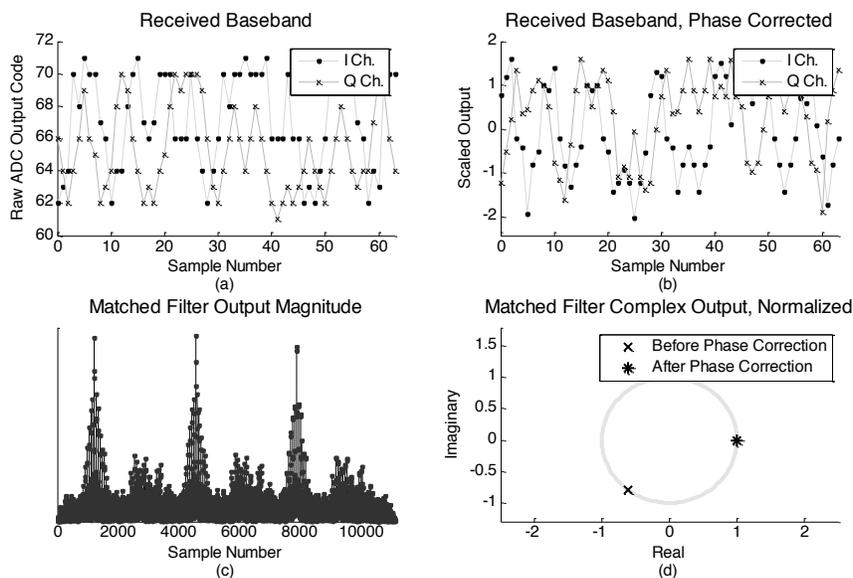


Figure 6. Measured modulated digital baseband at 4MS/s and the resulting internal signals of the MATLAB demodulator processes the bitstream. The FPGA demodulator is similarly implemented.

The demodulator first removes the DC offset and scales the signal to a desired amplitude. It then performs (complex) matched filtering of the received bitstream to the packet's synchronization header (SHR). The magnitude of the filter output is shown in Figure 6(c) for a bitstream that contains 3 consecutive packets, as seen by the correlation peaks. This matched filter serves three purposes. First, peaks in the magnitude identify the presence of a packet. Second, the peak magnitude location provides symbol timing information. And third, the relative energy in the I and Q channels at the peak magnitude location identifies the phase offset.

The third point above is depicted Figure 6(d), in which the energy of the I (real) and Q (imaginary) channels at the peak magnitude location is normalized to unit magnitude and plotted on the complex plane. The phase offset, ϕ , in this

example is approximately -127° before phase correction and is reduced to a negligible value by multiplying the (complex I/Q) input bitstream by $e^{-j\phi}$. The phase corrected samples are shown in Figure 6(b). If a frequency offset also exists, it can be observed as a linearly changing phase offset and can be corrected by match filtering to subsets of the SHR. The frequency offset can then be calculated from the output phase ramp and corrected. For demodulation¹², the samples are weighed by half-sine pulse shapes and summed over each symbol period to determine a corresponding chip value. Groups of chips are then compared to the 16 known 2450MHz band spreading codes to determine the symbol that is closest in (Hamming) distance.

4.5 FPGA Demodulator

The demodulator design developed in MATLAB is mapped to digital logic implementation on a Xilinx Virtex-4 FPGA. The FPGA demodulator is similar to the MATLAB implementation. The most significant functional difference is it identifies the SHR by searching for an output magnitude that exceeds a preset threshold, since it is impractical to buffer and process a large number of the matched filter outputs at once.

5. CONCLUSION

As modern devices integrate increasingly more wireless connectivity into a small form-factor, traditional wireless architectures have to be abandoned in favor of digital-dominant approaches. Our receiver and transmitter architectures achieve good performance by employing a design strategy that shifts circuit complexity to mixed-signal and digital circuits that perform well in advanced CMOS integrated circuit technologies. Moving forward, designers will continue to blur the distinction between analog, mixed-signal, and digital circuits and create systems that take advantage of the “intelligence” that can be designed with small, low-power digital logic. We foresee next-generation wireless transceivers as intelligent systems that constantly adjust gain, filtering, ADC conversion rate, and other parameters in real-time, in order to optimize both energy use and performance.

REFERENCES

- [1] Part 15.4: Wireless Medium Access Control (MAC) and Physical Layer (PHY) Specifications for Low-Rate Wireless Personal Area Networks (WPANs), IEEE Standard 802.15.4, 2006.
- [2] Part 11: Wireless LAN Medium Access Control (MAC) and Physical Layer (PHY) Specifications, IEEE Standard 802.11, 2007.
- [3] J. Mitola, “The software radio architecture,” IEEE Communications Magazine 33(5), 26–38 (May 1995).
- [4] R. Staszewski, K. Muhammad, D. Leipold et al., “All-Digital TX Frequency Synthesizer and Discrete-Time Receiver for Bluetooth Radio in 130-nm CMOS,” IEEE J. Solid-State Circuits 39(12), 2278-2291 (Dec. 2004)
- [5] K. Muhammad, Y. Ho, T. L. Mayhugh et al., “The First Fully Integrated Quad-Band GSM/GPRS Receiver in a 90-nm Digital CMOS Process,” IEEE J. Solid-State Circuits 41(8), 1772-1783, (Aug. 2006)
- [6] R. Bagheri, A. Mirzaei, S. Chehrazi et al., “An 800-MHz-6-GHz Software-Defined Wireless Receiver in 90-nm CMOS,” IEEE J. Solid-State Circuits 41(12), 2860-2876, (Dec. 2006).
- [7] L. Xu, S. Lindfors, K. Stadius, J. Ryyanen, “A 2.4-GHz Low-Power All-Digital Phase-Locked Loop,” IEEE J. of Solid State Circuits 45(8), 1513-1521, (Aug. 2010).
- [8] M. A. Ferriss, M. P. Flynn, “A 14 mW Fractional-N PLL Modulator with a Digital Phase Detector and Frequency Switching Scheme,” IEEE J. Solid-State Circuits 43(11), 2464-2471, (Nov. 2008).
- [9] D. T. Lin, L. Li, S. Farahani, M. P. Flynn, “A Flexible 500MHz to 3.6GHz Wireless Receiver with Configurable DT FIR and IIR Filter Embedded in a 7b 21MS/s SAR ADC,” IEEE Custom Integrated Circuits Conf. (CICC), (Sept. 2010).
- [10] M. Ferriss, D. T. Lin, M. P. Flynn, “A Fractional-N PLL Modulator with Flexible Direct Digital Phase Modulation,” IEEE Custom Integrated Circuits Conference (CICC), (Sept. 2009).
- [11] V. Lee, S.A. Sis, X. Zhu, A. Mortazawi, “Intrinsically Switchable Interdigitated Barium Titanate Thin Film Contour Mode Resonators,” IEEE International Microwave Symposium (MTT) Digest, 1448-50, (May 2010).
- [12] F. Xiong, [Digital Modulation Techniques], Artech House, Boston, 207-226 (2006).