A Cascaded Noise-Shaping SAR Architecture for Robust Order Extension

Lu Jie, *Member, IEEE*, Boyi Zheng, *Member, IEEE*, Hsiang-Wen Chen, *Member, IEEE*, and Michael P. Flynn, *Fellow, IEEE*

***Abstract*— The emerging noise-shaping (NS) successive approximation (SAR) architecture is highly efficient and compact; however, the order and signal-to-noise ratio (SNR) of sub-MHz NS SAR ADCs are still lower than conventional sigma–delta ADCs. This work proposes a cascaded NS (CaNS) SAR architecture that increases system order and enables more effective NS for higher SNR. The proposed architecture enhances the robustness of high-order NS performance at the system level and is inherently process, voltage and temperature (PVT) stable. A two-phase settling technique improves the efficiency of residue amplification without sacrificing robustness. A prototype CaNS SAR ADC, fabricated in 28-nm CMOS, occupies 0.02 mm^2 and consumes 120 μW. The measured Signal to Noise and Distortion Ratio (SNDR) over 100-kHz bandwidth is 88 dB, resulting in a Schreier Figure of Merit (FoM) of 177 dB.**

***Index Terms*— ADC, cascade form, discrete-time (DT) amplifier, noise shaping (NS), successive approximation (SAR).**

I. Introduction

HIGH-RESOLUTION, sub-MHz bandwidth data converters are essential for emerging applications, such as sensors and Internet-or-Things (IoT) devices. For these applications, high signal-to-noise ratio (SNR), high energy efficiency, and low cost are essential. The sigma–delta (SD) architecture is attractive because it provides high SNR; however, the dependence on op-amps makes conventional SD ADCs large and power hungry. The emerging noise-shaping (NS) successive approximation (SAR) architecture [1] is a compelling alternative because it combines the efficiency and area advantages of the SAR ADC architecture with NS. A further advantage is that many recent NS SAR designs are opamp-free. However, most reported sub-MHz NS SAR ADCs [2]–[4] are limited to medium-to-high SNR, in part because they are restricted to low-order NS.

To better compare different architectures, Fig. 1 plots the energy efficiency versus Signal to Noise and Distortion Ratio (SNDR) for high-resolution sub-MHz (10 kHz–1 MHz) bandwidth ADCs from [5].

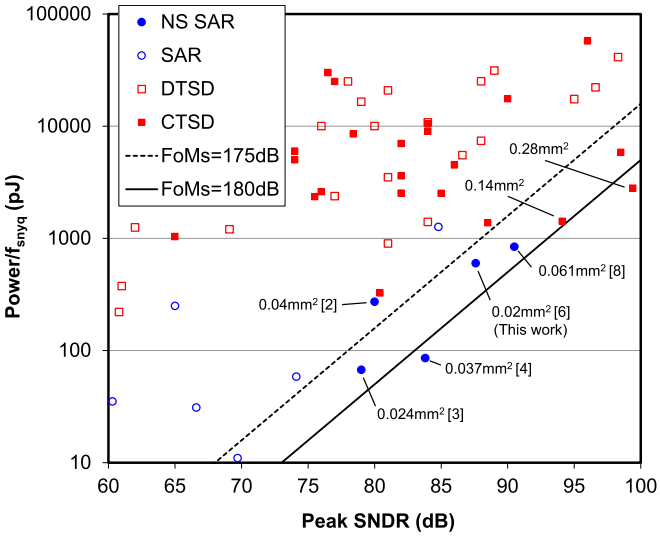

Fig. 1. Comparison of state-of-the-arts sub-MHz ADC designs.

As shown, conventional SD ADCs offer high SNDR but tend to have low power efficiency. Some continuous-time (CT) SD ADCs are more efficient, but a disadvantage is that CTSD ADCs generally require capacitor tuning and are relatively large in terms of die area. In contrast, NS SAR ADCs are highly efficient and are noticeably smaller. However, the SNDR of most existing NS SARs is inadequate for many sub-MHz applications. Furthermore, many highly efficient NS SAR ADCs rely on low-power dynamic amplifiers (DAs), which potentially suffer from large performance variation under process, voltage and temperature (PVT) variation and may require complicated calibration.

In this work, we introduce the cascaded NS (CaNS) SAR architecture [6], which cascades two second-order NS stages to provide a fourth-order noise transfer function (NTF) for high resolution while consuming similar power and area to an NS SAR with a second-order NTF. The higher order of the proposed architecture significantly enhances robustness and eliminates the need for PVT calibration. Two-phase settling improves amplification efficiency without the need for DAs. The prototype CaNS SAR ADC has a measured SNDR of 88 dB over a 100-kHz bandwidth and consumes 120 μW from a 1-V supply, resulting in a Schreier Figure of Merit (FoM) of 177 dB. Implemented in 28-nm CMOS, it occupies only 0.02 mm^2. The proposed NS-SAR architecture is an area-efficient alternative to SD ADCs for high-resolution, low-power, area-critical applications.

To better understand the inherent advantage of the proposed design, Section II reviews the system-level considerations for

Manuscript received May 8, 2020; revised July 11, 2020; accepted August 21, 2020. Date of publication September 7, 2020; date of current version November 24, 2020. This article was approved by Guest Editor John P. Keane. This work was supported in part by the Semiconductor Research Consortium (SRC) under Project 2712.007. This article was presented at the 2020 IEEE International Solid-State Circuits Conference (ISSCC). *(Corresponding author: Lu Jie.)*

The authors are with the Electrical Engineering and Computer Science (EECS) Department, University of Michigan, Ann Arbor, MI 48109 USA (e-mail: jielu@umich.edu).

Color versions of one or more of the figures in this article are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/JSSC.2020.3019487

0018-9200 © 2020 IEEE. Personal use is permitted, but republication/redistribution requires IEEE permission.
See https://www.ieee.org/publications/rights/index.html for more information.

Authorized licensed use limited to: University of Michigan Library. Downloaded on December 02,2020 at 03:43:06 UTC from IEEE Xplore. Restrictions apply.

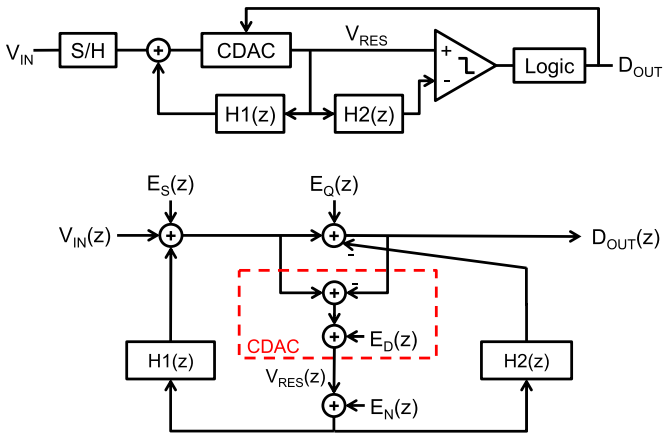

Fig. 2. Generalized behavioral (top) and signal (bottom) model of NS SAR.

NS SAR. Section III introduces the CaNS SAR. Section IV discusses the implementation of the prototype CaNS SAR ADC. Section V explains and analyzes the multiphase settling scheme for high-efficiency residue amplification. Following this, Finally, Sections VI presents measurement results and Section VII provides conclusions.

II. System-Level Considerations for High-Resolution NS SAR

A. Design Factors in NS SAR

Although actual implementations vary, most NS SAR ADCs can be generalized with the behavioral signal model shown in Fig. 2.

Here, $V_{\mathrm{IN}}(z)$ is the analog input signal, and $D_{\mathrm{OUT}}(z)$ is the digitized output. $E_S(z)$ represents the errors or noise during sampling (e.g., kT/C noise), and $E_Q(z)$ is the quantization error (including comparator noise) from SAR. The CDAC generates a residue, $V_{\mathrm{RES}}(z)$, after each round of quantization, with a distortion error (E_D) from DAC nonlinearity and mismatch. $H1(z)$ and $H2(z)$ are the loop filters for different feedback paths, and $E_N(z)$ is the input-referred noise of these filters. An all-pass signal transfer function (STF) processes the input signal. The following NTFs shape the errors E_Q, E_D, and E_N:

$$\mathrm{STF} = \mathrm{NTF_S} = 1 \tag{1}$$

$$\mathrm{NTF_Q} = \frac{1 - \mathrm{H1(z)}}{1 - \mathrm{H2(z)}} \tag{2}$$

$$\mathrm{NTF}_N = \mathrm{NTF}_D = H1(z) - \frac{H2(z)}{1 + H2(z)}. \tag{3}$$

In-band NTF_N and NTF_D are approximately all-pass, and therefore, neither E_N nor E_D is suppressed.

Most of the specifications of an NS SAR directly relate to factors in the generalized behavioral model. SNR is a function of E_Q, E_D, E_N, and E_S, over-sampling rate (OSR), and the NTFs, while the noise requirement (E_N) of the loop filter usually dominates the power consumption (P) of a high-resolution NS SAR. The CDAC determines the area (A) and thus strongly depends on E_S and E_D. Finally, the sensitivity of the NTF determines the PVT robustness of an NS SAR ADC.

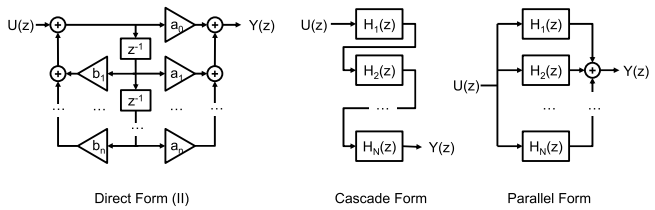

Fig. 3. Different DT filter implementation forms.

We modify the Schreier and Sauerbrey's FoM [7] to consider both area and robustness

$$\mathrm{FoM_{NSSAR}} = \mathrm{SNR_{worst}} + 10\log_{10}\sqrt{\frac{\mathrm{BW}}{P \cdot A \cdot \mathrm{OSR}}} \tag{4}$$

where $\mathrm{SNR_{worst}}$ is the worst case SNR in dB under PVT variation for a certain yield, BW is the effective bandwidth in Hz, P is the total power consumption in watts, and A is the area in mm^2. This FoM definition assumes that the error is dominated by thermal noise ($\propto P^{-1}\mathrm{BW}$) and kT/C noise ($\propto A^{-1}\mathrm{OSR}^{-1}$). Assuming that both types of noise are comparable in a reasonable design, then both ($P^{-1}\mathrm{BW}$) and ($A^{-1}\mathrm{OSR}^{-1}$) should decrease by 3 dB to increase SNR by 3 dB. In the following discussion, we use this $\mathrm{FoM_{NSSAR}}$ to compare NS SAR ADCs with different system designs.

B. NS SAR With Different System Design

Existing work applies circuit-level techniques, such as passive filtering [2], [8] and calibration [3] to improve performance and PVT robustness. Instead, we consider higher level solutions related to system order and the form of the NTF. Our approach is inspired by the discrete-time (DT) filter theory, which shows that the robustness of a filter strongly depends on its structure, especially for higher order filters. Fig. 3 shows the three most common DT filter structures: direct form, cascade form, and parallel form.

Almost all NS SAR designs use the direct form. The direct form is the most straightforward and is easily constructed from the filter coefficients. However, the direct form has several inherent disadvantages. It needs many summing blocks and requires relatively large coefficient magnitudes, both of which increase the cost in terms of power and area. Also, the direct form suffers from high sensitivity to variation in coefficients gain, which in practice means poor PVT robustness.

The cascade filter form is the most robust against coefficient variation and requires less coefficient gain. Unlike the parallel form, the cascade form enables direct, independent control of each zero (pairs), and thus has even lower coefficient sensitivity than the parallel form [9]. Another advantage of the cascade form is that the later stages filter the noise of the early stages, which reduces the overall in-band noise.

Before we introduce the proposed CaNS SAR in Section III, we first compare the performance of different NS SAR systems to illustrate the advantage of cascading. We build a theoretical model (described in Appendix I) and investigate the maximum performance ($\mathrm{FoM_{NSSAR}}$) of NS SAR ADCs by global optimization. Fig. 4 shows the results of this modeling.

Authorized licensed use limited to: University of Michigan Library. Downloaded on December 02,2020 at 03:43:06 UTC from IEEE Xplore. Restrictions apply.

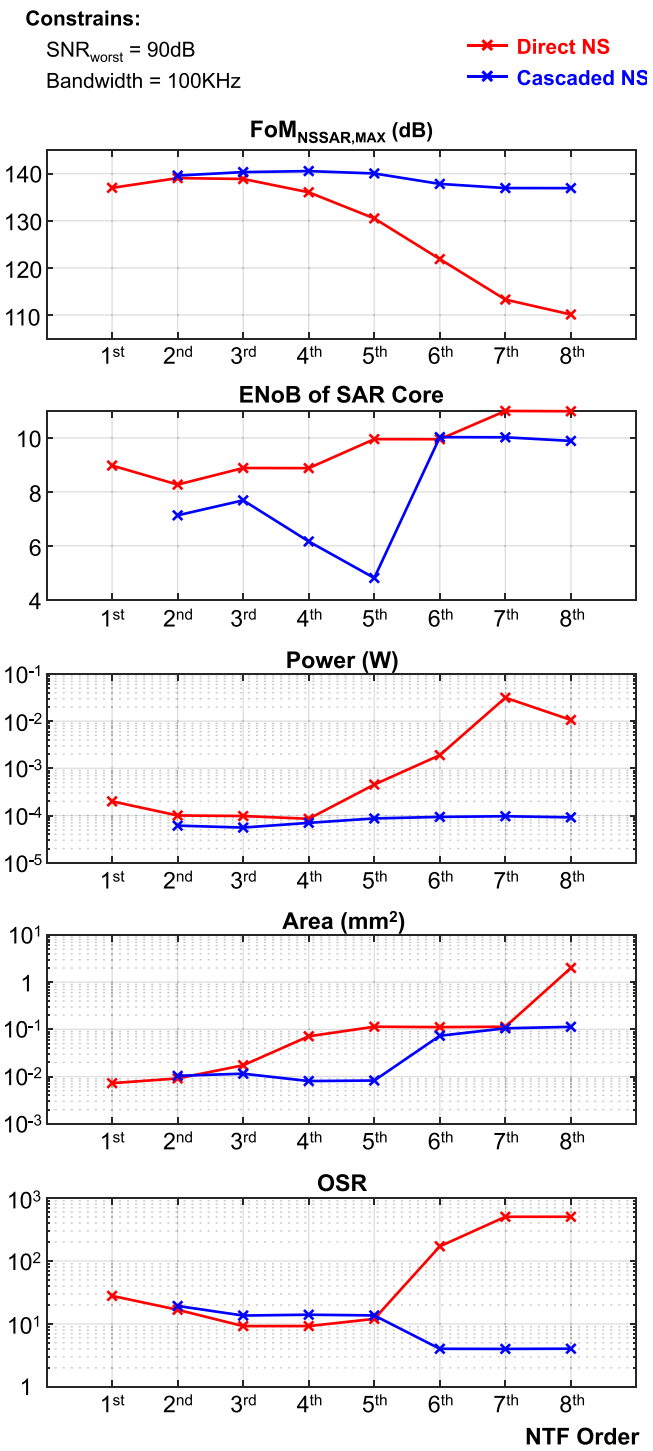

Fig. 4. Optimal FoM$_{NSSAR}$ [see (4)], SAR core ENOB, power, area, and OSR versus NTF order for different NTF forms.

We note that for a certain SNR and BW (90 dB and 100 kHz in our case), the optimal FoM$_{NSSAR}$ for the direct form occurs for a second-order NTF, whereas the peak for the cascade form is with a fourth-order NTF. Indeed, low-order NS is the optimal choice for existing NS SAR ADCs, which use the direct form. However, we also note that a better FoM$_{NSSAR}$ is possible with higher order NS for the cascade form NTF, which is our motivation for investigating the CaNS SAR architecture.

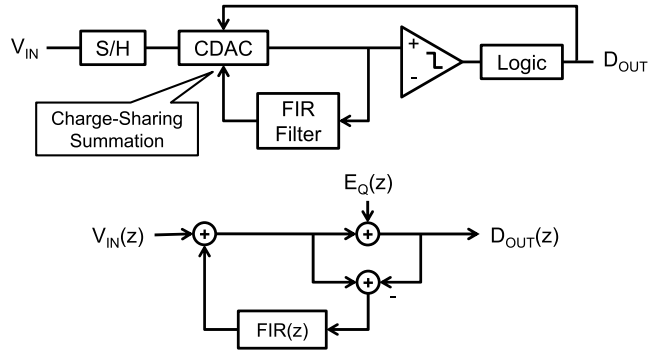

Fig. 5. EF NS SAR and a practical implementation [3].

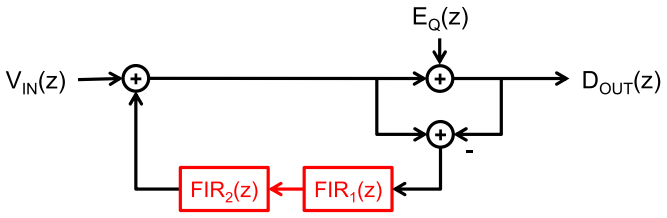

Fig. 6. EF NS SAR with loop filter in cascade form.

III. Proposed CaNS SAR Architecture

A. Error-Feedback Architecture

A practical NS SAR design does not require both the H1 and H2 loop filters, shown in Fig. 3, for high performance. The poles of the NTF are much less critical than the zeros because the quantizer in an NS SAR (i.e., the SAR ADC core) is high resolution. As (2) indicates, an advantage of the H1 filter is that an FIR filter can place the zeros of the NTF, without need for the H2 filter. This configuration is known as the error-feedback (EF) NS SAR architecture [3], as shown in Fig. 5.

Besides its system-level simplicity, the EF architecture also has several circuit-implementation advantages. EF not only eliminates integrators in the loop filter but also removes the requirement for a multi-input comparator. Moreover, the large capacitance of CDAC naturally suppresses the noise from the loop filter. Therefore, in this work, we take advantage of EF in a cascaded architecture.

B. Cascaded Error Feedback

A straightforward "cascading" of an NS SAR might directly cascade the loop filter. As shown in Fig. 6, the cascade of FIR$_1$ and FIR$_2$ implements the FIR filter.

Although such an implementation can reduce the magnitude of the filter coefficients, it does not preserve the ability to independently place the zeros of the NTF, which is an essential advantage of cascade form. The NTF for E_Q is

$$\mathrm{NTF}_Q(z) = 1 - \mathrm{FIR}_1(z) \cdot \mathrm{FIR}_2(z). \tag{5}$$

We note that the zeros of the NTF in (5) are not directly related to FIR$_1$ or FIR$_2$; in other words, cascading the loop filter does not provide a cascade form of the NTF. This problem not only increases design difficulty but also worsens

Authorized licensed use limited to: University of Michigan Library. Downloaded on December 02,2020 at 03:43:06 UTC from IEEE Xplore. Restrictions apply.

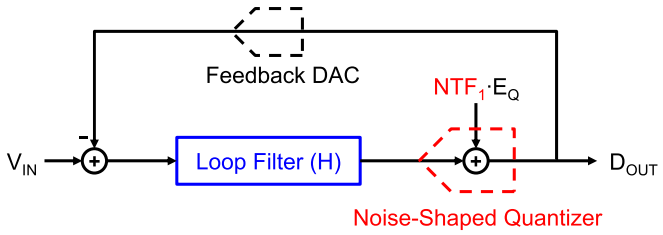

Fig. 7. SD ADC with noise-shaped quantizer.

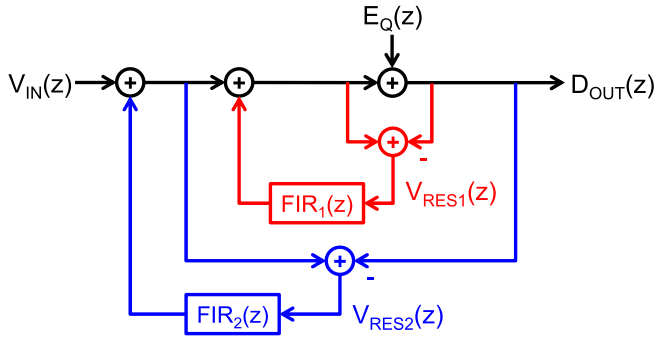

Fig. 8. Proposed CaNS SAR architecture.

the robustness of the NTF. For a fourth-order NTF in the form of (5), the SNR degradation with coefficient variation can be 20 dB larger compared to an NTF with a true cascade form. We provide a more detailed numerical comparison at the end of this section.

Recent work on CT SD ADCs with noise-shaped quantizers [10], [11] suggests a practical alternative to using a cascaded loop filter. Fig. 7 shows an SD ADC with noise-shaped quantizer. In these SD ADCs, an outer modulator loop increases the NS order.

We note that the overall NTF is the product of the two sub-NTFs so that the overall NTF is in cascade form of the two individual NTFs

$$\mathrm{NTF}(z) = \mathrm{NTF}_1(z) \cdot \mathrm{NTF}_2(z) = \frac{\mathrm{NTF}_1(z)}{1 + H(z)}. \tag{6}$$

Inspired by this, we introduce a CaNS SAR structure with similar advantages, as shown in Fig. 8.

We cascade loops with separate loop filters so that the overall NTF is in cascade form and the sub-loop filters independently control the zeros

$$\mathrm{NTF}_Q(z) = (1 - \mathrm{FIR}_1(z))(1 - \mathrm{FIR}_2(z)). \tag{7}$$

We name this architecture CaNS SAR. The input to FIR2 (V_{RES2}) is

$$\begin{aligned} V_{\mathrm{RES2}}(z) &= \mathrm{FIR}_1(z) \cdot E_Q(z) - E_Q(z) \\ &= V_{\mathrm{RES1}}(z) - \mathrm{FIR}_1(z) \cdot V_{\mathrm{RES1}}(z). \end{aligned} \tag{8}$$

Equations (7) and (8) suggest a straightforward implementation of the CaNS SAR, as shown in Fig. 9. Section IV discusses the circuit-level implementation in detail.

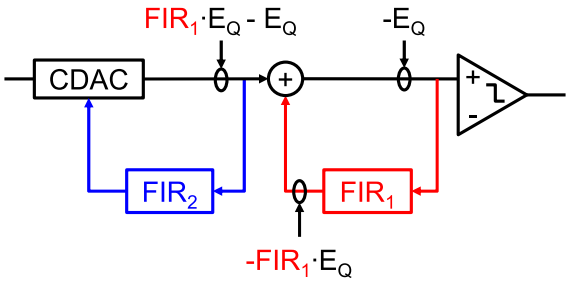

Fig. 9. Straightforward implementation of the CaNS SAR architecture.

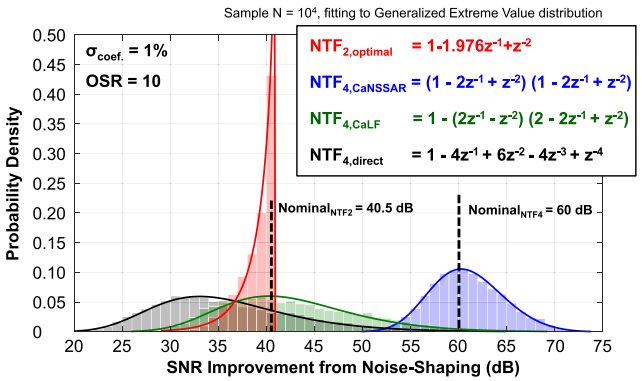

Fig. 10. Performance distributions for four different NTFs for a 1% 1-sigma coefficient variation.

C. Advantages of CaNS SAR

CaNS SAR preserves the system-level advantages of the cascade form. It enables a high-order NTF with small coefficients. The two sub-NTFs independently control the zeros of the NTF. As mentioned, this independent control dramatically reduces the sensitivity of the NTF to coefficient variation. To better illustrate this, Fig. 10 shows the calculated performance distributions for four different NTFs for a 1% 1-sigma coefficient variation. The horizontal axis represents the SNR improvement from NS, assuming an OSR of 10. The NTF of the proposed CaNS SAR provides a much better overall SNR, even accounting for manufacturing variation. We note that the direct-form loop filter and cascaded-form loop filter (see Fig. 6) of the fourth-order NTF perform even worse than the second-order one. The proposed cascaded architecture is crucial for reliable high SNR operation.

At the circuit level, CaNS SAR extends the advantages of EF. The outer loop shapes the noise from the inner loop and the noise from the FIR_1 filter. This shaping greatly relaxes the noise requirements for FIR_1 and thus reduces power and die area. The large capacitance of CDAC suppresses the noise from FIR_2, which is the dominant noise of the system. In effect, this reuse of the CDAC capacitance for FIR_2 noise reduction helps to reduce the area further.

IV. Prototype Implementation

Fig. 11 shows a complete schematic of the prototype CaNS SAR ADC. Besides the cascade EF structure, the remainder of implementation is relatively straightforward. The SAR core

Authorized licensed use limited to: University of Michigan Library. Downloaded on December 02,2020 at 03:43:06 UTC from IEEE Xplore. Restrictions apply.

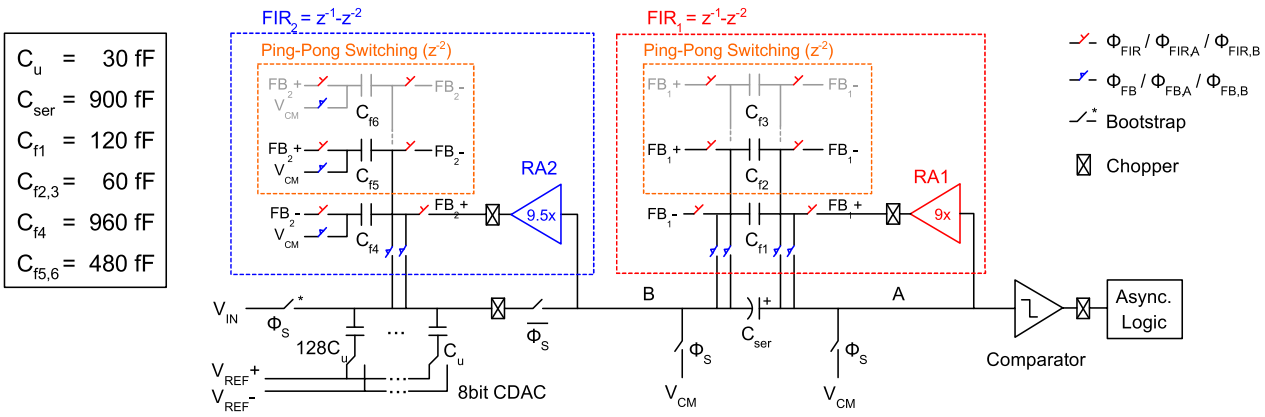

Fig. 11. Schematic of the prototype CaNS SAR ADC.

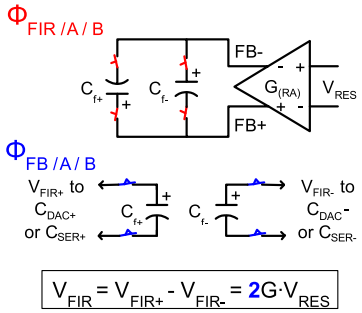

Fig. 12. Cross-differential sampling of FIR capacitors.

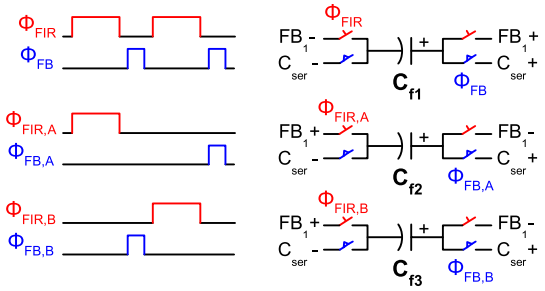

Fig. 13. FIR_1 switches timing. FIR_2 operates with the same timing.

uses an 8-bit CDAC, a Strong-ARM dynamic comparator, and asynchronous SAR logic. The input sampling switch is boot-strapped, whereas the other switches are simple transmission gates. Chopping in the main signal path suppresses flicker noise. CDAC mismatch is canceled with an off-chip calibration. The details about the calibration are described in Appendix II.

A. Circuit Implementation of Cascaded Error Feedback

A serial capacitor (C_{ser} in Fig. 11) cascades the NS stages and also implements the inner loop feedback. [1] C_{ser} is reset before each round of feedback to clear any residual charge from the previous cycle. Feedback for the inner stage is through simple change sharing of the output of FIR_1 with C_{ser}. In the subsequent conversion, the voltage on the top plate of C_{ser} (V_A) is naturally equal to the voltage on the bottom plate of C_{ser} (V_B), plus the voltage across C_{ser}(V_{ser})

$$V_A = V_B + V_{\text{ser}} = V_B + \alpha V_{\text{FIR1}} \tag{9}$$

where V_{FIR1} is the output of FIR_1 and α represents the loss due to charge sharing. In this way, a single capacitor C_{ser} implements the signal summation in Fig. 9, and this summation is entirely passive. Because the outer stage relaxes the noise requirements for the inner stage, C_{ser} can be a relatively small capacitance. The power and area overheads are therefore low.

A residue amplifier (RA) driving the input of each FIR filter compensates for the charge-sharing loss (α) and maintains the FIR coefficients. Cross-differential sampling, as in [12], provides an extra gain of 2, which relaxes the gain requirement of RAs and provides common-mode suppression (see Fig. 12). Charge-injection effect from the switches is negligible because of the fully differential operation and also because of the relatively large capacitance of FIR filters.

Unlike [3], the FIR filters in this work use ping-pong switching to realize two cycles of delay. C_{f2} and C_{f3} alternatively sample the output of RA1 (i.e., FB_1) and transfer their sampled charges to C_{ser} two cycles later, as shown in Fig. 13. Such an implementation simplifies the switching logic as there is only a single charge-sharing step in each conversion cycle.

FIR_2 operates in a similar way to FIR_1 and injects its output to the CDAC by charge sharing. As mentioned in [3], this charge sharing inevitably attenuates the sampled input voltage on CDAC and thus reduces the overall SNR. A high RA gain is required to entirely mitigate the attenuation, but this increases the design complexity and sensitivity. Thus, we choose an RA of around 10×, leading to a tolerable SNR degradation of 1.5 dB (16%).

As mentioned, an advantage of the cascaded architecture is that it shapes the noise of the inner loop. This greatly relaxes the noise requirements for RA1, allowing it to be a simple low-power *gm-R* amplifier (see Fig. 14). However, the noise of RA2 remains critical because its noise is not shaped and dominates the noise of the overall ADC. To solve this problem, we propose a *gm-R* amplifier with two-phase operation (discussed in Section V) to suppress noise and improve efficiency.

[1] [12] proposes a serial capacitor for residue summation in a conventional NS SAR.

Authorized licensed use limited to: University of Michigan Library. Downloaded on December 02,2020 at 03:43:06 UTC from IEEE Xplore. Restrictions apply.

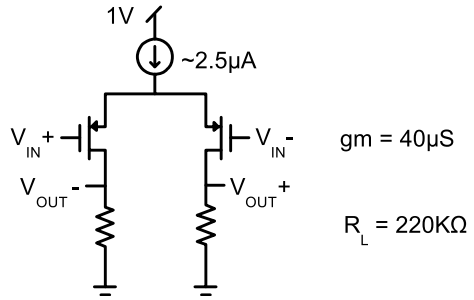

Fig. 14. Schematic of RA1.

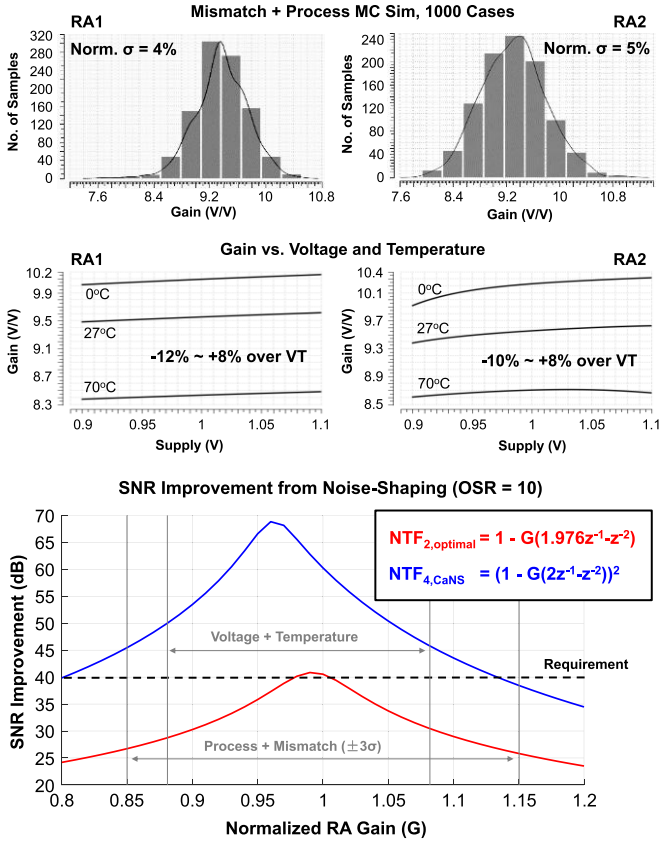

Fig. 15. RA gain variation (top) and the effect on NTF (bottom).

The system-level robustness of CaNS tolerates large gain variation from the open-loop RAs. With the simulated 1-sigma gain variation of 5%, the simulated SNR of the ADC is 90-dB SNR with >95% yield. Fig. 15 shows the simulated gain variation of the RAs under PVT variation and mismatch. The figure also shows the effect on the overall ADC.

B. Operation Details

Conversion occurs in four steps, as shown in Fig. 16. The overall timing is simple and little more complex than in a conventional SAR ADC.

In the first step (P1), CDAC samples the input signal. At the same time, the series capacitor C_{ser} discharges (reset). Feedback occurs in the second step (P2). The FIR filters inject their outputs onto C_{ser} and CDAC by charge sharing. The

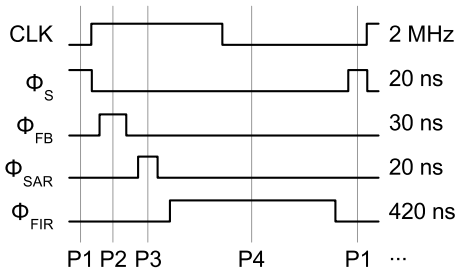

Fig. 16. Operation timing.

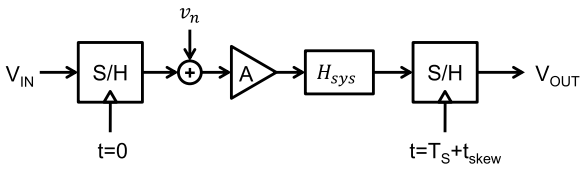

Fig. 17. Generalized signal model of DT amplifier.

third step (P3) proceeds in the same way as conversion in a conventional SAR ADC.

This operation tolerates linear parasitic capacitance at the plates of C_{ser} and C_{f1-6} because these capacitances only cause a linear gain error, and CaNS SAR is insensitive to gain error. However, any nonlinear parasitic capacitance on nodes A and B, such as from the input transistors of the RAs, causes distortion and degrades SNDR. To reduce this distortion, we adopt parasitic pre-charging [13] and reset nodes A and B to V_{CM} during P1. After P1, the parasitic capacitances at A and B share some of the charge from CDAC and C_{ser}. However, since V_A and V_B converge to virtual ground during SAR conversion, the charge shared by these two parasitic capacitors eventually returns, mostly eliminating the nonlinear error.

The fourth and final step (P4) is residue sampling. In this step, the two RAs amplify the residues on CDAC and the top plate of C_{ser}. After that, the two FIR filters sample the amplified outputs using the cross-differential connection for an additional gain of 2.

V. Multi-Phase Settling Amplifier

We propose a multi-phase settling scheme to improve RA efficiency without sacrificing robustness. Although some fully passive NS SAR ADCs are reported, most cannot provide enough loop gain for strong NS. In a high-resolution NS SAR, the active amplifier is usually the dominant noise source and easily becomes a performance bottleneck.

The RA in NS SAR ADCs operates in DT. Fig. 17 shows a generalized signal model for a DT amplifier.

Here, A is the nominal gain of the amplifier, and H_{sys} is a linear system that models the settling behavior. A CT white noise source, $v_n(t)$, models the additive noise of the amplifier. In most cases, the amplifier transconductance dominates v_n and determines the amplifier power consumption. T_S and t_{skew} are the sampling period and timing skew, respectively. Two critical specifications of a DT amplifier, the relative gain variation (g) and input referred noise ($v_{n,i}$), can be derived

Authorized licensed use limited to: University of Michigan Library. Downloaded on December 02,2020 at 03:43:06 UTC from IEEE Xplore. Restrictions apply.

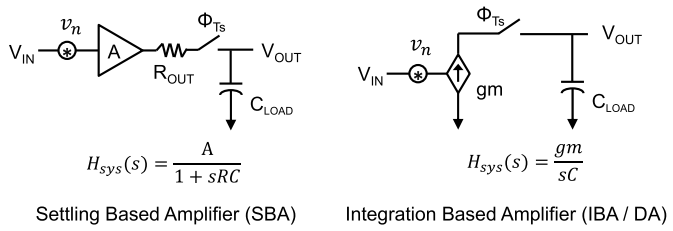

Fig. 18. Conventional DT amplifiers.

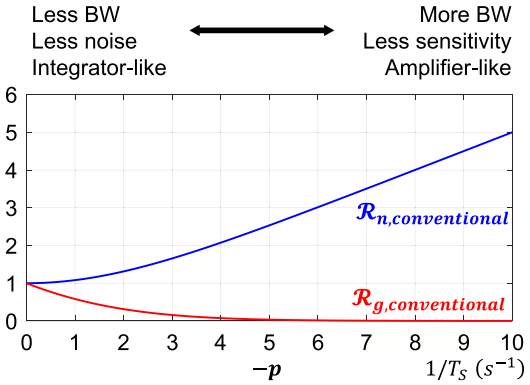

Fig. 19. Noise–robustness tradeoff for a conventional DT amplifier.

from the model

$$g = \frac{a(T_S + t_{\text{skew}})}{a(T_S)} \tag{10}$$

$$v_{n,i} = \frac{\int_0^{T_S} v_n(t)h(T_S - t)dt}{a(T_S)} \tag{11}$$

where $h(t)$ and $a(t)$ are the impulse and step response of H_{sys}, respectively.

A. Conventional DT Amplifiers

Conventional DT amplifiers can be classified into two types: settling-based amplifiers (SBAs) and integration-based amplifiers (IBAs). IBAs are also known as DAs.[2] Fig. 18 shows the two types and also provides the corresponding H_{sys}.

Although the two types of amplifier appear to be very different, and $H_{\text{sys}}$for both is a time-invariant, single-pole system, i.e., $H_{\text{sys}}(s) = (K/s - p)$. We define two metrics, R_n and R_g, to measure the noise performance and gain-timing sensitivity, respectively,

$$\mathcal{R}_n \triangleq \frac{\text{noise of DT amp.}}{\text{noise of IBA}} = \frac{v_{n,i}^2}{\left(\frac{v_n^2}{\Delta f}\cdot\frac{0.5}{T_S}\right)} = \frac{1}{2}pT_S\cdot\frac{e^{pT_S}+1}{e^{pT_S}-1} \tag{12}$$

$$\mathcal{R}_g \triangleq \frac{\text{sensitivity of DT amp.}}{\text{sensitivity of IBA}} = \frac{\mathrm{d}(g)}{\mathrm{d}\left(\frac{t_{\text{skew}}}{T_S}\right)} = pT_S\cdot\frac{e^{pT_S}}{e^{pT_S}-1} \tag{13}$$

where $p < 0$ for LHP pole. Physically, R_n compares the input-referred noise of a DT amplifier to an IBA, and R_g compares the gain-timing sensitivity of a DT amplifier to an IBA.

Fig. 19 plots the two metrics as a function of p for a DT amplifier. We see that there is a tradeoff between R_n and R_g,

[2]"Dynamic amplifier" refers to open-loop gm-C amplifiers. Closed-loop dynamic amplifiers, such as [4], are essentially SBAs with variable bandwidth.

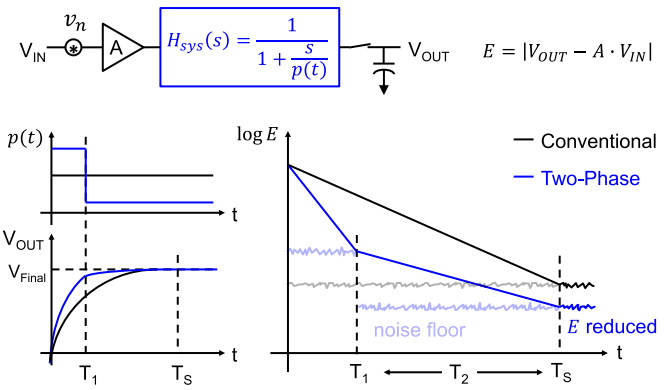

Fig. 20. Amplification progress (step response) of two-phase settling amplifier.

which means that we cannot simultaneously improve both noise and robustness by changing the pole of H_{sys}.

B. DT Amplifier With Multi-Phase Settling

We propose a time-variant H_{sys} to break the noise–robustness tradeoff of conventional DT amplifiers. In the proposed multi-phase settling amplifier, H_{sys} is still a single-pole system, but we change the pole location in different phases. As an example, Fig. 20 shows the amplification progress for a two-phase settling amplifier.

Here, H_{sys} has a large bandwidth in the first phase but also induces more noise. During the second phase, the bandwidth is reduced by suppressing noise. Intuitively, since the bandwidth of the second phase is smaller than with a conventional SBA, the overall noise is reduced. An essential advantage is that gain-timing sensitivity is much lower than a DA. The two metrics of a two-phase settling amplifier (i.e., $R_{n,2P}$ and $R_{g,2P}$) are

$$\mathcal{R}_{n,2P} = \frac{1}{2}T_S\cdot\frac{-p_1\left(1-e^{2p_1T_1}\right)\cdot e^{2p_2T_2} - p_2\left(1-e^{2p_2T_2}\right)}{\left(1-e^{(p_1T_1+p_2T_2)}\right)^2} \tag{14}$$

$$\mathcal{R}_{g,2P} = -(p_1T_1 + p_2T_2)\frac{e^{(p_1T_1+p_2T_2)}}{1-e^{(p_1T_1+p_2T_2)}}. \tag{15}$$

Fig. 21 plots these metrics versus phase division ratio, which supports the conclusion that two-phase settling can improve both noise efficiency and gain-timing robustness.

In the figure, the x-axis is the fraction of $\mathrm{T_S}$ that the amplifier operates in phase 1 (i.e., $\mathrm{T_1}$). The pole locations are calculated by minimizing $R_{n,2P} + R_{g,2P}$ for each value of $\mathrm{T_1}$. When compared to a conventional SBA with 6τ settling, two-phase settling reduces noise (R_n) by about 60%. This implies that 60% less power on gm transistors is required to achieve the same noise level. Although the noise with two-phase settling (and optimal phase division) is still a little higher (18%) than with a DA, the gain sensitivity (R_g) is 9× smaller. In a practical design, different weightings can be applied to $R_{n,2P}$ and $R_{g,2P}$ to emphasize noise or sensitivity depending on the application.

Adding more settling phases can further reduce noise and gain sensitivity, as shown in Fig. 22. With enough phases,

Authorized licensed use limited to: University of Michigan Library. Downloaded on December 02,2020 at 03:43:06 UTC from IEEE Xplore. Restrictions apply.

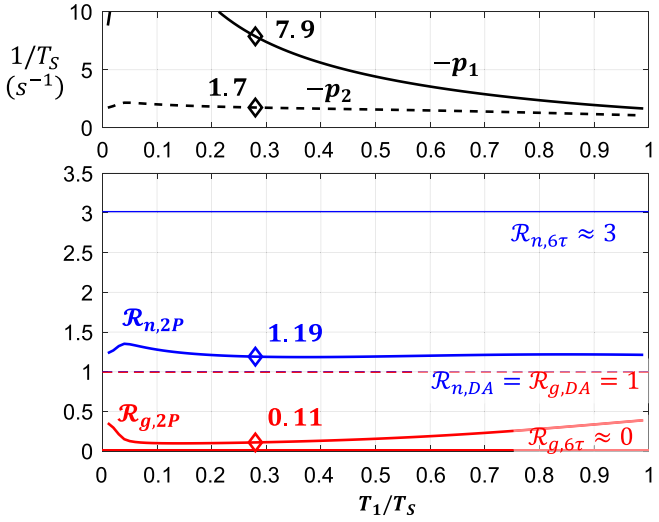

Fig. 21. Optimal pole locations (top) and metrics (bottom) of two-phase settling amplifier versus phase-division ratio. Diamonds mark the optimal phase division in the sense of minimizing $R_{n,2P} + R_{g,2P}$ globally.

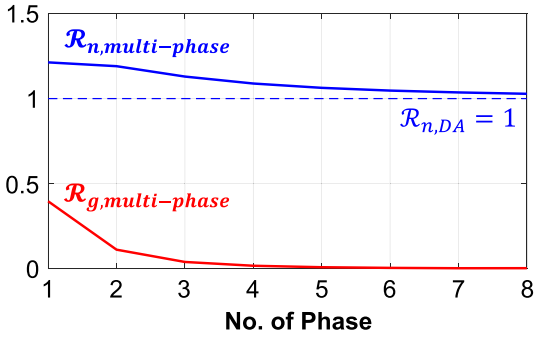

Fig. 22. Theoretical (optimal) performance versus number of settling phases. This calculated by optimizing $R_{n,m} + R_{g,m}$.

the theoretical noise approaches that of a DA, while the gain robustness remains as good as a conventional SBA.

C. Practical Residue Amplifier Design

Two-phase settling is the most practical choice among multi-phase designs, as it provides good performance with a negligible increase in complexity. In our prototype, RA2 is a *gm-R* structure with push–pull operation to double the transconductance and improve efficiency. Fig. 23 shows a schematic of RA2. The CMFB resistors (R_L) are the dominant resistive load. Cascoding reduces the influence of channel modulation on gain and linearity. The output resistance is configured by shorting the output series resistors (R_O). Thus, the main pole location can be changed during settling. The noise of R_O is suppressed by the gain of RA2 and is thus negligible.

To verify the effectiveness of two-phase settling, Table I compares the simulated noise performance of RA2 for different settling configurations. The simulations are for the same RA2 design and differ only in R_O and the switch operation. In the conventional settling case, an external R_O is added to satisfy 6-τ settling. The simulations show that two-phase

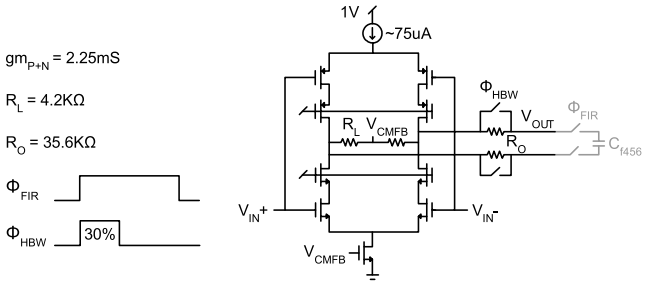

Fig. 23. Schematic of RA2.

TABLE I
NOISE PERFORMANCE OF RA2

		Conventional	Two-Phase	
			P1	P2
gm		2.25 mS		
R_L		4.2 KΩ		
C_L		2.88 pF		
R_O		7 KΩ [+]	shorted	35.6 KΩ
T_S		420 ns	120 ns	300 ns
main pole (p) [++]		2.2 MHz	6.6 MHz	0.7 MHz
time constant (τ) [++]		71 ns	28 ns	230 ns
$v_{n,in}^2$ [+++]	gm noise only	$(15.0\ \mu V)^2$	$(10.2\ \mu V)^2$ **[54% reduction]**	
	all noise enabled	$(17.6\ \mu V)^2$	$(14.4\ \mu V)^2$ **[33% reduction]**	

[+] R_O is added to satisfy 6-τ settling
[++] from post-layout AC simulation
[+++] statistical result from post-layout transient simulation with noise (1000 cases)

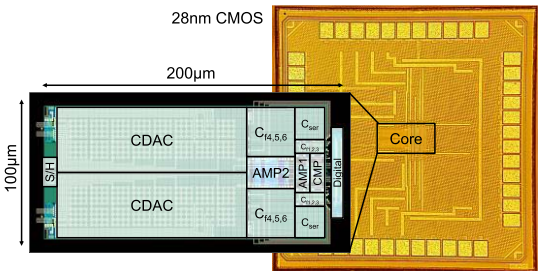

Fig. 24. Die photograph.

settling reduces noise by 33%. The discrepancy between the actual and theoretical improvements is due to other noise sources besides the *gm* transistors. When only the noise of *gm* transistors is considered, the simulated noise reduction is 54%, which is very close to the theoretical optimum. In this design, the pole locations are not optimal, so some discrepancy still exists.

VI. MEASUREMENTS

The prototype design is fabricated in 28-nm CMOS and measures 100 μm × 200 μm (see Fig. 24). The majority of the chip area is occupied by the CDAC, while the NS FIR filters account for only 21% of the total area.

In single-tone testing with 19.3-kHz full-scale input signal (1.05-Vp differential), the measured peak SNDR over a

Authorized licensed use limited to: University of Michigan Library. Downloaded on December 02,2020 at 03:43:06 UTC from IEEE Xplore. Restrictions apply.

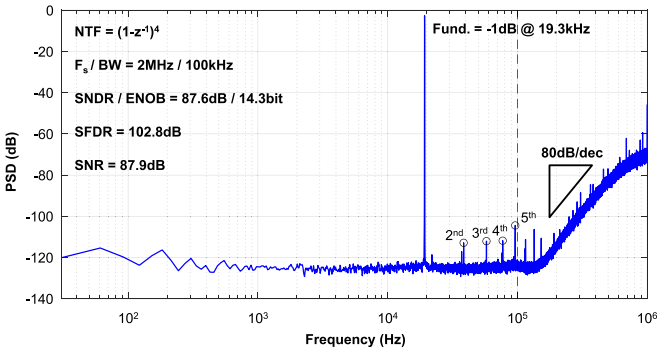

Fig. 25. FFT for single-tone test (64k samples Hann window, 16× averaging).

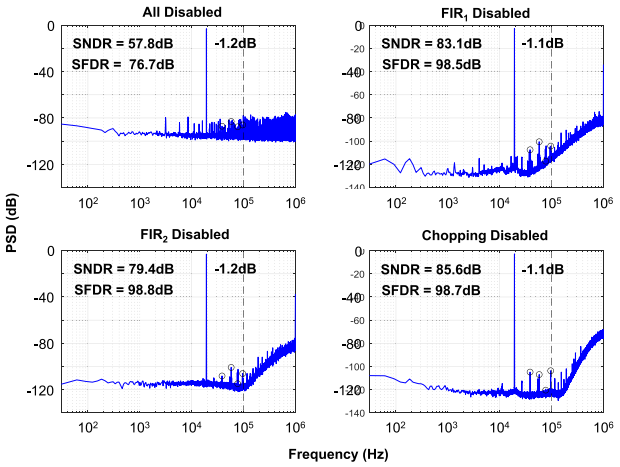

Fig. 26. Single-tone tests for different configurations.

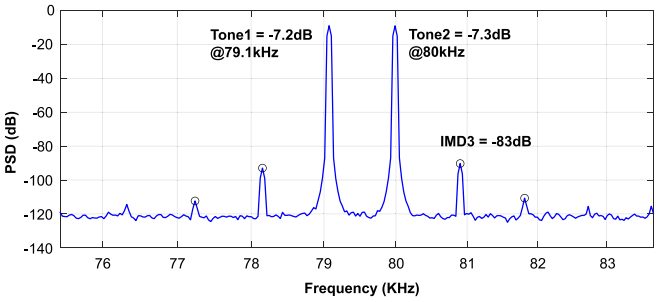

Fig. 27. Two-tone measurement test.

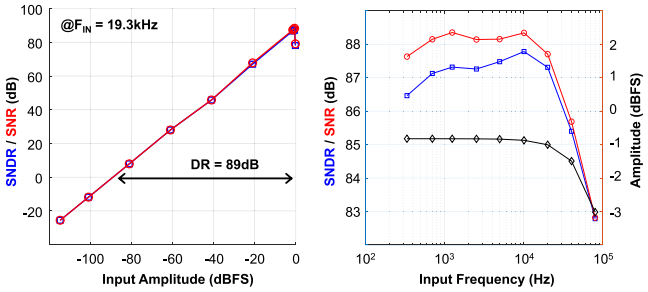

Fig. 28. Measured performance versus input amplitude and frequency.

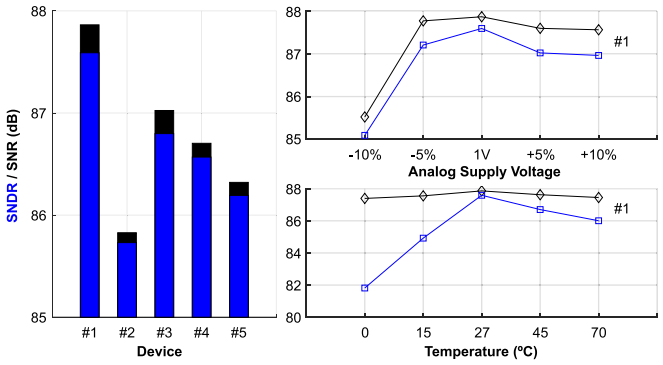

Fig. 29. PVT measurement results.

100-kHz bandwidth is 87.6 dB. A fourth-order-shaped noise floor with an 80 dB per decade slope is evident in the output spectrum, as shown in Fig. 25.

For comparison, we perform the same test with different configurations (see Fig. 26). SNDR improves by 25.3 dB when the outer loop (FIR2) is enabled. The inner loop (FIR1) provides an additional 4.5-dB SNDR improvement. The mild SNDR improvement from the inner loop is due to a conservative design strategy that makes the shaped quantization error much smaller than the thermal noise. Therefore, there is a large margin for NTF variation so that quantization error does not overwhelm thermal noise. However, a more aggressive design strategy with a lower OSR and quantizer resolution can achieve the same SNR but with less NTF margin. The low-cost increased NS order provided by CaNS SAR architecture gives the designer extra freedom and can either improve performance or robustness.

Fig. 27 shows the measured spectrum for a two-tone test. The measured IMD3 is −83 dB for a near-maximum input frequency. Fig. 28 shows the measured performance for different input amplitudes and frequencies. These measurements indicate consistent performance over the entire input frequency range. The measured dynamic range is 89 dB.

We measured five different devices to demonstrate the PVT robustness of the new architecture. Without any PVT calibration, the measured SNR variation across the devices is only 2 dB. As shown in Fig. 29, the measured variation in SNR is within 3 dB over ±10% change in analog supply voltage and a 0 °C–70 °C temperature range. The degradation of SNDR at low temperature is likely due to variation in the on-chip IC delays.

Fig. 30 shows a breakdown of the measured power and area. The ADC consumes 120 μW at 2 MS/s. Only 2.2% of power and 6% of area are taken by the inner NS loop, which contributes <1% of the total noise. Therefore, the cost of the increased order is negligible.

Finally, Table II compares this work with some other state-of-the-art sub-MHz ADCs. The prototype exhibits higher order NS than conventional NS SAR ADCs and also delivers the highest SNR over 100-kHz bandwidth. The overall efficiency, as measured with the Schreier FoM, is equivalent to that of the most efficient conventional NS SAR ADCs, but our implementation is free of DAs and is PVT stable on system

Authorized licensed use limited to: University of Michigan Library. Downloaded on December 02,2020 at 03:43:06 UTC from IEEE Xplore. Restrictions apply.

TABLE II
COMPARISON TABLE

	This Work [6]	X. Tang [4]	J. Liu [8]	S. Li [3]	W. Guo [2]	ISSCC 2018 P. Vogelmann	VLSI 2018 C. Lee
Architecture	**CaNS-SAR**	NS-SAR	NS-SAR	NS-SAR	NS-SAR	DT-SD	CT-SD
NTF Order	**4**	2	2	2	2	3	3
Amplifier	**2-Phase Settling**	Dynamic, Closed-Loop	Passive	Dynamic	Passive	Op-Amp	Op-Amp
Process (nm)	**28**	40	40	40	40	180	65
Area (mm^2) [+]	**0.02**	0.037	0.06	0.024	0.04	0.363	0.14
Supply (V)	**1**	1.1	1.1	1.1	1.1	3	1.2
Power (μW) [+]	**120**	107	67	84	143	1100	68
Fs (MHz)	**2**	10	2	10	8.4	30	6.14
OSR	**10**	8	25	8	16	150	128
BW (KHz)	**100**	625	40	625	263	100	24
SNDR (dB)	**87.6**[++]	83.8[++]	90.5	79[++]	80	86.6	94.1
SFDR (dB)	**102.8**[++]	94.3[++]	102.2	89[++]	-	101.3	107
DR (dB)	**89**	85.5	94.3	80.5	-	91.5	98.2
FoM_S (dB)	**176.8**	181.5	178.2	177.7	172.6	166.2	179.6
FoM_{NSSAR} (dB) [+++]	**135.7**	135.3	133.5	131.9	127.3	117.7	N/A

[+]Excludes power and area of CDAC calibration
[++]With CDAC mismatch calibration
[+++]Using SNDR in place of SNR_{worst} due to insufficient information

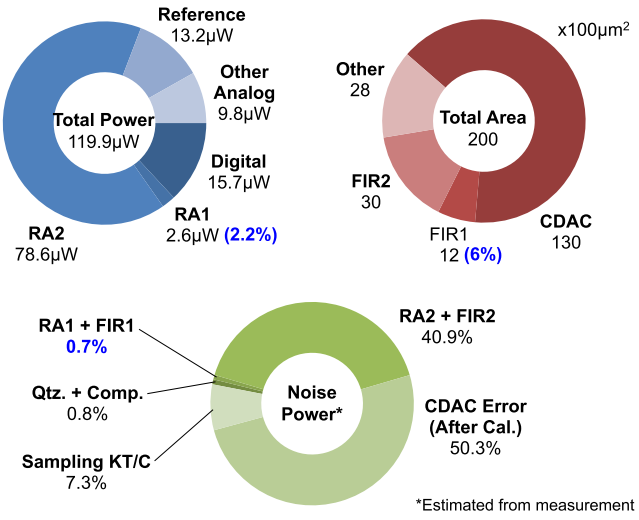

Fig. 30. Power, area, and noise (estimated) breakdown.

level. Compared with SD ADCs, the prototype is more than 7× smaller in area and thus is much lower in cost.

VII. CONCLUSION

The work proposes a new cascaded EF architecture for NS SAR ADC. The architecture provides extra NTF order for NS SAR at negligible cost. A two-phase settling technique is also proposed to boost the efficiency of DT amplifier without compromising PVT robustness. The prototype CaNS SAR ADC demonstrates the highest NTF order and highest SNDR among NS SAR ADCs over 100-kHz bandwidth and provides a low-cost solution for high-resolution sub-MHz analog-to-digital conversion.

APPENDIX I
NS SAR MODELING ASSUMPTIONS

The NTFs for the direct and cascade forms are

$$\mathrm{NTF}_{\mathrm{direct}} = \left(1-z^{-1}\right)^n = 1+\sum_{k=1}^{n} a_{n,k} z^{-k} \tag{A1}$$

$$\begin{aligned}\mathrm{NTF}_{\mathrm{cascade}} &= \left(1-z^{-1}\right)^{\lfloor \frac{n}{2} \rfloor} \cdot \left(1-z^{-1}\right)^{\lceil \frac{n}{2} \rceil} \\ &= \left(1+\sum_{k=1}^{\lfloor \frac{n}{2} \rfloor} a_{\lfloor \frac{n}{2} \rfloor,k} z^{-k}\right)\left(1+\sum_{k=1}^{\lceil \frac{n}{2} \rceil} a_{\lceil \frac{n}{2} \rceil,k} z^{-k}\right)\end{aligned} \tag{A2}$$

where n is the order of NTF and $a_{n,k}$ are the binomial coefficients with variation, i.e.,

$$a_{n,k} = (-1)^k \cdot \binom{n}{k} + N\left(0, \sigma_{n,k}^2\right). \tag{A3}$$

SNR is evaluated as

$$\mathrm{SNR} = \frac{K_1}{\frac{E_S^2}{\mathrm{OSR}} + \frac{E_Q^2}{\pi}\int_0^{\frac{\pi}{\mathrm{OSR}}} |\mathrm{NTF}(jw)|^2 dw + \frac{E_N^2}{\pi}\int_0^{\frac{\pi}{\mathrm{OSR}}} |1-\mathrm{NTF}(jw)|^2 dw} \tag{A4}$$

where K_1 is a constant related to the reference voltage. CDAC mismatch is ignored in this model, i.e., $E_D = 0$. The worst case SNR, i.e., $\mathrm{SNR}_{\mathrm{worst}}$, is calculated by

$$\mathrm{P}(\mathrm{SNR} > \mathrm{SNR}_{\mathrm{worst}}) = \mathrm{yield} \tag{A5}$$

Authorized licensed use limited to: University of Michigan Library. Downloaded on December 02,2020 at 03:43:06 UTC from IEEE Xplore. Restrictions apply.

based on the Monte Carlo method and distribution fitting. Power is the core power plus filter power

$$P = P_{\text{core}} + P_{\text{filter}} = \text{BW} \cdot \text{OSR}\left(\frac{K_2}{\sqrt{E_Q^2}} + \frac{K_3}{E_N^2}\right) \quad \text{(A6)}$$

where K_2 and K_3 are related to FoM_W and the process.

Area is evaluated as the CDAC area plus filter area

$$A = A_{\text{CDAC}} + A_{\text{filter}} = \frac{K_4}{E_S^2}(1 + K_5) \quad \text{(A7)}$$

where K_4 and K_5 are related to capacitance density and the ratio between CDAC and filter caps.

Finally, the variation of NTF coefficients is related to the area of filter cap

$$\sigma_{n,k}^2 = K_6^2 \cdot \frac{2^n}{A_{\text{filter}}} \cdot \left|a_{n,k}^-\right| \quad \text{(A8)}$$

where K_6^2 is the variance of a unit area of capacitance and $(2^n/A_{\text{filter}})$ is the reciprocal of FIR filter unit capacitor's area (2^n is the sum of all FIR coefficients).

The results in Fig. 4 are from solving an optimization problem

$$\begin{aligned}
&\text{maximize } \text{FoM}_{\text{NSSAR}} \\
&\text{variable } \{E_Q, E_S, E_N, \text{OSR}\} \\
&\text{subject to } \text{SNR}_{\text{worst}} = 90 \text{ (dB)} \\
&\qquad \frac{2^{-4}}{\sqrt{12}} \le E_Q \le \frac{2^{-11}}{\sqrt{12}} \text{ (V)} \\
&\qquad 10^{-5} \le E_S, E_N \le 10^{-2} \text{ (V)} \\
&\qquad 4 \le \text{OSR} \le 512
\end{aligned}$$

with the following presets:

$$\begin{aligned}
&K_1 = 0.125, \quad K_2 = 2.9 \times 10^{-14}, \quad K_3 = 1.3 \times 10^{-20} \\
&K_4 = 1 \times 10^{-11}, \quad K_5 = 0.1, \quad K_6 = 2.5\% (\text{per } \mu\text{m}^2) \\
&\text{BW} = 100 \text{ K}, \quad \text{yield} = 95\%
\end{aligned}$$

where K_{1-6} are based on process data and information from the ADC survey. Since the objective function is stochastic, the optimization is done by first running the Surrogate Algorithm on the full parameter space, followed by running a localized pattern search algorithm. The optimization is repeated ten times and the result with minimal OSR is picked as the final result.

APPENDIX II
STATIC ERROR CALIBRATION OF NS SAR

We perform a foreground calibration to reduce static errors (i.e., mostly CDAC mismatch, E_D) in our NS SAR design. The calibration system consists of a digital low-pass filter and a lookup table (LUT). It reads the digital output from the NS SAR and outputs a calibrated in-band signal. Fig. 31 shows the signal diagram of the calibration system.

A low-pass filter first filters the ADC output (i.e., Calibration In). The filter bandwidth matches the bandwidth of ADC and provides enough attenuation so that out-of-band quantization errors become negligible. The 16-bit truncated

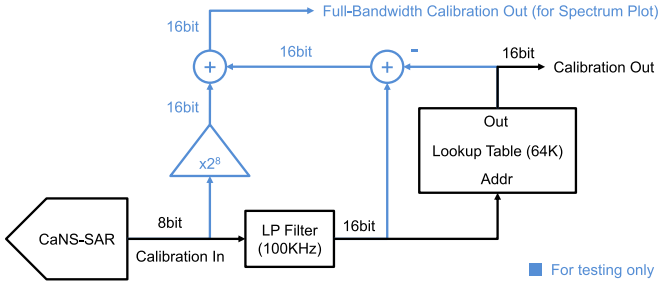

Fig. 31. Calibration system applied.

TABLE III
ESTIMATED POWER AND AREA COST OF CALIBRATION

	Filter (IIR – 4$^{\text{th}}$)	LUT (64K x 16bit)
Power @ 2MHz	3 μW	24 μW
Area	< 0.001 mm^2	0.22 mm^2

outputs of the filter provide the address input to the LUT. The LUT values, which are generated by an optimization algorithm (e.g., LMS adaptation), cancel static nonlinear errors of the ADC by simply mapping an inverse function to the error. The LUT generation process needs only run once for each device and can then be applied for any input signal and PVT condition. The reason for low-pass filtering first is that the LUT can mix down high-frequency errors back in-band and degrade SNR. Adding a filter prevents this effect.

The calibration method used in this work is for testing and is implemented off-chip. The method is not optimized for power and area in the sense of an on-chip implementation. Thus, we do not include the power and area cost of calibration in Section VI. However, for readers' reference, Table III provides the estimates of the power and area of the calibration circuitry from logic synthesis and APR tools for a 28-nm CMOS process.

REFERENCES

[1] J. A. Fredenburg and M. P. Flynn, "A 90-MS/s 11-MHz-bandwidth 62-dB SNDR noise-shaping SAR ADC," *IEEE J. Solid-State Circuits*, vol. 47, no. 12, pp. 2898–2904, Dec. 2012.

[2] W. Guo, H. Zhuang, and N. Sun, "A 13b-ENOB 173dB-FoM 2nd-order NS SAR ADC with passive integrators," in *Proc. Symp. VLSI Circuits*, Jun. 2017, pp. C236–C237.

[3] S. Li, B. Qiao, M. Gandara, D. Z. Pan, and N. Sun, "A 13-ENOB second-order noise-shaping SAR ADC realizing optimized NTF zeros using the error-feedback structure," *IEEE J. Solid-State Circuits*, vol. 53, no. 12, pp. 3484–3496, Dec. 2018.

[4] X. Tang *et al.*, "9.5 a 13.5b-ENOB second-order noise-shaping SAR with PVT-robust closed-loop dynamic amplifier," in *IEEE ISSCC Dig. Tech. Papers*, Feb. 2020, pp. 162–164.

[5] B. Murmann. *ADC Performance Survey 1997–2020*. Accessed: May 7, 2020. [Online]. Available: http://web.stanford.edu/~murmann/adcsurvey.html

[6] L. Jie, B. Zheng, H.-W. Chen, R. Wang, and M. P. Flynn, "9.4 a 4th-order cascaded-noise-shaping SAR ADC with 88dB SNDR over 100 kHz bandwidth," in *IEEE ISSCC Dig. Tech. Papers*, Feb. 2020, pp. 160–162.

[7] J. Sauerbrey, T. Tille, D. Schmitt-Landsiedel, and R. Thewes, "A 0.7-V MOSFET-only switched-opamp /spl Sigma//spl Delta/ modulator in standard digital CMOS technology," *IEEE J. Solid-State Circuits*, vol. 37, no. 12, pp. 1662–1669, Dec. 2002.

Authorized licensed use limited to: University of Michigan Library. Downloaded on December 02,2020 at 03:43:06 UTC from IEEE Xplore. Restrictions apply.

[8] J. Liu, X. Wang, Z. Gao, M. Zhan, X. Tang, and N. Sun, "9.3 a 40 kHz-BW 90dB-SNDR noise-shaping SAR with 4× passive gain and 2nd-order mismatch error shaping," in *IEEE ISSCC Dig. Tech. Papers*, Feb. 2020, pp. 158–160.
[9] J. G. Proakis and D. G. Manolakis, "Analysis of sensitivity to quantization of filter coefficients," in *Digital Signal Processing*, 3rd ed. Upper Saddle River, NJ, USA: Prentice-Hall, 1996, pp. 569–578.
[10] T. Kim, C. Han, and N. Maghari, "28.2 an 11.4 mW 80.4dB-SNDR 15MHz-BW CT delta-sigma modulator using 6b double-noise-shaped quantizer," in *IEEE ISSCC Dig. Tech. Papers*, Feb. 2017, pp. 468–469.
[11] T.-Y. Lo, C.-H. Weng, H.-Y. Hsieh, Y.-S. Shu, and P.-C. Chiu, "20.4 an 8×—OSR 25MHz-BW 79.4dB/74dB DR/SNDR CT $\Delta\sigma$ modulator using 7b linearized segmented DACs with digital noise-coupling-compensation filter in 7nm FinFET CMOS," in *IEEE ISSCC Dig. Tech. Papers*, Feb. 2019, pp. 334–336.
[12] Y.-Z. Lin, C.-Y. Lin, S.-C. Tsou, C.-H. Tsai, and C.-H. Lu, "20.2 a 40MHz-BW 320MS/s passive noise-shaping SAR ADC with passive signal-residue summation in 14nm FinFET," in *IEEE ISSCC Dig. Tech. Papers*, Feb. 2019, pp. 330–332.
[13] L. Jie, B. Zheng, and M. P. Flynn, "A calibration-free time-interleaved fourth-order noise-shaping SAR ADC," *IEEE J. Solid-State Circuits*, vol. 54, no. 12, pp. 3386–3395, Dec. 2019.

Lu Jie (Member, IEEE) was born in China, in 1995. He received the B.Eng. degree in electrical and electronic engineering from Zhejiang University, Hangzhou, China, in 2017. He is currently pursuing the Ph.D. degree with the University of Michigan, Ann Arbor, MI, USA, with a focus on hybrid-architecture ADC design.

Boyi Zheng (Member, IEEE) received the B.S. degree in microelectronics from Shanghai Jiao Tong University, Shanghai, China, in 2016, and the M.S. degree in electrical and computer engineering from the University of Michigan, Ann Arbor, MI, USA, in 2018, where she is currently pursuing the Ph.D. degree.

Her research interests include digital intensive communication systems, as well as digital direct to RF and beamforming techniques.

Hsiang-Wen Chen (Member, IEEE) received the B.S. degree in electrical engineering from National Taiwan University, Taipei, Taiwan, in 2016, and the M.S. degree in electrical and computer engineering from the University of Michigan, Ann Arbor, MI, USA, in 2019, where he is currently pursuing the Ph.D. degree.

His research interests include analog/mixed-signal circuit design, such as filters, data converters, and wireline communication.

Michael P. Flynn (Fellow, IEEE) received the Ph.D. degree from Carnegie Mellon University, Pittsburgh, PA, USA, in 1995.

From 1995 to 1997, he was a Member of Technical Staff with Texas Instruments, Dallas, TX, USA. From 1997 to 2001, he was with Parthus Technologies, Cork, Ireland. In 2001, he joined the University of Michigan, Ann Arbor, MI, USA, where he is currently a Professor. His technical interests are in RF circuits, data conversion, serial transceivers, and biomedical systems.

Dr. Flynn is a 2008 Guggenheim Fellow. He received the NSF Early Career Award in 2004, the 2016 University of Michigan Faculty Achievement, the 2011 Education Excellence Award and the 2010 College of Engineering Ted Kennedy Family Team Excellence Award from the College from Engineering at the University of Michigan, and the 2005–2006 Outstanding Achievement Award from the Department of Electrical Engineering and Computer Science, University of Michigan. He is the Chair of the Data Conversion Committee of the International Solid-State Circuits Conference. He formerly served on the Technical Program Committees of ESSCIRC, A-SSCC, and the Symposium on VLSI Circuits. He was the Editor-in-Chief of the IEEE JOURNAL OF SOLID-STATE CIRCUITS(JSSC) from 2013 to 2016. He is a former Distinguished Lecturer of the IEEE Solid-State Circuits Society. He has served as an Associate Editor for the IEEE JSSC and of the IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS.

Authorized licensed use limited to: University of Michigan Library. Downloaded on December 02,2020 at 03:43:06 UTC from IEEE Xplore. Restrictions apply.