9.4 A 4th-Order Cascaded-Noise-Shaping SAR ADC with 88dB SNDR Over 100kHz Bandwidth

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High-resolution, sub-MHz-bandwidth data converters are essential for audio and sensor applications and are conventionally implemented as sigma-delta (SD) converters. The dependence of SD ADCs on op-amps inherently results in difficulties for process scaling, power efficiency improvement, and area reduction. A promising alternative to SD ADCs is the emerging noise-shaping (NS) SAR ADC, which provides high resolution with high energy efficiency and compactness. For medium-high SNR applications, some NS-SAR ADCs already exhibit better performance than SD ADCs [1-2]. However, NS-SARs for applications that require SNR >85 dB and hundreds of kHz of bandwidth are currently lacking. The SNR is limited because most recent NS-SAR ADCs are restricted to a low-order NTF. Additionally, noise from the loop filter limits performance. In this work, we propose a cascaded-noise-shaping (CaNS) SAR architecture that cascades two 2nd-order NS stages to provide a 4th-order NTF for high resolution, while consuming similar power and area to a 2nd-order NS-SAR. Our prototype achieves 88dB SNDR over a 100kHz bandwidth while consuming only 120µW and occupies 0.02mm^2, resulting in a Schreier FoM of 177dB. The proposed architecture enables the NS-SAR to be used in low-power, area-critical audio applications in place of SD ADCs.

Realizing an aggressive NTF in an NS-SAR is challenging. For conventional NS-SARs, the choice is either a power-hungry active integrator for a sharp NTF, or a passive IIR filter that is limited to a mild NTF. Some recent works use the error-feedback (EF) structure for a sharper NTF without an op-amp [2]. Nevertheless, the difficulty of implementing an EF-NS-SAR increases dramatically as the NTF order increases because the coefficients of the FIR filter become larger and more sensitive to variation. Furthermore, it is hard for the delay cells in a high-order FIR filter to precisely hold the analog value for multiple sampling cycles. For these reasons, NS-SAR ADCs rarely achieve an NTF order higher than 3, which is common for SD ADCs.

To solve these challenges, we propose a novel NS SAR architecture that cascades two low-order NS stages to create a high-order NTF (Fig. 9.4.1). The first stage is implemented by the inner EF loop with filter FIR1, while the second stage is constructed by an outer EF loop around the first stage with filter FIR2. The quantization noise, Q, including any noise from the comparator, is shaped by both the first and second stages, resulting in a high-order overall NTF. Besides the increase in the NTF order, there are three other important advantages to this new approach: 1) the zeros of the overall NTF are independently controlled by the two sub-NTFs (NTF1,2), and thus 2) the NTF is much less sensitive to the variation in the coefficients. (Figure 9.4.1 shows the theoretical SNR distribution under coefficients variation for both the cascaded NTF and a conventional one, which shows improvement in robustness.) Moreover, 3) the noise from FIR1 (n_{FIR1}) can also be shaped by the second stage, which greatly eases the implementation of the first stage, and thus the overall area and power cost of this architecture is comparable to a single-stage EF-NS-SAR.

In our prototype CaNS-SAR design (Fig. 9.4.2), a passive filter, FIR1, along with a serial capacitor (C_b) for feedback summation [3] implements the EF of the first NS stage. After each SAR conversion, FIR1 samples the residue at the comparator input through a low gain amplifier (AMP1) and provides the appropriate delay. The two-sample delay (z^{-2}) is simply realized by a ping-pong switching approach. Charge-sharing transfers the delayed sample from FIR1 to C_b, which is reset each cycle. The gain of AMP1 compensates for the attenuation of charge-sharing and enables the required overall transfer function of FIR1. Due to the series-voltage summation, the voltage on the bottom plate of C_b (V_X), after each SAR conversion, is equal to the residue shaped by the first stage ($V_X = Q \cdot NTF1$), which is exactly the required input for the FIR2. Thus, the second NS stage can simply be implemented with another similar EF structure, where FIR2 operates on the shaped residue (V_X) through another attenuation compensating amplifier, AMP2. CDAC charge-sharing summation [2] is adopted in the second stage EF, so that the capacitance of CDAC is reused to suppress the kT/C noise of FIR2, further improving compactness.

Although the power and area of NS ADCs are usually constrained by noise requirements, our prototype preserves high efficiency through both system-level and circuit-level innovations. Since the second stage also shapes the noise of the first stage, the noise requirement of FIR1 is greatly relaxed. This allows the capacitance in FIR1 to be small, and AMP1 can simply be a low-power differential pair (Fig. 9.4.3). AMP2 is the only noise-critical active block in the system, as its noise cannot be shaped. To improve power efficiency, we build AMP2 as a complementary differential g_m-R structure with cascode to improve linearity (Fig. 9.4.3). In addition, we actively manage the output resistance of AMP2 to optimize settling and noise. We reduce the output resistance of AMP2 at the beginning of each FIR sampling (ϕ_{HBW}) to enable fast settling, and increase the output resistance during the rest sampling to limit noise bandwidth, which reduces up to 47% settling error (Fig. 9.4.3). Furthermore, chopping in both amplifiers reduces flicker noise (Fig. 9.4.2).

PVT variation is another concern for high-performance ADCs. Unlike the dynamic amplifiers in [1-2], the AMP1,2 are static and much less sensitive to PVT variation. Although there is still a simulated ~±10% amplifier gain variation, this is fortunately common to all the FIR coefficients and results in less impact on the NS performance. The cascaded structure of the NTF further reduces the sensitivity to gain variation. As a result, the proposed design can tolerate a -20% to +15% amplifier gain variation, while still providing the required 40dB NS SNR improvement for a 90dB overall SNR (Fig. 9.4.3). Therefore, no calibration for PVT is required.

Many NS SARs are built with a SAR quantizer >=9b due to the limitations in their NTFs. Thanks to the higher NTF order, our prototype only needs an 8b (7.7pF) CDAC to achieve an SNR >85dB. The low core resolution eases the implementation of the SAR logic and CDAC routing, and also simplifies digital filtering and calibration. A one-time LMS-based foreground calibration generates a lookup table (off-chip) to cancel CDAC mismatch at the ADC output.

Fabricated in 28nm HPC+ CMOS, our prototype CaNS-SAR ADC occupies an active area of 0.02mm^2 and consumes 119.9µW power from a 1V supply at a 2MS/s sampling rate. Figure 9.4.4 shows the measured output spectrum, where a peak SNDR of 87.6dB can be observed with a 10× OSR, resulting in a Schreier FoM of 176.8dB. Figure 9.4.4 shows the spectrum for a two-tone input, as well as the ADC performance vs. input frequency. IMD3 is 83dB at high frequency. Figure 9.4.5 shows the measured SNDR vs. input amplitude, and indicates a DR of 89dB. Figure 9.4.5 also presents the power breakdown. To verify the PVT robustness, Fig. 9.4.5 gives the measured performance of 5 devices. The figure also shows measurements for different temperatures and supply voltages. An SNR change of only 2dB is observed between devices, over a 0~70°C temperature range and for a ±10% amplifier supply variation. Figure 9.4.7 shows the die photo.

Figure 9.4.6 compares this work to other state-of-the-art NS-SAR and SD ADCs, and clearly shows the advantage of CaNS-SAR in NTF order and overall performance. In conclusion, this work presents a novel CaNS-SAR architecture that enables a 4th-order NTF and excellent SNR performance in single-channel NS-SAR ADCs, while preserving the energy efficiency of the SAR architecture. The proposed ADC is a more compact and energy efficient alternative to SD ADCs for audio and sensing applications that require high SNDR in sub-MHz bandwidth.

Acknowledgement:
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Reference:
[1] C. Liu and M. Huang, "A 0.46mW 5MHz-BW 79.7dB-SNDR Noise-Shaping SAR ADC with Dynamic-Amplifier-Based FIR-IIR Filter," *ISSCC*, pp. 466-467, Feb. 2017.
[2] S. Li et al., "A 13-ENOB 2nd-Order Noise-Shaping SAR ADC Realizing Optimized NTF Zeros Using an Error-Feedback Structure," *ISSCC*, pp. 234-236, Feb. 2018.
[3] Y. Lin et al., "A 40MHz-BW 320MS/s Passive Noise-Shaping SAR ADC with Passive Signal-Residue Summation in 14nm FinFET," *ISSCC*, pp. 330-332, Feb. 2019.

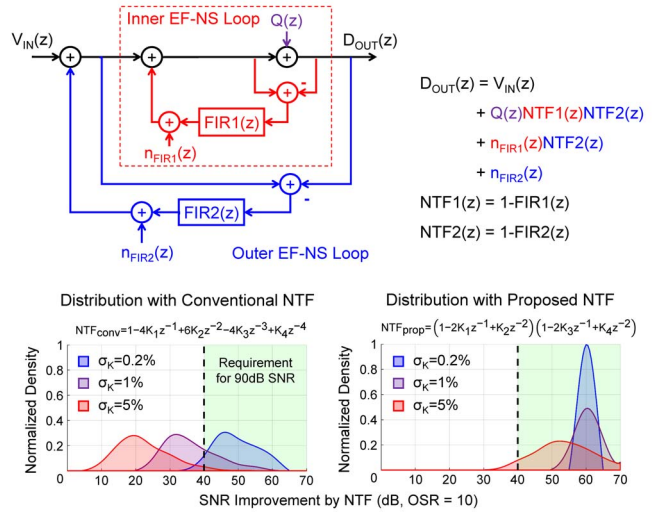


Figure 9.4.1: Signal model of the proposed CaNS architecture (top), and SNR distributions for proposed and conventional NTFs with coefficient variation (bottom).

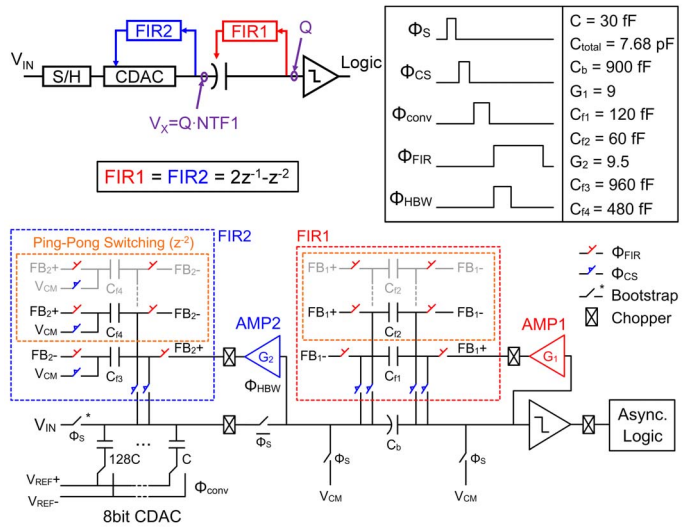


Figure 9.4.2: Implementation of the proposed CaNS-SAR (single-ended) and the corresponding timing diagram.

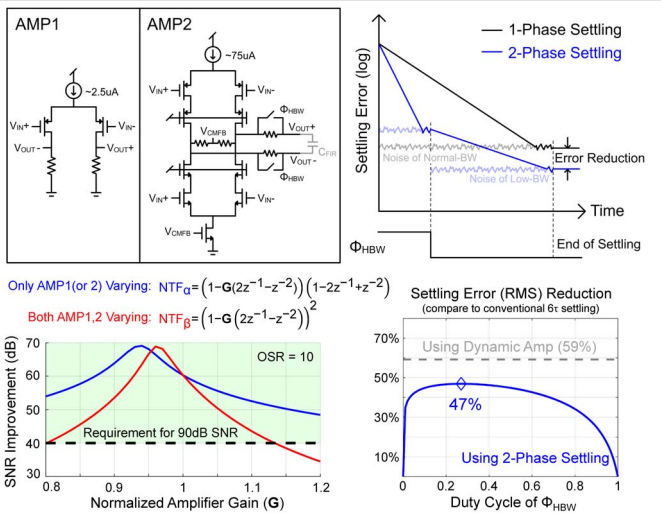


Figure 9.4.3: Amplifier schematics (top-left), proposed two-phase settling (top-right), reduction in error with two-phase settling (bottom-right), and theoretical SNR variation with gain variation (bottom-left).

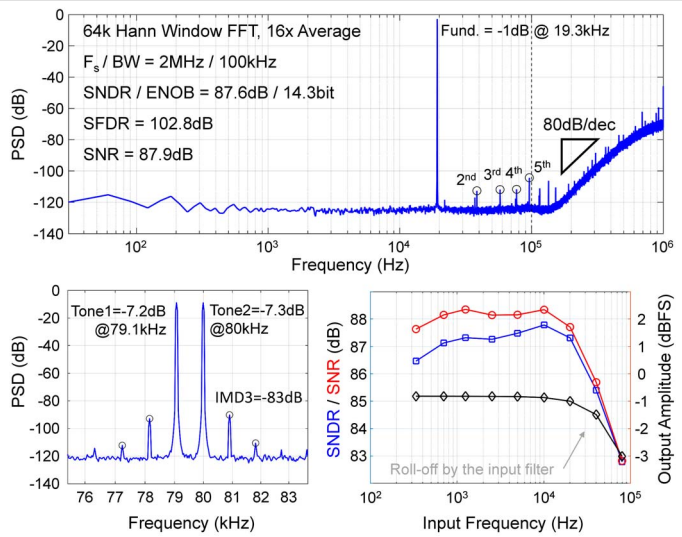


Figure 9.4.4: Measured output spectrum with single-tone input (top), spectrum with two-tone input (bottom-left) and measured SNDR vs Fin (bottom-right).

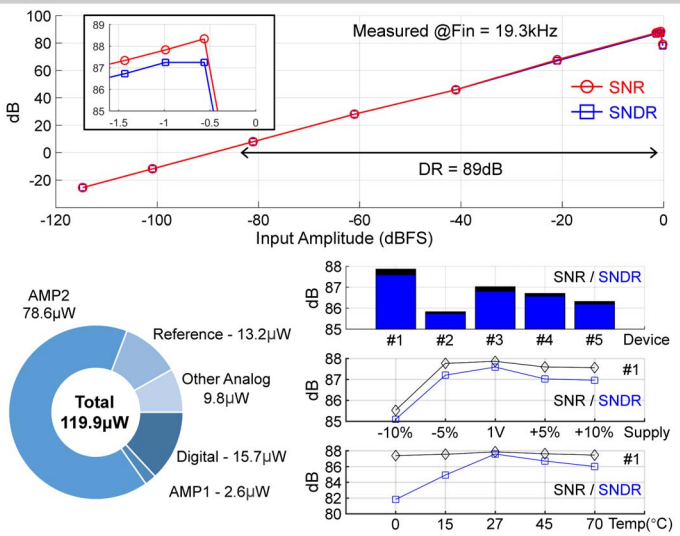


Figure 9.4.5: Measured SNDR vs. input-signal amplitude (top), power breakdown (bottom-left), and measured performance over PVT (bottom-right).

	This work	ISSCC 2018 S. Li	VLSI 2017 W. Guo	ISSCC 2018 P. Vogelmann	VLSI 2018 C. Lee
Architecture	CaNS-SAR	NS-SAR	NS-SAR	DT-SD	CT-SD
NTF Order	**4**	2	2	3	3
PVT Stable	**Yes**	No	No	Yes	Yes
Process (nm)	28	40	40	180	65
Area (mm^2)	**0.02**	0.024	0.04	0.363	0.14
Supply (V)	1	1.1	1.1	3	1.2
Power (µW)	120	84	143	1100	68
Fs (MHz)	2	10	8.4	30	6.14
OSR	10	8	16	150	128
BW (kHz)	100	625	263	100	24
SNDR (dB)	87.6	79	80	86.6	94.1
SFDR (dB)	102.8	89	-	101.3	107
DR (dB)	89	80.5	-	91.5	98.2
FOMs (dB)	176.8	177.7	172.6	166.2	179.6

Figure 9.4.6: Comparison table.

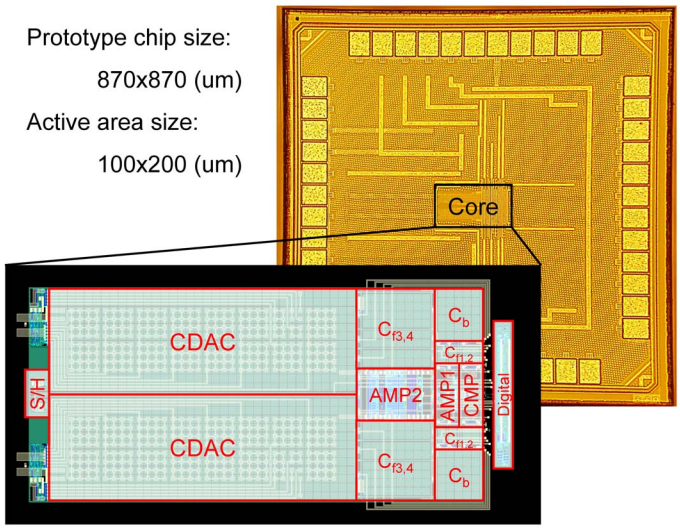
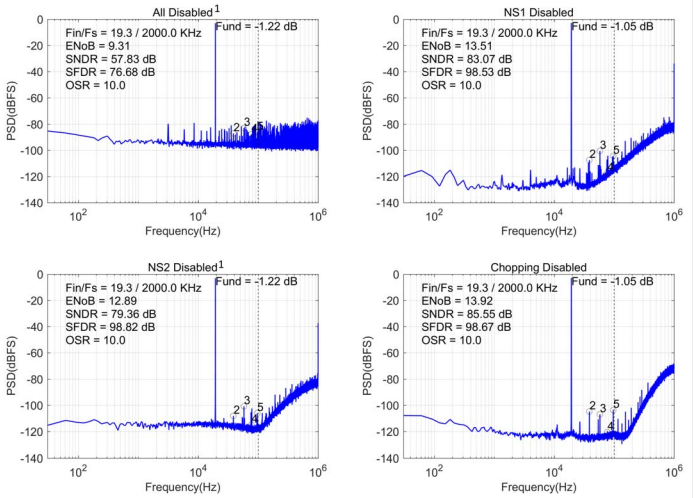


Figure 9.4.7: Die photo.



1. Input amplitude is set lower when NS2 is disabled to compensate for the attenuation from charge-sharing.
2. All measurements are made with same off-chip calibration for CDAC mismatch.
3. All measurements are done on Device #3.

Figure 9.4.S1: Measured spectrums for different configurations.

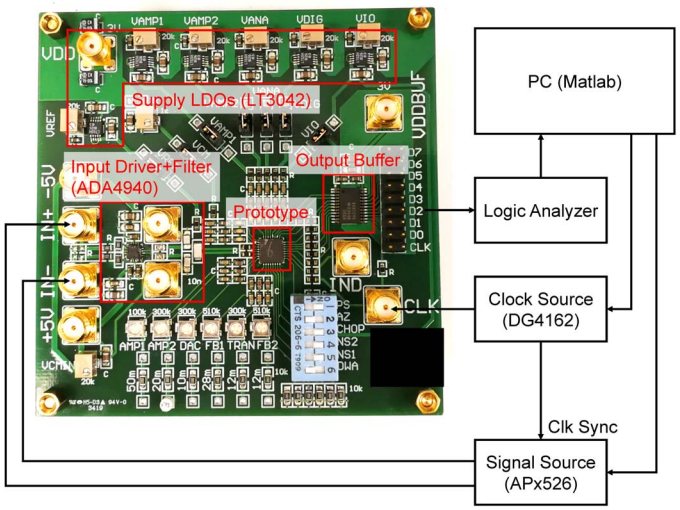


Figure 9.4.S2: Test setup.

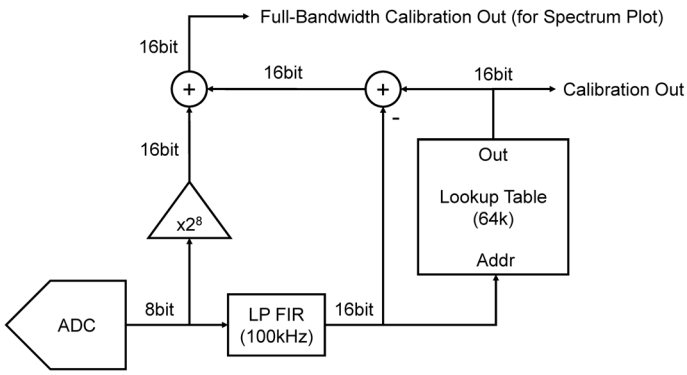


Figure 9.4.S3: Off-chip calibration for CDAC mismatch.

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