A Calibration-Free Time-Interleaved Fourth-Order Noise-Shaping SAR ADC

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***Abstract*— Noise-shaping SAR (NS-SAR) is an emerging analog to digital converter (ADC) architecture that offers both high-resolution and high-energy efficiency. Despite these advantages, oversampling limits the useful bandwidth of NS-SAR ADCs. This article introduces a robust and practical interleaving architecture that overcomes this bandwidth limitation. Midway feedback to multiple successive-approximation conversion phases enables a realizable time-interleaved noise-shaped (TINS) system. The inherent delay between channels is harnessed to generate a high-order noise-transfer function (NTF). Redundancy and optimization of the NTF coefficients eliminate the risk of quantization overload, ensuring robust operation. Error feedback (EF) is realized with a summing pre-amplifier and a shared feedback bus, keeping the architecture simple. Thanks to the low required gain, the pre-amplifier is simply implemented as a single-stage open-loop amplifier. A prototype 40-nm CMOS TINS-SAR ADC has a measured SNDR of 70.4 dB for a 50-MHz bandwidth. It consumes only 13 mW and occupies 0.06 mm^2. Testing of several devices and evaluation over temperature and supply variations demonstrate robust performance without calibration.**

***Index Terms*— Analog to digital converter (ADC), calibration free, noise shaping, successive approximation (SAR), time interleaving.**

I. Introduction

NOISE shaping in successive approximation (SAR) analog to digital converters (ADCs) enables both high-resolution and high-energy efficiency [1]. State-of-the-art NS-SAR ADCs eliminate the need for op-amps, which relaxes design complexity and technology scaling issues [2]–[4]. However, the need for oversampling limits the effective bandwidth of NS-SAR ADCs making them unsuitable for applications that need bandwidths in the tens of megahertz range, such as wireless communications. Traditionally, high-bandwidth, high-resolution applications depend on pipeline or continuous-time sigma–delta (CT-SD) ADCs, but these architectures are much more power hungry than the NS-SAR. To increase the bandwidth of NS-SAR ADCs and extend their low-power advantages, this article presents a new time-interleaved NS SAR (TINS-SAR) architecture that enables higher bandwidth [5].

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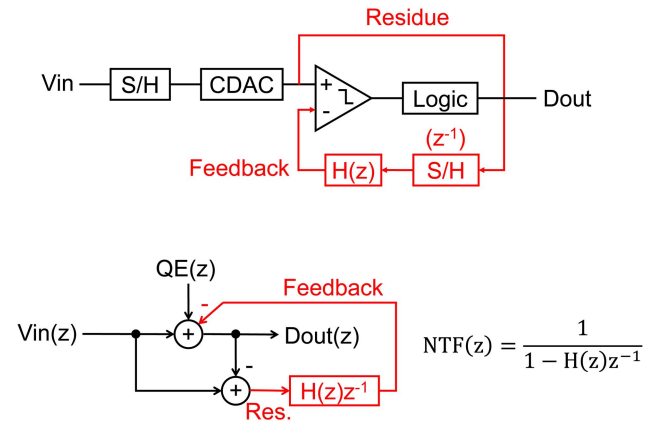

Fig. 1. NS SAR (top) and its equivalent signal model (bottom).

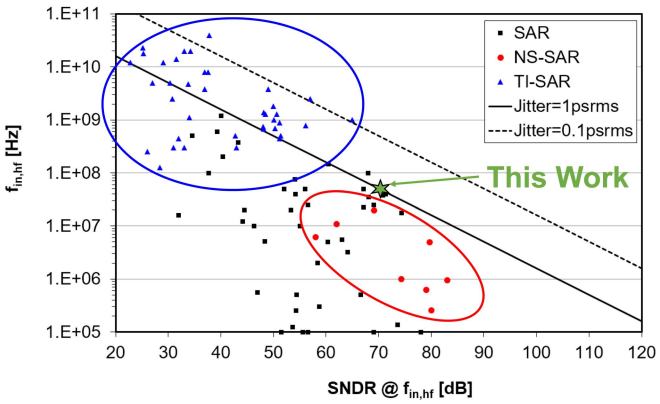

Fig. 2. Bandwidth and resolution of SAR, NS-SAR, and TI-SAR ADCs, using data from [6].

The NS-SAR makes use of the fact that the quantization error, or residue, can be easily captured, as it is naturally held on the capacitor DAC (C-DAC) after conversion. We can form a feedback system similar to a SD modulator by passing this residue through a loop filter and feeding it back to an extra comparator input, as shown in Fig. 1. In this way, NS increases the in-band signal-to-noise ratio (SNR) and the effective resolution of the ADC. Early versions of the NS-SAR ADC require power-hungry op-amps, which diminish the energy efficiency of SAR. Recently, passive or op-amp-free NS-SAR ADCs [2]–[4] enable NS-SAR ADCs with similar power efficiency to conventional SAR ADCs, but bring the advantage of much higher resolution.

Fig. 2 shows the relationship between SNDR and input bandwidth for recent SAR ADC designs and clearly reveals the performance regions for TI-SAR, NS-SAR, and traditional

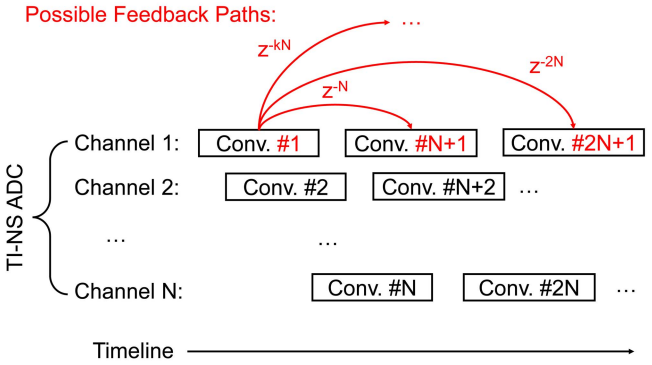

Fig. 3. Direct interleaving of NS ADCs. (Here feedback is within the same channel.)

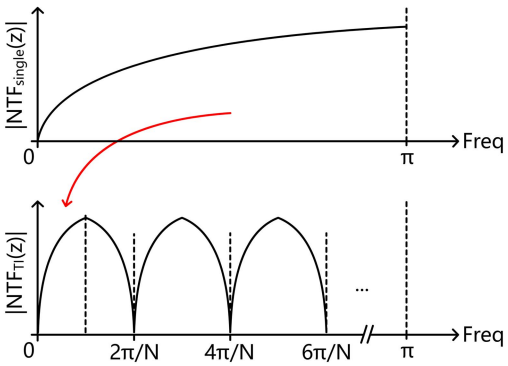

Fig. 4. Comparison of the original NTF for single NS-SAR ADC (top) and the repeating pattern of the interleaved NTF (bottom).

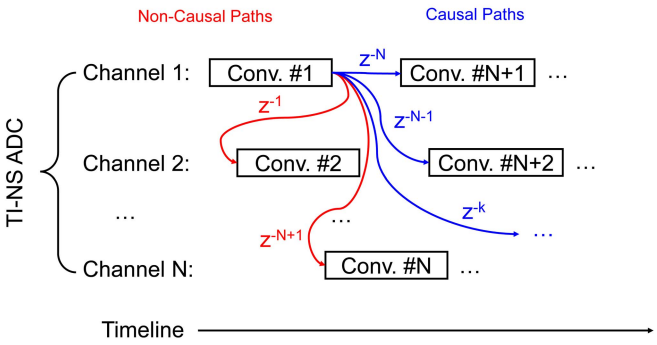

Fig. 5. Inter-channel feedback and the possible non-causal paths.

SAR ADCs [6]. TI-SAR ADCs deliver the highest bandwidth, but with relatively low SNDR. Conversely, NS-SAR ADCs occupy the highest SNDR region but have limited bandwidth. Our new SAR-based architecture combines NS with time interleaving, to break tradeoff between speed and accuracy, and enable both high speed and high resolution. To the best knowledge of the authors, the prototype ADC delivers the highest bandwidth among all reported NS-SAR ADCs and achieves similar performance to CT-SD ADCs.

Although interleaving might seem to be a natural evolution of the NS-SAR, interleaving of NS ADCs is challenging. Section II discusses the challenges of time interleaving of NS-SAR ADCs and introduces the new midway feedback architecture. Our approach harnesses the inherent delay between channels to generate a high-order noise-transfer function. Section III focuses on system-level considerations and how we ensure the robustness of the midway error feedback (EF) architecture. In particular, SAR ADC redundancy and optimization of the NTF coefficients eliminate the risk of quantization overload. Section IV explains the circuit-level implementation in detail. The EF scheme uses a summing pre-amplifier and a shared feedback bus. Thanks to the low required gain, the pre-amplifier is a simple single-stage open-loop amplifier. Section V provides measurement results of the prototype ADC. Measurements of several devices and testing over temperature and supply demonstrate robust performance without the need for calibration. Section VI is the conclusion.

II. Interleaving of NS ADCs

A. Direct Interleaving

Although time interleaving is a potential way of mitigating the reduced bandwidth of NS ADCs, the combination of time interleaving and NS is challenging in practice. The difficulty is not only in the circuit-level implementation but is also fundamental at the system level. This system-level difficulty is related to the inevitable feedback delay in a time-interleaved system. When we attempt to interleave multiple ADCs containing feedback, the effective feedback delay changes. Thus, the overall system does not preserve the NS transfer function of the individual NS ADCs.

To better explain this, Fig. 3 shows a direct attempt at interleaving multiple conventional NS ADCs. Feedback is within each NS ADC; however, due to the interleaving, the actual feedback delay is a N times the interleaved-ADC sampling period. This means that all unit delays, z^{-1}, in the individual NTF are replaced with z^{-N}. Therefore, the equivalent NTF of this TI-NS ADC becomes

$$\mathrm{NTF_{TI}}(z) = \mathrm{NTF_{single}}(z^N).$$

Fig. 4 shows the resulting NTF. Since the overall NTF is now a repeating pattern, it is impossible to synthesize the desired single-notch NS characteristic.

B. Inter-Channel Feedback and Causality Restrictions

Inter-channel feedback is a promising approach to noise shaping in interleaved ADCs (Fig. 5). With inter-channel feedback, feedback paths travel from each channel to all channels, instead of only to the channel itself. Hence, the effective feedback signal delay can be as small as a single sampling delay, so that the NTF can be similar to a classical NS ADC.

Nevertheless, the TI-NS ADC shown in Fig. 5 is not physically realizable as some of the feedback signal paths are non-causal. Inter-channel feedback paths traveling earlier in time cannot be implemented. If we attempt to make these inter-channel feedbacks causal, then each channel must finish conversion before the next channel starts, as shown in Fig. 6. However, imposing this requirement eliminates the benefit of interleaving as there is no longer an overlap between channels to improve conversion throughput.

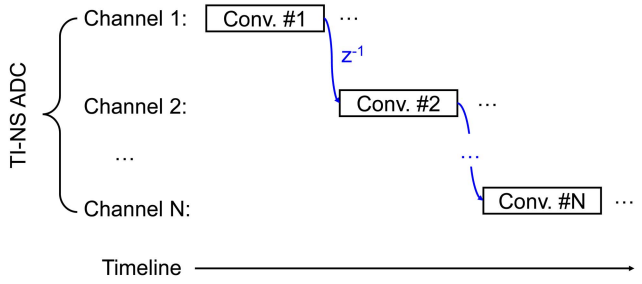

Fig. 6. This causal inter-channel feedback loses the throughput advantages of interleaving.

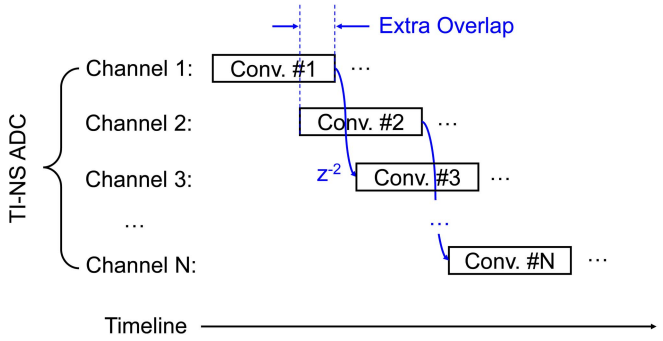

Fig. 7. Timing diagram for a TINS ADC with no single interleaving period (z^{-1}) delay.

C. Midway Feedback and Multi-Phase Conversion

As discussed above, it is difficult to retain the benefits of interleaving and maintain flexibility in the transfer function. Although this may seem discouraging, we can still draw two useful conclusions between Figs. 5 and 6. First, for a feedback path with longer delay, that is, traveling from a channel to another channel further separated in the interleaving sequence, the causality restriction is relaxed. For example, if a TI-NS system does not have any feedback from a channel to an adjacent channel (i.e., there is no z^{-1} term in the transfer function), then there can still be some overlap in the conversions, as shown in Fig. 7. Therefore, if we can decompose the system into subsystems each with different delays, each subsystem can retain some benefits of interleaving (except for the subsystem with a delay of z^{-1}).

Second, the discussion above is based on the analysis of the feedback system. However, in a practical ADC system, many other actions introduce delay, including sampling, signal settling, and logic delay. All these events are not restricted by the causality considerations that we mention, and therefore can be overlapped (i.e., interleaved) for higher ADC throughput.

Inspired by these observations, we propose a midway feedback based on multi-phase conversion to implement a realizable TINS system. Fig. 8 shows the timing sequence for a second-order midway feedback system. The conversion process for each channel is decomposed into multiple phases, and each phase performs only part of the conversion. The feedback path is also decomposed into multiple feedback paths

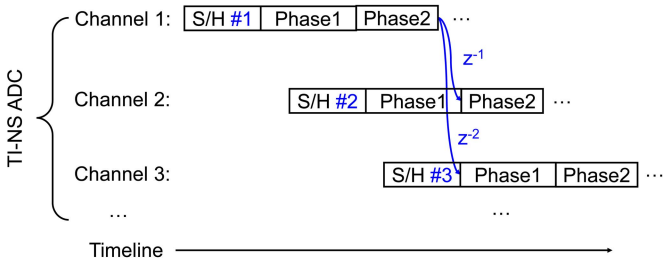

Fig. 8. Timing diagram for the 2nd-order midway feedback.

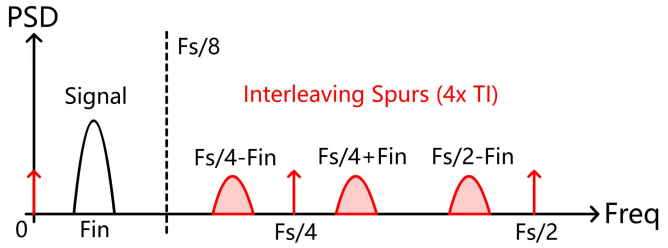

Fig. 9. Output spectrum due to channel mismatch (4× TI as example).

with different delays. Each sub-path feeds between different phases of different channels, enabling the maximum overlap.

D. Non-Idealities of Interleaving

As mentioned in the introduction, a significant drawback of time interleaving is the degradation in accuracy due to the mismatch between the channels. Typically, three kinds of mismatch dominate: offset mismatch, gain mismatch, and sampling skew. Offset mismatch causes input-independent tones at (F_S/N) and its multiples, where F_S is the overall sampling rate and N is the number of channels. Gain mismatch and sampling skew cause modulation around (F_S/N) and its multiples [7], as shown in Fig. 9.

For interleaved Nyquist-rate ADCs, these artifacts fall in the band of interest, and therefore the performance of traditional TI ADCs is highly sensitive to mismatch. However, for a TI-NS ADC, the band of interest is reduced by the over-sampling rate (OSR). We notice in Fig. 9 that as the artifacts are only located at frequencies around (F_S/N), it is possible to limit the bandwidth of interest so that the interleaving artifacts all fall out of band. More specifically, assuming the signal band is from dc to BW, the lowest possible artifact is located at $(F_S/N) - \mathrm{BW}$. Thus, if we limit

$$\mathrm{BW} < \frac{F_S}{N} - \mathrm{BW}$$
$$\text{or } \mathrm{OSR} = \frac{F_S}{2\mathrm{BW}} > N$$

then, the artifacts fall out of band. In this way, TINS ADC can suppress the mismatch problem naturally. This is a significant advantage as generally TI ADCs need complicated and power-hungry calibration to mitigate the impacts of channel mismatch. Although out-of-band blockers can still be mixed-down into the signal band, in this case, a pre-filter can be used to suppress the out-of-band blockers. An advantage

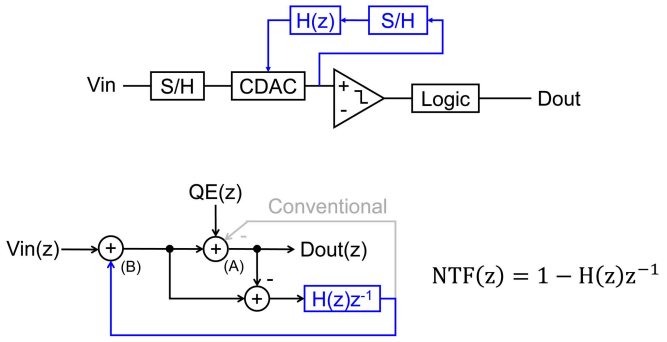

Fig. 10. EF structure (top) and the equivalent signal model (bottom).

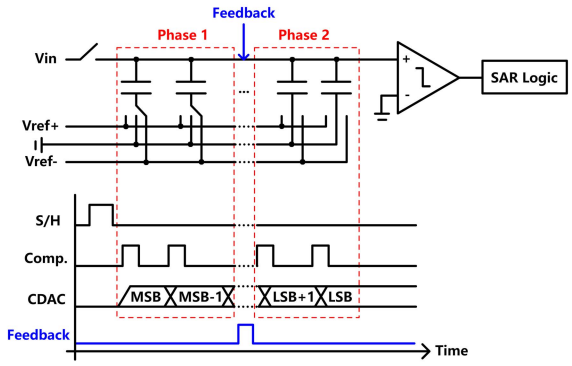

Fig. 11. Multi-phase division of SAR ADC (two-phase example).

is that this filter can be simpler than the anti-aliasing filter in a Nyquist rate ADC, as the modulation by channel mismatch is relatively weak.

III. Proposed TINS-SAR

A. Loop Filter

The loop filter, at the core of an NS-SAR ADC, dominates the overall performance. Conventionally, the loop filter is a cascaded FIR-IIR structure to synthesize the desired low-pass NTF, as shown in Fig. 1. However, the implementation of an IIR filter is challenging because power-hungry, scaling-unfriendly op-amps are needed to make switched-capacitor (SC) integrators. An alternative is to build passive integrators through charge sharing, but the resulting low loop gain limits the performance of the NTF. Many recent NS-SARs [2], [4] use the latter approach in order to preserve the energy efficiency of the SAR architecture. Since high-order passive IIR filters are very difficult to implement, NS-SARs with NTF orders higher than the two are rarely reported.

The EF structure, shown in Fig. 10, eases the implementation of the loop filter [3]. The EF structure directly feeds the residue back into the C-DAC instead of to the comparator. From a system view, the feedback summing node is moved from A to B. Therefore, the overall NTF changes to $1 - H(z)z^{-1}$. We notice that the loop filter, $H(z)$, now appears in the numerator of the NTF rather than in the denominator, which means that zeros, rather than poles, are required in the $H(z)$ to shape the NTF as low pass (or bandpass). An advantage is that since poles are no longer necessary in the loop filter, we do not need to implement an IIR filter, as an FIR filter alone can provide the zeros we need in $H(z)$. An FIR filter is much easier to implement than an IIR filter, and therefore the EF structure is naturally a good candidate for a TI-NS-SAR ADC. Section III-B discusses our proposed TI-NS-SAR implementation which extends EF to midway feedback.

B. Midway Error Feedback Using Inherent Delay

As described above, midway feedback is a key to interleaving NS ADCs, and a prerequisite for midway feedback is the decomposition of the original conversion into multiple phases. Fortunately, it is easy to decompose the SAR conversion

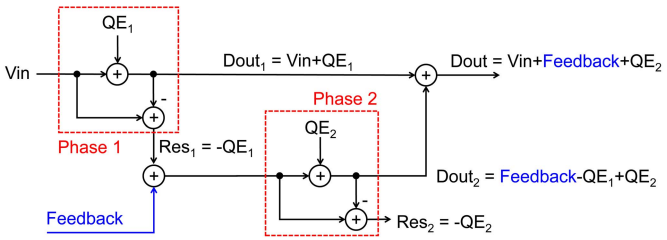

Fig. 12. Channel signal model with injected midway feedback signal.

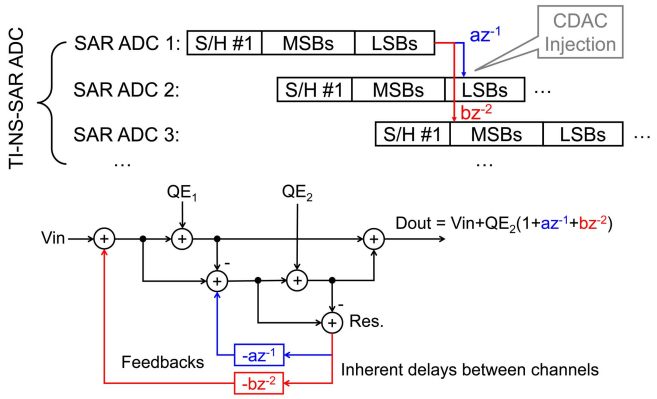

Fig. 13. 2nd-order midway EF and its signal model.

process. As a SAR conversion has multiple cycles, we can simply group these cycles into phases, as shown in Fig. 11. Such a division is only in a logical sense, as each phase of the conversion is still performed with the same physical circuitry. However, similar to a pipeline ADC with an inter-stage residue gain of 1, each phase partially digitizes the signal and passes a residue to the next phase.

Although each conversion phase generates its own independent quantization noise, this noise is digitized in subsequent phases and passed to the digital output. Eventually, the quantization noise from all phases, except the last, cancels at the output. Furthermore, as long as the ADC is not overloaded, any signal injected onto the C-DAC, irrespective of the phase the conversion, is also digitized and passed to the digital output, as shown in Fig. 12. Later, Section III-C discusses overload.

We realize the midway EF based on such a conversion division, as shown in Fig. 13. The combination of C-DAC injection

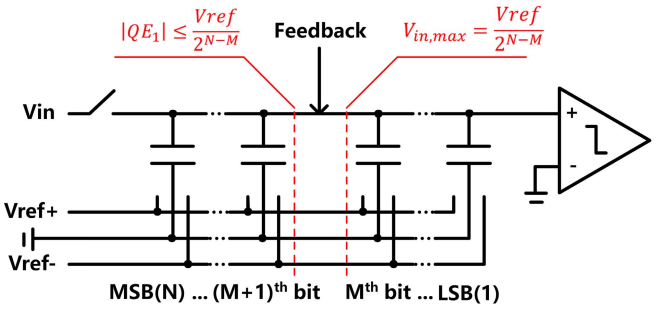

Fig. 14. Potential overload caused by feedback injection.

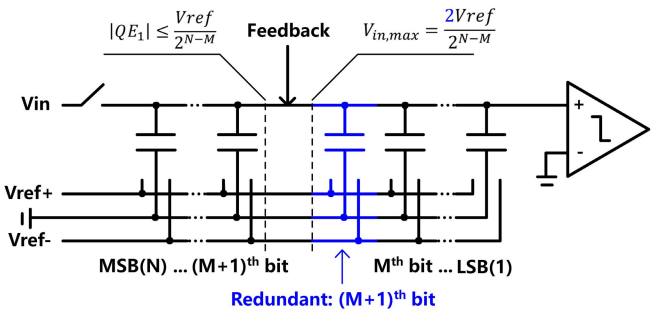

Fig. 15. Redundant bit enlarges the quantization range.

and time interleaving enables a practical implementation of the FIR filter. Recall that for midway feedback, we decompose the feedback path into multiple different feedbacks with different delays. We simply sum different delayed paths with appropriate weights to form any desired FIR filter. In other words, we make use of the inherent delay between different channels in a TI ADC to significantly simplify the overall architecture.

C. Overload

Although midway feedback in a TINS-SAR is elegant and straightforward, it is susceptible to overload, especially during the latter quantization phases. We simply model each quantization phase as an ideal quantizer with purely additive quantization noise. However, this model fails when the input signal is larger than the maximum quantization range of the quantizer. In a multi-phase SAR, since there is no gain between phases, the quantization range shrinks due to the successive-approximation steps, as Fig. 14 shows; thus, the condition, QE + Feedback $> V_{\text{in,max}}$ can easily occur. In particular, for the final phase, the conversion range is as small as a few LSBs. Therefore, even a small injected feedback signal can cause overload.

Once overload occurs, the digital output of the quantizer can no longer be regarded as the summation of the input and noise, and therefore the assumption of quantization noise cancellation no longer holds. As a result, the overall NS performance badly degrades, and the system can even become unstable. Worse, for a high-order FIR filter, the coefficients are large, which means that the injected feedback signal is amplified making overload even more likely.

We introduce two modifications to solve the overload problem. First, we add redundant bits to each quantization phase. Conventionally, redundancy relaxes the settling requirement for the C-DAC [8], as decision errors can be repaired in extra conversion cycles. The extra redundant decision bits provide additional input range to tolerate errors made by previous decisions. This extra signal range also helps with the overload problem, as shown in Fig. 15. Although additional redundancy bits can further prevent overload, the tradeoff is reduced overall sampling rate. In practice, we add redundant bits mainly to the last phase as it has more limited conversion range and is easier to overload.

Second, we reduce the coefficients of the FIR filter to limit the amplitude of the feedback signals. As mentioned,

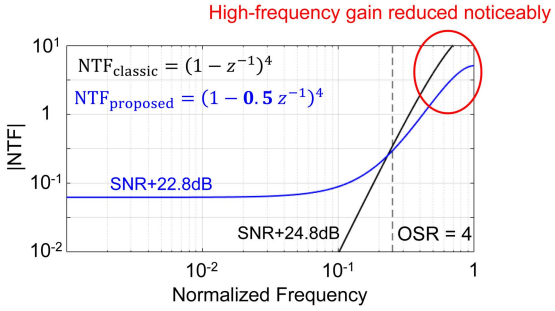

Fig. 16. Comparison of an aggressive NTF and a mild NTF.

the coefficients of a high-order FIR filter are generally large, especially for an aggressive NTF such as $(1-z^{-1})^N$. However, for NS ADCs with low OSR, a mild NTF with relatively small coefficients still delivers near-optimum SNR. Fig. 16 shows the comparison of the performance for a conventional NTF and for a mild NTF to illustrate this idea. In our prototype, we use $(1 - 0.5z^{-1})^4$ since the 0.5 coefficient is easily implemented in layout with a ratio of 2.[1] Another advantage is that a mild NTF is much more tolerant to coefficient variation. This is an important advantage as pole and zero positions always vary in real circuits due to mismatch and gain variations. An aggressive NTF degrades rapidly in the presence of small variation even without considering overload. We discuss this in detail in Section IV-B.

D. Implementation and PVT Considerations

Our proposed TINS-SAR architecture is stable and practical thanks to the two overload mitigation techniques, described above. The prototype TINS-SAR ADC targets a 400 M/s sampling rate with four-way interleaving. It employs fourth-order EF-based NS, as shown in Fig. 17.

Each channel of the TINS-SAR performs 16 conversion cycles grouped in four phases. The 6 bits of redundancy are added to the 10-bit binary digitization to eliminate overload based on model simulation results. As mentioned, the NTF is relaxed to $(1 - 0.5z^{-1})^4$ to help further prevent overload. We discuss the implementation in detail in Section IV.

[1]Technically, the architecture can support a more optimized NTF.

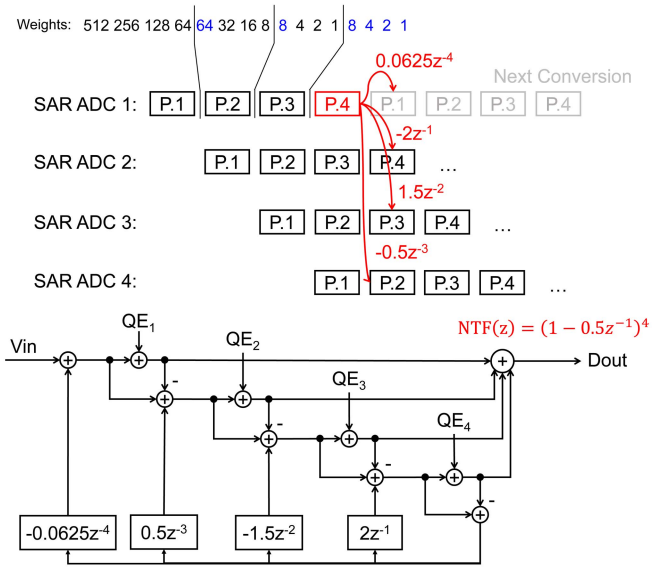

Fig. 17. Prototype TINS-SAR ADC (top) and its signal model (bottom).

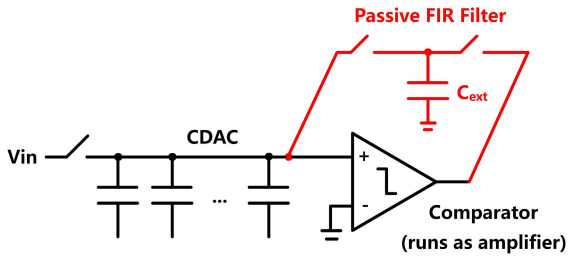

Fig. 18. Conventional charge sharing summation in EF [3].

IV. Implementation Details

A. Summing Pre-Amplifier Based EF

In this section, we first focus on the implementation of EF. Since the delay needed for the FIR filter is inherent in our proposed time-interleaved system, we need only consider the summation and weighting of the feedback values. Previous work on EF-NS-SAR [3] sums the EF signal with an extra capacitor, C_{ext}, as shown in Fig. 18. This approach first samples the residue on C_{ext}, which is then connected to the C-DAC in the next conversion to inject the feedback value through charge sharing. However, this passive charge-sharing approach inevitably attenuates the signal sampled on the C-DAC. This attenuation is problematic for the proposed TI-NS architecture, since the cancellation of quantization error is no longer valid if the gain of the residue changes (assuming C_{ext} is disconnected after injection). In [3], a large sharing ratio (i.e., a small C_{ext}) minimizes such attenuation. Nevertheless, the design in [3] requires a high-gain residue amplifier to compensate for the attenuation error—this amplifier can be as difficult to design as the amplifier in a conventional NS-SAR.

We introduce a summing pre-amplifier to accomplish C-DAC injection, as shown in Fig. 19. In each channel, a summing pre-amplifier drives the comparator. The pre-amplifier output also provides feedback to all the interleaved channels through a single shared analog bus. The pre-amplifier is a multi-input low-gain differential amplifier, with its inputs

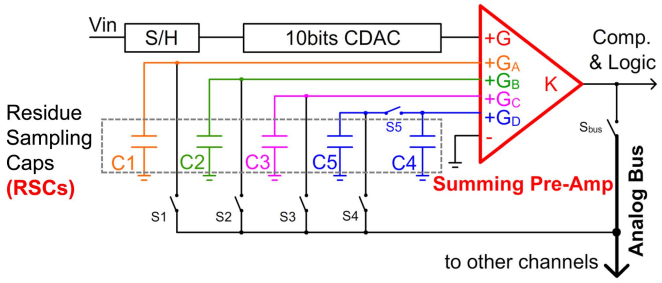

Fig. 19. Summing pre-amplifier implementation of EF.

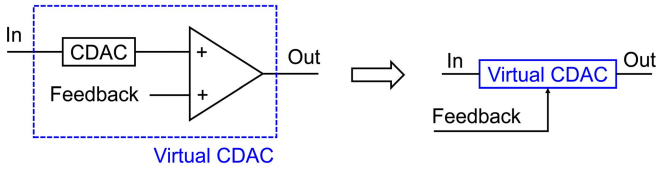

Fig. 20. Pre-amplifier and C-DAC form a virtual C-DAC that realizes an equivalent feedback injection.

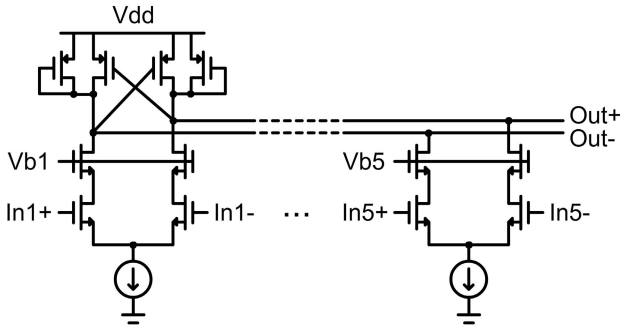

Fig. 21. Summing pre-amplifier schematic.

connected to the C-DAC and to four residue sampling capacitors (RSCs) ($C1$–$C4$ in Fig. 19), which hold the feedback signals from each channel. The pre-amplifier sums and weights the C-DAC voltage as well as the stored feedback values. Thus, the output of pre-amplifier is equivalent to C-DAC output voltage after feedback injection. From another point of view, the pre-amplifier and the C-DAC form a Virtual C-DAC (Fig. 20) that realizes feedback injection.

There are significant benefits to using a pre-amplifier. First, the charge on the C-DAC is not contaminated during the feedback operation, and the cancellation of quantization error is therefore preserved. Second, the pre-amplifier provides good isolation between the comparator and both the C-DAC and the RSCs (which hold the feedback voltages), thereby reducing concerns of comparator kickback. Third, the pre-amplifier can be realized as a simple single-stage open-loop amplifier due to the low required gain. A single-stage open-loop amplifier is smaller and more power efficient than a high-gain amplifier and is also easier to implement in modern CMOS processes. Furthermore, unlike a dynamic amplifier, such an amplifier does not require accurate timing or calibration.

In the pre-amplifier, multiple differential pairs with ratioed sizes drive a cross-coupled diode load, as shown in Fig. 21.

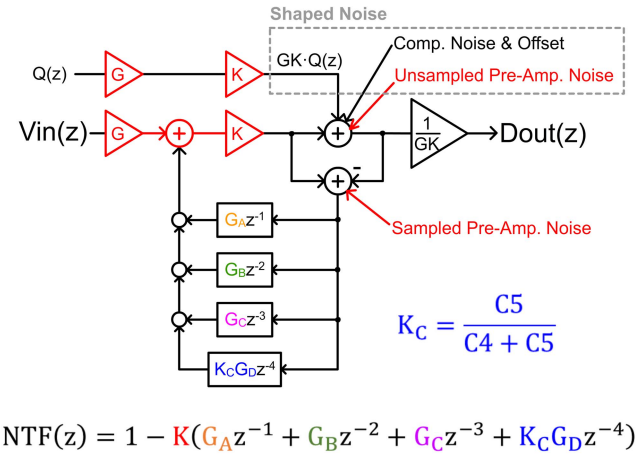

Fig. 22. Signal model considering noise and gain variation.

Different input pair sizes implement the various feedback-gain coefficients (i.e., G, G_A–G_D), shown in Fig. 19. The amplifier provides the required gain ($\sim$10$\times$ considering all inputs) and a stable common-mode output voltage. Since the input of the amplifier (i.e., the residue) is only a few megavolts, the linearity of such open-loop design is sufficient for the target ADC SNDR. At any time, only one channel is completing conversion and generating a residue to feed back. A shared bus (i.e., analog bus in Fig. 19) passes feedback between channels, keeping the wiring implementation simple. In addition to the inter-channel sampling capacitors ($C1$–$C3$), an auxiliary capacitor ($C5$) samples the residue of the channel itself. After $C5$ samples the pre-amplifier output of the channel, this sampled value is passed to the corresponding residue storage capacitor ($C4$) by simple charge-sharing. The attenuation due to charge-sharing (noted as K_C in Fig. 22) is simply considered to be part of the feedback coefficient.

B. Noise and PVT Considerations

The noise from the summing pre-amplifier is a main source of the total noise, but fortunately it is partially shaped by the NTF and can be well controlled. Fig. 22 shows a signal model that considers pre-amplifier noise. The noise of the pre-amplifier contributes differently in conversion and feedback. During the conversion phase, the noise of the pre-amplifier (unsampled noise in Fig. 22) can be referred to the output and combined with the comparator input-referred noise. In this case, the noise of the pre-amplifier and comparator are shaped by the NTF and thus has a negligible effect on performance.

During the feedback phase, while the pre-amplifier is generating a residue, the noise of the pre-amplifier is sampled onto the RSCs and added to the feedback summation node. Therefore, this noise contribution is determined by the signal transfer function (STF) rather than NTF and is not shaped. Fortunately, during the feedback phase, the required signal-settling speed is much slower than during the conversion phase. Therefore, the bandwidth of the pre-amplifier can be significantly reduced to limit thermal noise. Such a bandwidth reduction is easily realized by the loading of RSCs, and therefore this part of pre-amplifier noise contribution is well controlled.

PVT variation is another concern with open-loop amplifiers. Although the offset of the pre-amplifier does not affect performance, as it is similar to the comparator offset and only causes out-of-band mismatch tones, another concern is that the gain is inaccurate and sensitive to variation. However, since the inputs of the pre-amplifier are built with layout-matched differential pairs and drive the same load, the gain ratio between the different inputs is quite precise and independent to PVT variation. To explain this advantage, the signal model in Fig. 22 decomposes the gain of the pre-amplifier into gain ratio and common gain. G and G_A–G_D represent the nominal gains of different inputs, which are matched by layout techniques. K, nominally equal to 1, represents the common-gain variation from PVT. In modern CMOS processes, it is relatively easy to get 1% or better gain matching (i.e., G and G_A–G_D accuracy), while the common-gain variation, K, is roughly 10% or even higher. Interestingly, while our proposed NTF strongly depends on the gain ratios, it only weakly depends on the common gain. This advantage is clearly shown by the behavioral-level Monte Carlo simulations reported in Fig. 23. These simulations use a behavioral TINS-SAR model and vary the NTF coefficients and channel mismatch. With a 10% RMS gaussian common gain variation, the proposed NTF provides a robust SNDR improvement, while the conventional NTF suffers from large performance degradation and the risk of instability. Therefore, the performance of the pre-amplifier-based approach is robust enough under PVT variation to be free of calibration, even though the amplifier itself may have a large absolute gain variation. This feature also relieves the settling requirements of the amplifier, as any settling error can simply be considered as a common-gain reduction.

C. Timing

Asynchronous logic is commonly used to maximize the sampling rate of SAR ADCs [9]. A possible concern with asynchronous logic in the TINS-SAR architecture is the difficulty of aligning feedback timing between channels. Although in our analysis, we assume that the conversion phases of different channels are perfectly aligned in time, and that feedback happens right at the end of the last phase of each channel (Fig. 17); such strict timing is not necessary in practice. As mentioned, the division of conversion phases is a grouping the conversion cycles of SAR in a logical sense. Therefore, there is no need to have equal division of phases as any grouping is valid for the analysis. In the case that the conversion phases of different channels are misaligned due to mismatch in the asynchronous logic or due to input-dependent delay of the comparator, the only change from the signal point of view is the magnitude of quantization error of each phase (exclude the last phases), as shown in Fig. 24. Since the quantization errors of the former phases are eventually cancelled at the output, such a timing misalignment does not affect the overall performance, as long as the timing skew is not large enough to trigger overload. In measurements, we did not observe any overload by timing issues.

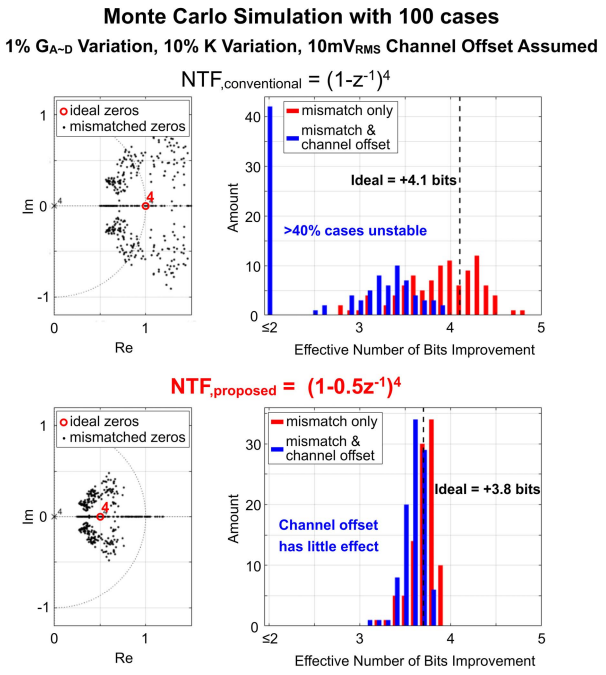

Fig. 23. Gain variation and channel mismatch effects for the conventional and proposed NTF.

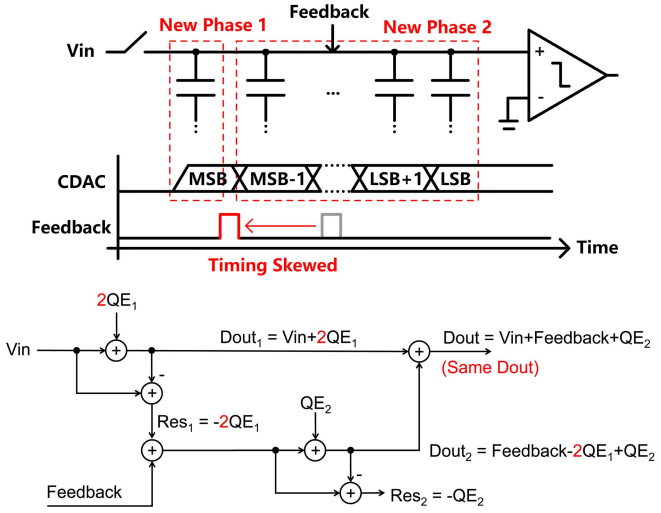

Fig. 24. Feedback timing skew has no effect on the system behavior. In this example, timing skew causes the feedback signal to be early. In the signal model, the quantization error from the first phase is enlarged by 2× as phase 1 is now shortened by one SAR cycle.

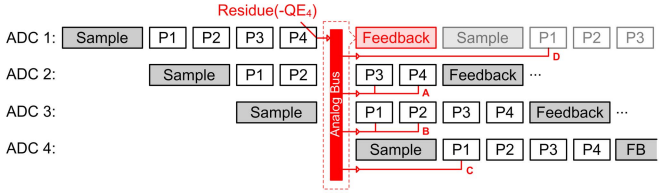

Fig. 25. Actual ADC timing sequence.

Fig. 25 shows the actual timing sequence of the prototype, where phases 1 and 2 are approximately aligned to phases 3 and 4, respectively. Thus, some of the feedbacks are

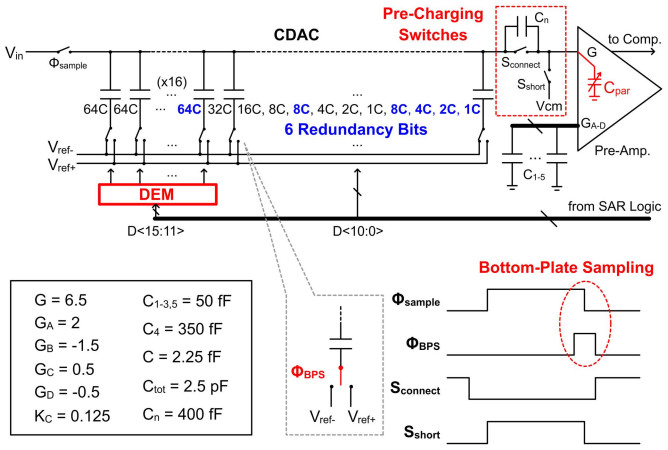

Fig. 26. DEM, BPS, and parasitic pre-charging technique enhance linearity.

actually injected in earlier phases than is shown in Fig. 17. Note that Fig. 25 only illustrates the timing in the nominal case and is subject to possible skew. The advantage of such a design is that more time can be assigned to the feedback phase, so that the bandwidth of the pre-amplifier can be smaller and the noise minimized. Similarly, the sampling phases are also lengthened to improve the linearity of the bootstrap switch.

D. Linearity Enhancements

NS effectively reduces the noise floor due to quantization error and comparator noise. Nevertheless, NS does not improve the linearity of ADC, which can then limit performance in high-resolution applications. We introduce three linearity enhancements, shown in Fig. 26, to help maintain the accuracy advantage of the proposed TINS-SAR architecture. First, dynamic element matching (DEM) shuffles the four MSBs of the CDAC, reducing distortion caused by CDAC mismatch. Second, the non-linear charge injection of the bootstrap switch is another source of distortion. To mitigate this, the CDAC switches connected to the bottom-plates are disconnected shortly before the bootstrap switch opens (i.e., during Φ_{BPS}), which equivalently realizes bottom-plate sampling (BPS) to prevent non-linear charge injection.

The third enhancement deals with the sizeable non-linear capacitance of the pre-amplifier input. In our design, the input pair of the pre-amplifier is large in order to reduce noise and improve matching. Inevitably, such a large input pair adds a large non-linear parasitic capacitance (i.e., C_{par}, ~50 fF) to the top plate of the C-DAC, which can cause noticeable distortion since the top plate of CDAC is still connected to the input signal before the actual sampling (similar to top-plate sampling). To solve this problem, our third linearity enhancement adds two extra switches (S_{short} and $S_{connect}$ in Fig. 26) to disconnect and pre-charge the non-linear parasitic capacitance to a fixed voltage (i.e., V_{cm}). In this way, the parasitic capacitance only shares a fixed charge with the C-DAC and does not harm the linearity. Here, we need only consider the charge sharing from C_{par} when the conversion is done. During the conversion, such charge sharing has a little effect since the comparator only measures the sign of CDAC voltage. A potential drawback

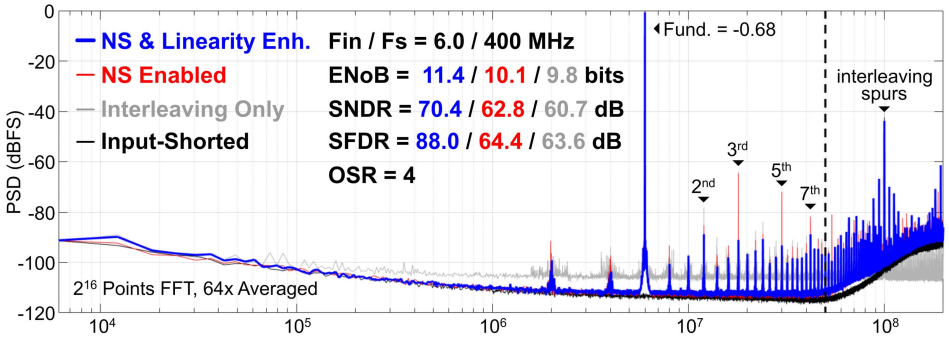

Fig. 27. Measured output PSD for different configurations.

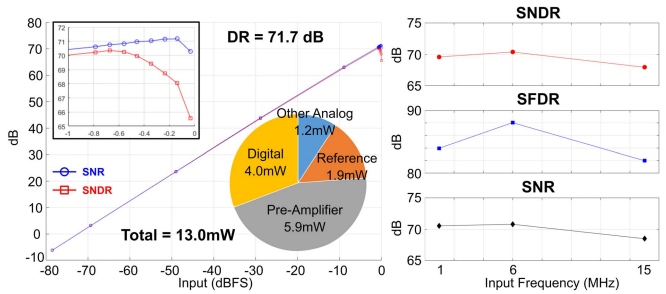

Fig. 28. Measured SNR/SNDR versus input power, power breakdown (left), and performance versus input frequency (right).

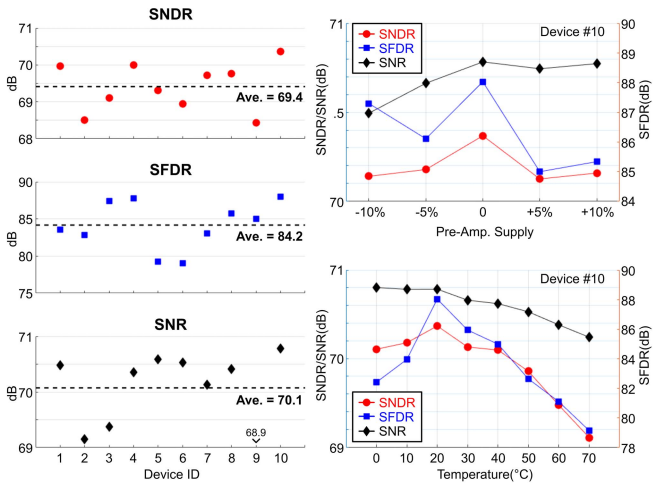

Fig. 29. Measured performance of ten devices (left), and measured performance under supply voltage, and temperature variation (right).

of this scheme is that the switch S_{short} induces a new noise source, which can be significant as C_{par} is small and thus the noise has a wide bandwidth. In order to limit this noise, an extra capacitor (C_n in Fig. 26) is placed across this switch to limit its noise bandwidth.

V. Measurements

The prototype TINS-SAR ADC is fabricated in 40-nm CMOS and has an active area of 0.06 mm^2. The maximum sampling rate is 400 MS/s and with an oversampling rate of 4×; the effective bandwidth is 50 MHz. Fig. 27 shows the measured FFT at 400 MS/s, indicating peak SNDR and SFDR of 70.4 and 88 dB, respectively. The rise in the noise floor at low frequency is mainly due to the flicker noise of the pre-amplifier and has a negligible contribution to the overall ADC resolution as the total bandwidth is high. Fig. 27 shows the comparison of the performance when the NS and the linearity enhancements are enabled and disabled. The ADC consumes 13 mW from a 1-V supply while running at 400 MS/s, where 1.9, 5.9, 1.2, and 4 mW are dissipated by the reference, the pre-amplifier, the other analog circuitry, and the digital circuitry, respectively, resulting in a Schreier FoM of 166.3 dB. The measured performance versus input amplitude and versus input frequency is presented in Fig. 28, showing a dynamic range (DR) of 71.7 dB.

In order to demonstrate the PVT robustness of the proposed design, we evaluate the performance of ten different devices without calibration. The results are shown in Fig. 29, where the average SNDR and SFDR exceed 69 and 84 dB, respectively.

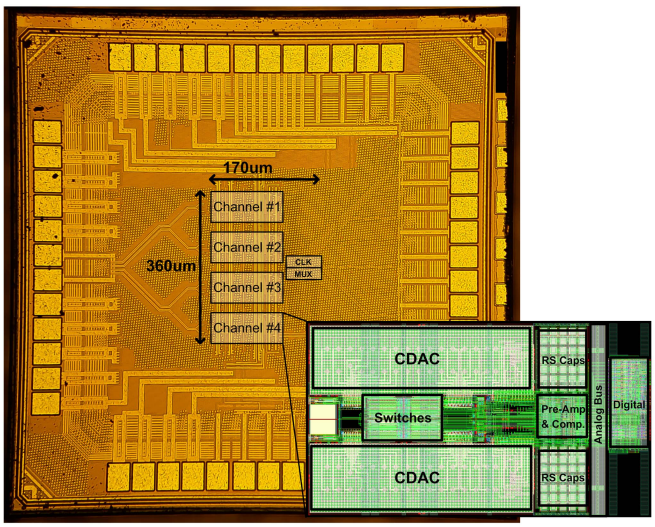

Fig. 30. Die photograph of the 40-nm CMOS prototype.

With a ±10% variation in the pre-amplifier supply voltage the measured SNDR varies by less than 0.3 dB. SNDR varies by less than 1.4 dB for a 0 °C–70 °C variation in temperature. Fig. 30 shows a die photograph. Table I provides

TABLE I
COMPARISON TABLE

	This work	[1]	[4]	[10]	[11]	[12]
Architecture	TINS-SAR	NS-SAR	NS-SAR	NS-SAR	CT-SD	CT-SD
Calibration Free	√	√	√	√	X	X
Technology (nm)	40	65	14	14	28	65
Area (mm^2)	0.061	0.0462	0.0021	0.0043	0.25	0.07
Supply Voltage (V)	1	1.2	0.9	1	1.16/1.5	1.4
Power (mW)	13.0	0.8	1.25	2.4	64.3	13.3
Sampling Rate (MS/s)	400	90	320	300	2000	6000
OSR	4	4	4	6	20	50
Bandwidth (MHz)	**50**	**11**	**40**	**25**	**50**	**60**
NTF Order	**4**	**1**	**1**	**1**	**4**	**4**
SNDR (dB)	**70.4**	**62.1**	**66.6**	**69.1**	**79.8**	**67.6**
SFDR (dB)	88.0	72.5	77.4	78	95.2	77.4
DR (dB)	71.7	-	-	72	82.8	76
FoM_S (dB)	166.3	163.3	171.7	169.3	168.7	164.1
FoM_W (fJ/conv-step)	48.1	35.8	8.9	20.6	80.5	56.5

a performance summary and compares with state-of-the-art, high-bandwidth NS ADCs, highlighting the advantages in bandwidth, high NTF order and also accuracy of the proposed TINS-SAR architecture compared to conventional NS-SARs.

VI. CONCLUSION

The new TINS-SAR architecture extends the bandwidth of the NS-SAR technique but retains the advantages of high resolution and energy efficiency. In contrast to other SAR ADCs that provide similar speed and accuracy (e.g., some of the data points in [6, Fig. 2]), this approach provides system-level methods to achieve this performance without calibration or sophisticated circuit optimization. Our design attains the highest bandwidth among NS-SAR ADCs and approaches the performance of state-of-the-art CT-SD ADCs.

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