## 20.3 A 50MHz-Bandwidth 70.4dB-SNDR Calibration-Free Time-Interleaved 4th-Order Noise-Shaping SAR ADC

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Noise-Shaping SAR (NS-SAR) is an emerging ADC architecture that offers both high resolution and high energy efficiency. State-of-the-art NS-SAR ADCs eliminate the need for op-amps, which relaxes design complexity and technology scaling issues. However, existing NS-SAR ADCs, with high FoM, are limited in bandwidth [1,2] (typically in the MHz range). This makes NS-SAR ADCs unsuitable for applications that need bandwidths in the tens of MHz range, such as wireless communications. Traditionally, high-bandwidth, high-resolution applications utilize pipeline or continuous-time sigma-delta (CT-SD) ADCs, but these architectures are much more power hungry than the NS-SAR. Thus, to increase the bandwidth of NS-SAR ADCs and extend their low-power advantages, this work presents a new time-interleaved noise-shaping SAR (TINS-SAR) architecture that enables higher bandwidth. Although time-interleaving of ADCs is difficult for high resolution, interleaving impairments can be avoided when combining interleaving with noise-shaping. Our prototype 40nm CMOS TINS-SAR ADC has a measured SNDR of 70.4dB for a 50MHz bandwidth without calibration. It consumes only 13mW and occupies 0.061mm$^2$, making it a potential substitute for CT-SD ADCs.

Interleaving of NS-SARs is inherently challenging for the following reasons: 1) inter-channel feedback greatly increases system complexity; 2) residues are not available at the beginning of each conversion, making existing NS-SAR design methods not applicable; and 3) noise from channel mismatch can be large enough to cause the system to become unstable. Our proposed TINS-SAR architecture solves these problems, with an error-feedback-based, multi-phase, noise-shaping method to implement interleaving, shown in Fig. 20.3.1. Major interleaving impairments due to channel mismatch [3] can be relegated to out-of-band noise as long as we choose an OSR greater than or equal to channel number N, or keep the bandwidth less than Fs/(2N).

In our 4× interleaved design, the SAR core of each channel operates in four phases (P1-P4), each of which quantizes a quarter of the bits (Fig. 20.3.1). Instead of feeding the CDAC residue at the end of the channel conversion, (i.e. Q4), back into the same channel for the next conversion, we feed this residue to all four channels at different phases. This feedback is scaled with different coefficients, A,B,C,D in Fig. 20.3.1. Utilizing the delay, related to interleaving, a 4th-order error-feedback structure is formed and any form of noise transfer function (NTF) with four zeros can be realized. At any point during operation, only one channel generates a residue and provides feedback. Therefore only one shared analog bus is needed to pass the residue to the other channels, keeping the routing simple.

Unlike previous work on non-interleaved error-feedback-based NS-SARs [1], a charge-sharing implementation cannot be applied to a TINS-SAR since charge-sharing changes the stored-charge on the CDAC, disturbing the next phase conversion. Instead, in this work, we realize residue summation with the multi-input, summing pre-amplifier, shown in Fig. 20.3.2. The four capacitors (C1-C4) at the pre-amplifier input sample the pre-amplifier outputs (i.e. residue) of each of the four channels. In order to sample the residue of the channel itself, an extra auxiliary capacitor (C5) is added to first sample the output of the pre-amplifier. Afterwards, this sampled value is passed to capacitor C4 by simple charge sharing. The attenuation from charge-sharing ($K_C$) is considered part of the feedback coefficient. The pre-amplifier sums the voltages on the CDAC and the four capacitors to form the input of the comparator. Equivalently, the residues from all four channels are "added" to the CDAC. By adjusting the gain ($G_{A\text{-}D}$) of each pre-amplifier input, any form of 4th-order NTF can be realized.

The pre-amplifier approach has two inherent advantages: 1) its gain suppresses the noise and offset of the comparator; 2) it provides effective isolation between the comparator and feedback capacitors, protecting them from any kickback noise. Although the noise from the pre-amplifier sampled on the feedback capacitors is not shaped, this noise is set by the capacitance value and can be made negligible through careful design.

The active pre-amplifier only requires a low gain and operates in open loop. Therefore, it is much more power efficient and more amenable to process scaling compared to an op-amp in a pipeline or CT-SD ADC. In our prototype, we use a single-stage, differential amplifier, which consumes only 1.5mW per channel. A typical concern with this type of open-loop amplifier is PVT variation. However, since the inputs of the pre-amplifier are built with layout-matched differential pairs and drive the same load (Fig. 20.3.2), the gain ratio between the different inputs is precise and independent to PVT variation. As the transfer function strongly depends on gain ratios ($G_{A\text{-}D}$), but only weakly depends on the common gain variation, K, the performance of this method is PVT stable and no calibration is needed.

Overloading is a potential problem in a TINS-SAR since the large out-of-band noise spurs, induced by channel mismatch, can easily overload the quantizer. We prevent this issue both at the architectural and system levels. At the architectural level, we use a 10b SAR core with 6 redundant bits (Fig. 20.3.3). In addition to protecting against overloading, the redundant bits also provide some extra tolerance for CDAC settling errors. At the system level, we set the zeros of the NTF to 0.5, as shown in Fig. 20.3.3, for the following three reasons: 1) unlike a conventional 4th-order NTF with zeros at 1, this modified NTF provides a flatter in-band noise floor which is better for low-OSR applications; 2) the proposed NTF has good tolerance to coefficient variation, and thus no calibration or tuning is needed; and 3) most importantly, the feedback values for the proposed NTF are much smaller than for a conventional NTF, further preventing the quantizer from overloading.

Since the pre-amplifier has relatively large input pairs, the parasitic capacitance ($C_{par}$ in Fig. 20.3.3) from the pre-amplifier input can cause noticeable distortion. To solve this, we add two extra switches ($S_{connect}$ and $S_{short}$) to isolate the CDAC and pre-amplifier. During the sampling phase, $S_{connect}$ is open and $S_{short}$ is closed, shorting the input of the pre-amplifier to Vcm, resulting in input-independent charge storage. Capacitor $C_n$ is added to limit the thermal noise from $S_{connect}$ and speed up settling. Bottom-plate sampling reduces the non-linearity caused by charge injection. To eliminate the effect of CDAC mismatch (~1%), dynamic element matching (DEM) shuffles the four MSBs in the CDAC. 23.4dB and 7.6dB improvements in SFDR and SNDR are observed, respectively, when all linearity enhancements are enabled.

Our prototype TINS-SAR ADC (Fig. 20.3.7) is fabricated in 40nm CMOS and has an active area of 0.061mm$^2$. Figure 20.3.4 shows the measured PSD at 400MS/s, with a peak SNDR and SFDR of 70.4dB and 88.0dB, respectively. Figure 20.3.4 also compares performance when noise-shaping and the linearity enhancements are enabled and disabled. With a 1V power supply, the ADC consumes 13mW at 400MS/s, where 1.9mW, 1.2mW, 5.9mW, and 4.0mW are dissipated by the reference, analog, pre-amplifier and digital circuitry, respectively, resulting in a Schreier FoM of 166.3dB. The measured performance vs input amplitude and vs input frequency are presented in Fig. 20.3.4. The measured dynamic range (DR) is 71.7dB. Figure 20.3.5 shows the measured performance of 10 devices. The average SNDR and SFDR exceed 69dB and 84dB without calibration. SNDR varies less than 0.3dB for a ±10% variation in pre-amplifier supply and 1.4dB for a 0-70°C variation in temperature. Figure 20.3.6 provides a performance summary and comparison with state-of-the-art, high-bandwidth NS ADCs. In conclusion, the new TINS-SAR architecture extends the bandwidth of the NS-SAR technique but keeps the advantages of high resolution and energy efficiency. Our design achieves a higher bandwidth among NS-SAR ADCs and approaches the performance of state-of-the-art, CT-SD ADCs.

*Acknowledgements:*
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*References:*
[1] S. Li, et al., "A 13-ENOB 2nd-order noise-shaping SAR ADC realizing optimized NTF zeros using an error-feedback structure," *ISSCC*, pp. 234-235, Feb. 2018.
[2] C.-C. Liu, et al., "A 0.46mW 5MHz-BW 79.7dB-SNDR Noise-Shaping SAR ADC with Dynamic-Amplifier-Based FIR-IIR Filter," *ISSCC*, pp. 466-467, Feb 2017.
[3] N. Kurosawa, et al., "Explicit formula for channel mismatch effects in time-interleaved ADC systems," *IEEE Instrumentation and Measurement Technology Conference*, pp. 763-768, vol.2, 2000.

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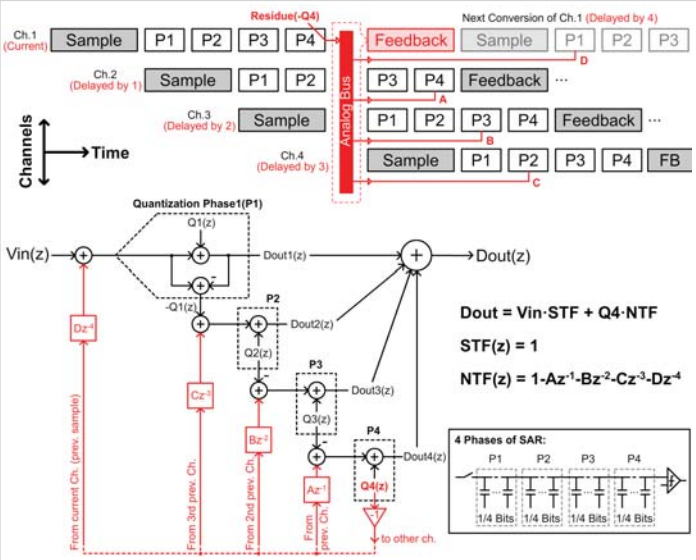


Figure 20.3.1: Interleaving sequence diagram and signal model diagram.

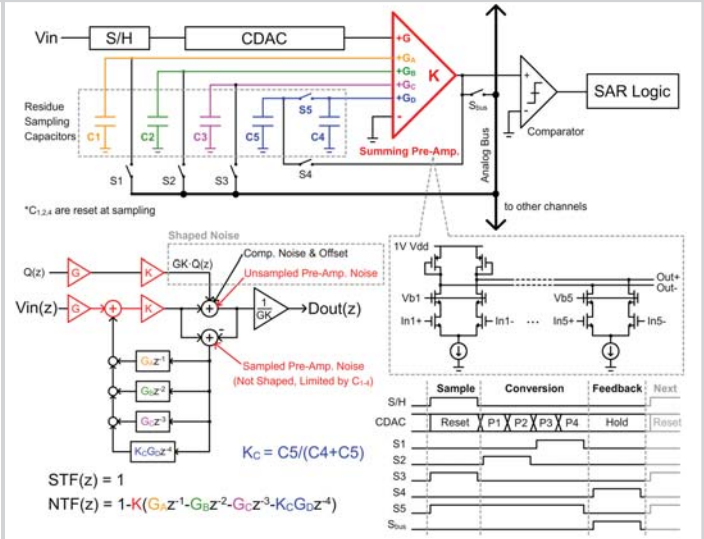


Figure 20.3.2: The proposed multi-input preamplifier realizing residue summation, the related signal model, and the feedback timing.

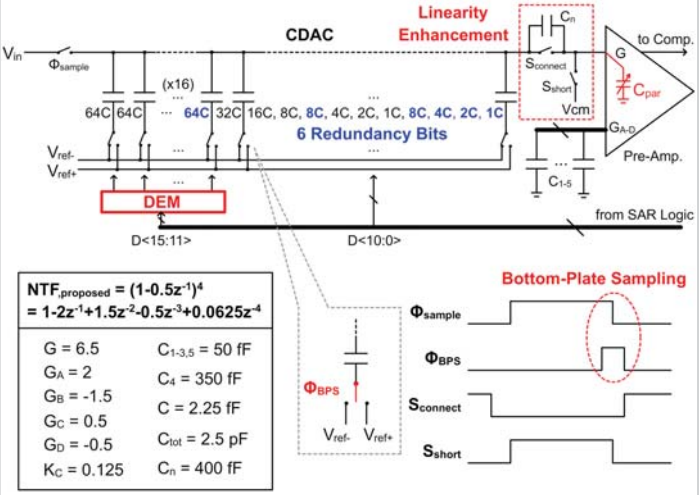


Figure 20.3.3: Details of the CDAC (single-ended) and the proposed linearity enhancements.

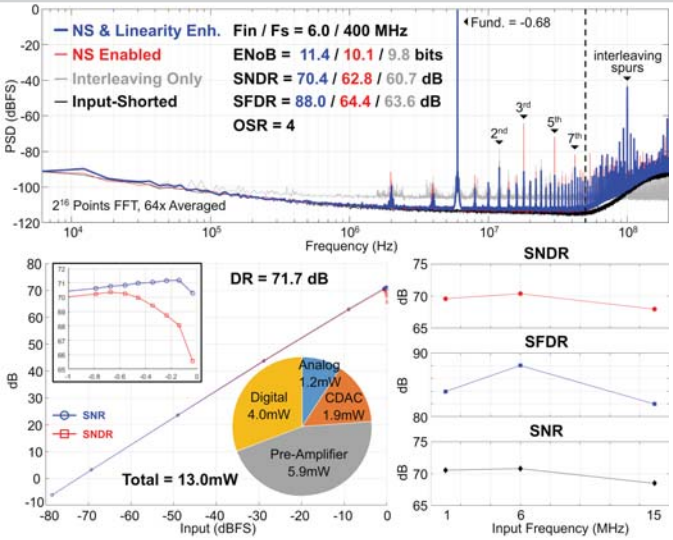


Figure 20.3.4: Measured output PSD (top), SNR/SNDR versus input power, power breakdown (left), and performance versus input frequency (right).

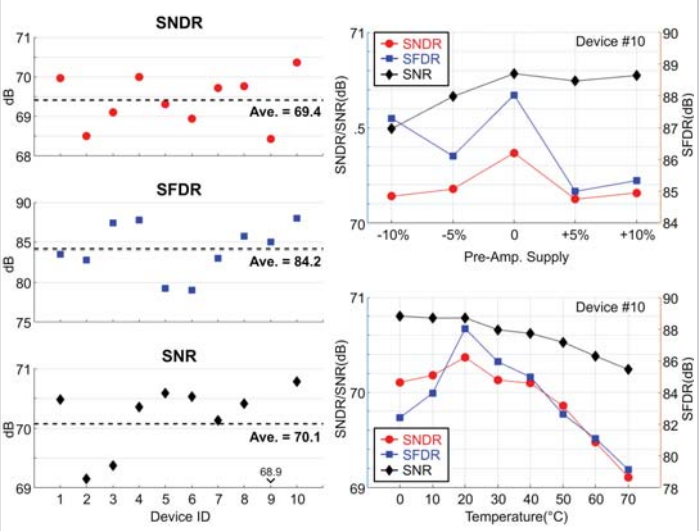


Figure 20.3.5: Measured performance of 10 devices (left), measured performance under supply voltage, and temperature variation (right).

| | This work | [1] | VLSI 17 Lin | ISSCC 12 Fredenburg | ISSCC 18 He | VLSI 16 Jain |
|---|---|---|---|---|---|---|
| Architecture | **TINS-SAR** | NS-SAR | NS-SAR | NS-SAR | CT-SD | CT-SD |
| Calibration Free | √ | X | √ | √ | X | X |
| Technology (nm) | **40** | 40 | **14** | 65 | 28 | 65 |
| Area ($mm^2$) | **0.061** | 0.024 | 0.0043 | 0.0462 | 0.25 | 0.07 |
| Supply Voltage (V) | **1** | 1.1 | 1 | 1.2 | 1.16/1.5 | 1.4 |
| Power (mW) | **13.0** | 0.084 | 2.4 | 0.8 | 64.3 | 13.3 |
| Sampling Rate (MS/s) | **400** | 10 | 300 | 90 | 2000 | 6000 |
| OSR | **4** | 8 | 6 | 4 | 20 | 50 |
| Bandwidth (MHz) | **50** | 0.625 | 25 | 11 | 50 | 60 |
| NTF Order | **4** | 2 | 1 | 1 | 4 | 4 |
| SNDR (dB) | **70.4** | 79 | 69.1 | 62.1 | 79.8 | 67.6 |
| SFDR (dB) | **88.0** | 89 | 78 | 72.5 | 95.2 | 77.4 |
| DR (dB) | **71.7** | 80.5 | 72 | - | 82.8 | 76 |
| $FoM_S$ (dB) | **166.3** | 178 | 169.3 | 163.3 | 168.7 | 164.1 |
| $FoM_W$ (fJ/conv-step) | **48.1** | 9 | 20.6 | 35.8 | 80.5 | 56.5 |

Figure 20.3.6: Performance summary and comparison with state-of-the-art high-bandwidth NS ADCs and CT-SD ADCs (last two columns).

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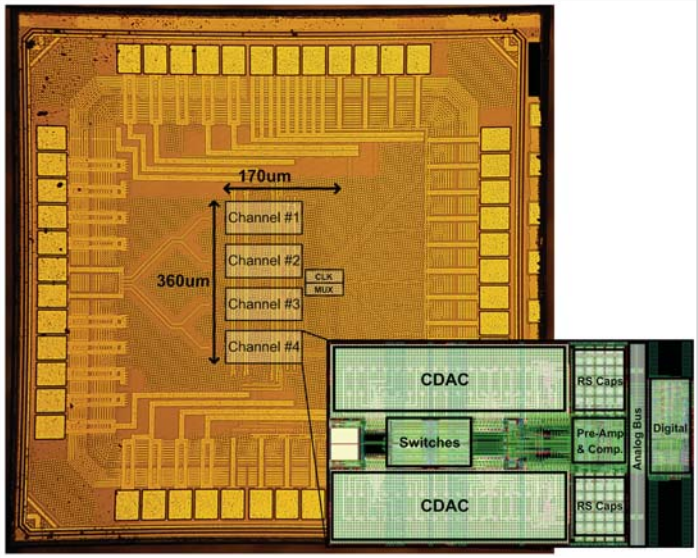


Figure 20.3.7: Die photo and zoomed-in layout of single channel.


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