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Design Considerations for Integrated Radar Chirp Synthesizers

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ABSTRACT Phase-locked loops (PLLs) effectively generate frequency chirps for frequency-modulated continuous-wave (FMCW) radar and are ideal for integrated circuit implementations. This paper discusses the design requirements for integrated PLLs used as chirp synthesizers for FMCW radar and focuses on an analysis of the radar performance based on the PLL configuration. The fundamental principles of the FMCW radar are reviewed, and the importance of low synthesizer phase noise for reliable target detection is quantified. This paper provides guidance for the design of chirp synthesizer PLLs by analyzing the impact of the PLL configuration on the accuracy and reliability of the radar. The presented analysis approach allows for a straightforward study of the radar performance and quantifies the optimal settings of a PLL-based chirp synthesizer for a given application scenario, while the developed methodology can be easily applied to other scenarios. A novel digital chirp synthesizer PLL design that meets the requirements of FMCW radar is presented. The synthesizer prototype fabricated in 65-nm CMOS drives a radar testbed to verify the effectiveness of the synthesizer design in a complete FMCW radar system.

INDEX TERMS Chirp linearity, chirp synthesis, frequency-modulated continuous-wave (FMCW) radar, fully-integrated chirp synthesizer, phase locked loop (PLL), phase noise, PLL bandwidth, radar testbed.

I. INTRODUCTION

Radar applications for driver assistance systems and autonomous vehicles have spurred the development of frequency-modulated continuous-wave (FMCW) radar [1]. FMCW radar relies on accurate frequency modulation of a continuously transmitted signal to measure target properties [2]. Unlike more traditional radar schemes that use pulses and operate in the MHz- or lower GHz-range, FMCW radar for the K- or W-bands offers lower power consumption and can be realized with much smaller form factors. Advances in silicon technology and the increasing demand for power-efficient, compact and low-cost high-frequency FMCW radar have motivated research on single-chip waveform synthesizers [3]–[5] and fully-integrated transceiver systems [6]–[8].

Fractional-N phase locked loops (PLLs) which digitally modulate the division ratio of the feedback divider are an effective tool for synthesis of FMCW. The performance requirements of the radar system, however, pose significant challenges and trade-offs for the design of PLL-based FMCW chirp synthesizers. With the assumption of linear chirps, FMCW radar determines target range and relative velocity from the frequency difference between transmitted and received signals, as described in detail in Section II. A key performance characteristic of the chirp synthesizer PLL is the phase noise. In an FMCW radar, the transmit signal is also used to down-convert the receive signal. The target properties are calculated from the low-frequency baseband signal resulting from the down-conversion. For slow to moderate-speed chirps, this baseband signal falls into the close-in phase noise region of the synthesizer. High phase noise levels reduce the signal-to-noise ratio (SNR) or may even mask the baseband signal. As discussed in detail in Section III, low close-in phase noise is crucial for high detection sensitivity of the radar.

The stair-step approximation of the chirp signal leads to trade-offs in the choice of the bandwidth of the PLL. Digital modulation of the feedback divider approximates the desired FMCW waveform as a sequence of discrete frequency levels with a certain stepping rate. On the one hand, the PLL must

exhibit settling behavior fast enough for the PLL output frequency to follow the modulation signal. This calls for a PLL loop bandwidth that is much larger than the chirp modulation frequency. On the other hand, the PLL bandwidth must be smaller than the stepping rate to ensure that the PLL does not output the stair-like approximation, which would result in degraded chirp linearity. For high chirp linearity and to guarantee accurate target detection, the PLL bandwidth must be carefully chosen for a given application scenario.

Previous works have studied synthesizer bandwidth and chirp non-linearity and to some extent their effects on the radar performance. Chirp linearity has been expressed as a function of synthesizer bandwidth by deriving the linearity based on a Fourier series [9]. However, this analysis does not consider the effect of digital modulation in a PLL-based synthesizer. Also, it does not provide insight into the quality of the radar as it is not conducted within the context of a complete radar system. Furthermore, the effects of sinusoidal non-linearities in the frequency chirp on the receiver baseband spectrum have been studied, but the non-linearities are not related to the synthesizer bandwidth and thus do not offer practical guidance for the design of a PLL-based synthesizer [10]. In this paper, we analyze PLL bandwidth and chirp linearity based on a model of a complete radar system. Our analysis incorporates a detailed model of a PLL-based chirp synthesizer and considers design aspects of the DSP backend as well. We examine the impact of the PLL bandwidth on the radar performance and quantify the upper and lower bounds of the PLL bandwidth, considering slow and fast chirp modulation. The presented modeling approach allows for a straightforward study of the radar accuracy and reliability as functions of the chirp parameters and the synthesizer PLL configuration.

Although general guidelines can be given regarding the design of an FMCW chirp synthesizer PLL, it is hard to evaluate synthesizer performance and provide design guidance without a specific application scenario. We choose the well-known 77GHz standard for long-range automotive radar (LRAR) to examine PLL requirements and analyze radar performance. The methodology developed in this paper can be easily applied to other scenarios. In the paper, we refer to component performance reported in the literature for integrated 77GHz radar systems listed in Table 1.

In addition, this paper presents a novel PLL-based chirp synthesizer implementation and describes an experimental setup to test the effectiveness of the synthesizer. While fully-integrated synthesizer PLLs can be implemented as analog or digital PLLs, analog implementations still dominate at high frequencies. Digital PLLs offer greater programmability and area efficiency, but suffer from performance limitations of conventional time-to-digital converters (TDCs), in particular poor time resolution, which severely limits the close-in phase noise of the PLL. This shortcoming of digital PLLs becomes even more pronounced with the wide loop bandwidths required for FMCW radar, as wide-loop-bandwidth PLLs allow more phase detector (or TDC) noise through to the PLL output. Binary TDCs (also referred to as bang-bang phase detectors) can be a useful alternative to address the resolution-power trade-off designers face with conventional TDCs, offering low power consumption thanks to their simplicity. A chirp synthesizer PLL using a binary TDC can be implemented with a two-point modulation (TPM) scheme for fast frequency modulation with a narrow PLL bandwidth. In fact, TPM has emerged as a popular approach to solve the trade-off between PLL bandwidth and phase noise [3], [5], but such PLL designs must apply calibration to address the gain mismatch between the modulation paths. We present a digital synthesizer implemented as a single-loop digital PLL that meets the conflicting requirement of low close-in phase noise and wide PLL bandwidth. This design succeeds by using a novel TDC architecture that combines a conventional analog phase-frequency detector (PFD) and charge pump with a continuous-time $\Delta\Sigma$ modulator.

TABLE 1. Component values for 77GHz radar scenario.

Quantity	Value
Transmitter output power P_T	11dBm [6]
Power amplifier gain G_{PA}	14dB [8]
Transmit and receive antenna gain G_T, G_R	20dBi [7], [8]
Low-noise amplifier gain G_{LNA}	17.5dB [7]

The paper is organized as follows: Section II begins with a theoretical discussion based on an overview of the principles of FMCW radar. Section III discusses the impacts of synthesizer phase noise. Section IV focuses on the loop bandwidth of an FMCW synthesizer PLL with an analysis supported by simulation results. Section V presents our novel PLL-based FMCW synthesizer design. Section VI describes a complete end-to-end radar testbed that demonstrates the effectiveness of the synthesizer architecture in a complete radar system. Section VII concludes the paper.

II. FMCW RADAR

An FMCW radar continuously transmits a signal whose frequency is linearly modulated during the measurement. The most commonly used chirp profiles are sawtooth and triangular profiles, as illustrated in Fig. 1. We observe a propagation delay between the transmitted and received signals due to the signal roundtrip. Further, the received signal frequency experiences a Doppler shift if the target is moving relative to the radar. The resulting offset frequency between transmitted and received signal is referred to as the beat frequency and represents a measure of target range and velocity. For a sawtooth profile (Fig. 1(a)), we can express the beat frequency as

$$f_b = \frac{2R\,BW}{c\,T} + f_d \tag{1}$$

where R denotes the target range, BW the chirp modulation bandwidth, c the speed of light, T the modulation period,

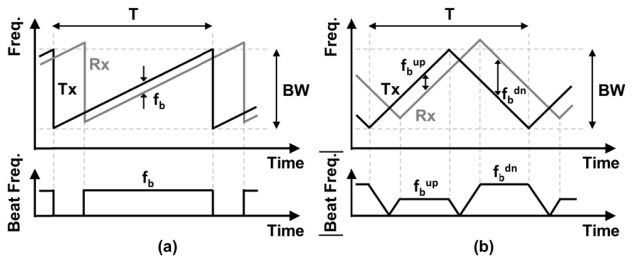


FIGURE 1. Sawtooth FMCW chirp (a) and triangular FMCW chirp (b).

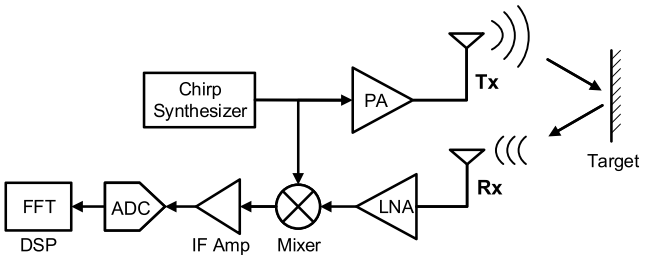


FIGURE 2. FMCW radar system.

and f_d the Doppler frequency [1]. To unambiguously resolve the range, R, and relative velocity, $v = cf_d/(2\,f_c)$, where f_c represents the center frequency of the waveform, a sequence of chirps with different ramp slopes can be generated.

Using a triangular waveform profile (Fig. 1(b)), however, we obtain two distinct beat frequencies (f_b^{up}, f_b^{dn}) from the up- and down-chirps and can unambiguously calculate range and velocity as [7]

$$R = \frac{c\,T}{4\,BW} \cdot \frac{f_b^{up} + f_b^{dn}}{2} \tag{2}$$

$$v = \frac{c}{2f_c} \cdot \frac{f_b^{up} - f_b^{dn}}{2} \tag{3}$$

High resolution in range and velocity measurements is critical for target separability. If we assume that the beat signal period is limited by the duration of the up- and down-chirps, then the minimum detectable beat frequency (and beat frequency difference) is $2/T$, and we can derive the range and velocity resolutions as

$$\Delta R = \frac{c}{2\,BW} \tag{4}$$

$$\Delta v = \frac{c}{2f_c\,T} \tag{5}$$

Accordingly, the radar requires a large modulation bandwidth for fine range resolution, whereas a longer period of the triangular chirp improves the velocity resolution. Although equations (4) and (5) describe the ideally achievable resolutions, the actual values are further limited by several factors including the overlap of the transmitted and received chirps due to the signal propagation delay, time gating to discard highly nonlinear chirp segments near the chirp turnaround points, and, most importantly, chirp non-linearity [9], [10].

A block schematic of a complete FMCW radar system is shown in Fig. 2. The chirp synthesizer generates the FMCW signal and a power amplifier (PA) feeds the synthesizer output signal to the transmit antenna. A receive antenna picks up the returned signal, which is then mixed with the synthesizer output to obtain the beat frequencies. The DSP back-end performs an FFT on the digitized baseband signal to determine the beat frequencies and calculates distance and velocity of the target.

To gain insight into the design challenges of the radar system, it is instructive to study the radar link budget. The receive power P_R of the transceiver is given as

$$P_R = \frac{P_T G_T G_R \sigma \lambda^2}{(4\pi)^3 R^4} \tag{6}$$

where P_T denotes the transmit power, G_T and G_R are the transmit and receive antenna gain, respectively, σ is the radar cross section (RCS), λ is the wavelength and R is the range of the target [11]. We evaluate (6) for a potential fully-integrated CMOS radar, assuming the LRAR scenario. The RCS of a mid-sized car varies greatly with the incident angle of the radar signal [1]. We assume an RCS of 30m^2 at the rear of the car [7]. Using 100m as a typical target range for LRAR, the specifications in Table 1 yield a receive power of -95dBm. Such a low power level makes it challenging to achieve a receive SNR that guarantees reliable target detection. For reliable detection with a low false-alarm rate, the SNR must exceed a certain threshold SNR. Values given in the literature vary and are in the range of 10 to 16dB [1], [11], requiring the noise floor to be at around -110dBm. Several noise sources contribute to the total noise at the receive back-end and include the phase noise from the chirp synthesizer, the low-noise amplifier (LNA) noise and the quantization noise of the analog-to-digital converter (ADC).

III. SYNTHESIZER PHASE NOISE

An FMCW radar system uses the transmit signal to down-convert the receive signal (Fig. 2). For slow and moderate chirp slopes, the beat frequencies typically fall into the close-in phase noise region of the synthesizer and may be masked by the phase noise. Moreover, in multi-target scenarios, reflected signal powers are likely to vary significantly and the phase noise reflected by targets with strong reflection may mask other targets. Low close-in synthesizer phase noise is therefore crucial for reliable target detection.

In a PLL, several noise sources contribute to the output phase noise. A basic block diagram of a fractional-N PLL used for triangular chirp generation is shown in Fig. 3. A PLL synchronizes the phase and frequency of its high-frequency output to a lower-frequency reference signal [12]. The voltage-controlled oscillator (VCO) generates the PLL output signal whose frequency is proportional to the tuning voltage at the VCO input. The frequency divider in

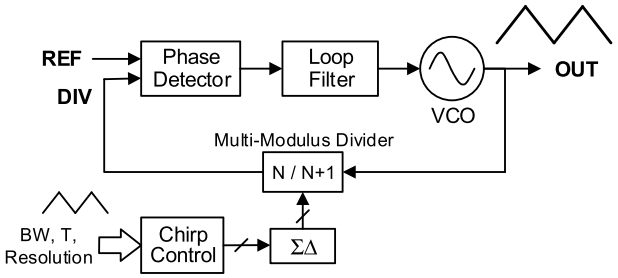


FIGURE 3. Fractional-N PLL with chirp control unit for FMCW chirp synthesis.

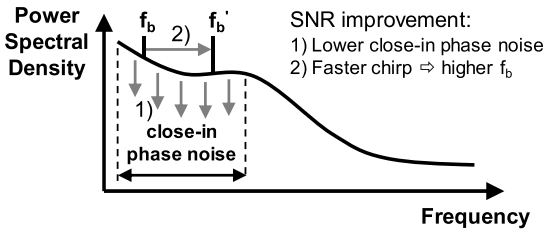


FIGURE 4. Noise spectrum at mixer output with beat frequency within close-in phase noise region.

the feedback path of the PLL divides the VCO output frequency, producing an output signal whose frequency is equal to (or during start-up at least close to) the PLL reference frequency. The phase detector (PD) measures the phase difference between the reference clock and the feedback signal. Finally, the loop filter stabilizes the feedback loop, smoothing the PD output and providing the tuning voltage for the VCO. Fractional division is accomplished by using a $\Delta\Sigma$ modulator to switch the division ratio of the programmable divider between different integer values so that the average value is equal to the desired fractional value [13].

Reference noise, phase detector noise, divider noise and $\Delta\Sigma$ quantization noise can be referred to the reference node of the PLL. The combined noise contribution at this node, which is typically dominated by the phase detector noise at low frequency offsets, is low-pass filtered by the PLL and determines the close-in phase noise. In contrast, the VCO noise is high-pass filtered and dominates the PLL phase noise at large frequency offsets. The amount of phase detector noise getting through to the PLL output increases with the PLL bandwidth, whereas more VCO noise is suppressed with a larger PLL bandwidth. Fast chirp modulation requires fast PLL settling behavior, which translates to a wide PLL bandwidth. Thus, low phase detector noise (i.e. highly accurate phase detection) is critical for low close-in phase noise.

The phase noise profile given in Fig. 4 shows a realistic phase noise characteristic with a plateau-like region at low and moderate frequency offsets as typically seen with wide-bandwidth PLLs and accounts for flicker noise (higher noise level at low offsets). As the location of the beat frequency suggests, lower close-in phase noise improves the SNR in the radar receiver. Although other potential measures such as higher amplification in the transmit PA or a high-gain LNA can provide some remedy, good close-in phase performance is imperative for the synthesizer in order to ensure reliable target detection.

The power of the receive signal at the mixer input equals the receive power P_R multiplied by the gain, G_{LNA}, of the LNA and must surpass the phase noise level $L(f_b)$ of the synthesizer [14]. Taking into account that a certain detection threshold SNR_{min} must be met, we can derive an estimate of the maximum close-in phase noise level according to

$$10 \cdot \log_{10} \frac{G_{PA} G_T G_R G_{LNA} \sigma \lambda^2}{(4\pi)^3 R^4} \geq L(f_b) + SNR_{\min} \qquad (7)$$

We again use the component values in Table 1 for the LRAR scenario and assume $SNR_{min} = 15dB$, $\sigma = 30m^2$ and $R = 100m$. In this case, (7) yields a maximum close-in phase noise level of -90dBc/Hz. Considering results reported in the literature [6], [7], this close-in phase noise is challenging to achieve at 77GHz.

However, we must note here that transmitter phase noise and receiver phase noise are in fact correlated, which is not accounted for by (7). Since the receive signal is mixed with the transmit signal, this noise correlation cancels phase noise, thus relaxing the phase noise requirement and increasing the sensitivity of the radar. The effectiveness of the cancellation depends on the target range as well as the frequency offset. Reference [15] investigates the effect of range correlation on the baseband (or IF) spectrum by formulating the baseband spectrum as a combination of the transmitter phase noise spectrum, scatterer spectra and range correlation effects. The residual phase noise present after mixing in the baseband signal can be expressed as $\Delta\Phi(t) = \Phi(t - t_d) - \Phi(t)$, where $\Phi(t)$ describes the transmitter phase noise and t_d is the round-trip propagation delay of the radar signal. To quantify the phase noise cancellation, [15] derives the baseband phase noise spectrum as

$$S_{\Delta\Phi}(f, R) = S_{\Phi}(f) \cdot [4 \sin^2(2\pi R f / c)] \qquad (8)$$

where $S_{\Phi}(f)$ is the phase noise spectrum of the transmitter. From the term in square brackets in (8), we can see that the noise cancellation is more effective for low frequency offsets and for close targets. As an example, for a 100kHz offset, the phase noise attenuation is $-27.6dB$ for $R = 10m$ and $-7.6dB$ for $R = 100m$, respectively. Fig. 5 shows the attenuation as a function of the frequency offset for $R = 10m$ and $R = 100m$. Clearly, range correlation significantly reduces the low-frequency phase noise components in the baseband spectrum. Therefore, we can think of (7) as giving a pessimistic upper bound for the required phase noise performance. Finally, we can use (8) to study the influence of phase noise on the system performance while taking noise cancellation into account. This is done in [16], which calculates the rms phase error of the baseband signal based on (8) and uses this result to derive a lower bound for the uncertainty in the range measurement. However, the ranging uncertainty shown in [16] for a LRAR scenario is less than 1cm, which can be considered negligible.

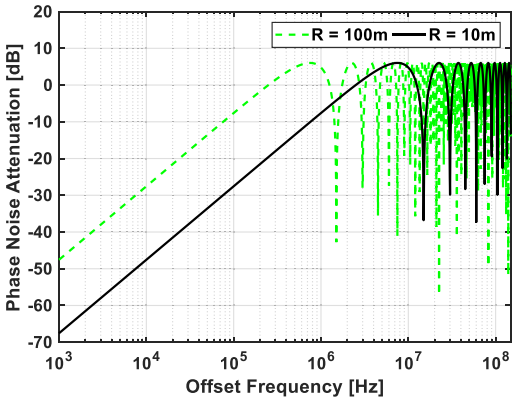


FIGURE 5. Attenuation of baseband phase noise due to noise cancellation as a function of frequency offset for R = 10m and R = 100m.

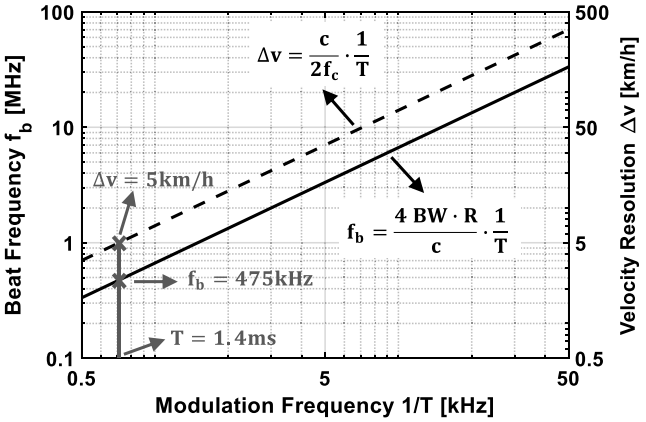


FIGURE 6. Beat frequency and velocity resolution as functions of the modulation frequency for BW = 500MHz, f_c = 77GHz and R = 100m.

To improve the baseband SNR, we can generate faster chirps, that is chirps with a higher slope, resulting in higher beat frequencies for the otherwise same radar scenario. As suggested in Fig. 4, this may push the beat frequencies into a region of lower phase noise. It should be noted, however, that the close-in phase noise of an analog charge-pump PLL may increase significantly if fast chirps are generated [17]. This is because fast chirps result in a large static phase error at the phase detector and thus a large charge pump duty cycle. The average duty cycle can be derived as

$$\alpha_{CP} = \frac{C\ BW}{I_{CP}\ K_V\ T_S} \tag{9}$$

where C is the loop filter capacitance, I_{CP} is the charge pump current, K_V is the VCO gain and T_S is the sweep time. It can be shown that there is an optimum charge pump duty cycle that minimizes the close-in phase noise [17]. Therefore, the PLL parameters (i.e. C and I_{CP}) should be adjusted for faster chirps. Accordingly, [17] suggests having a programmable loop filter capacitance to enable phase noise optimization for a given charge pump current and chirp slope.

We can generate faster chirps by reducing the chirp modulation period. According to (5), however, a shorter modulation period reduces the velocity resolution of a radar system using a triangular chirp profile. In theory, we could also achieve a higher chirp slope by increasing the modulation bandwidth of the chirp (and hereby also improve the range resolution), but the output frequency range of integrated PLLs is typically critically limited by the VCO tuning range, and therefore this measure is impractical. For example, increasing the chirp slope by one order of magnitude by increasing the chirp bandwidth is usually not possible, whereas doing so by decreasing the modulation period may be feasible provided that the PLL bandwidth is sufficiently large.

The trade-off between increased chirp slope and reduced velocity resolution must be carefully considered for the specific application scenario. Fig. 6 shows beat frequency and velocity resolution as functions of the modulation frequency for the LRAR scenario. We can see that a reasonable resolution of 5km/h corresponds to a rather low beat frequency of 475kHz. Fast chirps can realistically produce beat frequencies well in the megahertz range in this scenario, but also result in unacceptably coarse velocity resolution. In this case, if velocity detection is desired, alternative ways of extracting the velocity information must be explored and applied, for example, velocity calculation based on consecutive range measurement results.

IV. LINEARITY AND PLL BANDWIDTH ANALYSIS

FMCW radar is based on the premise that the frequency chirps are perfectly linear so that the beat frequencies accurately represent the parameters of the detected targets. An optimized PLL bandwidth is key to achieving high chirp linearity. The PLL division ratio (Fig. 3) approximates the chirp waveform with a stair-like signal. This modulation is discrete in time and output value. The PLL bandwidth must be large enough for the PLL to follow the trajectory of the ideal linear chirp profile, requiring a bandwidth far greater than the chirp modulation frequency. At the same time, PLL settling must not be so fast that the PLL output frequency follows the stepped modulation signal too closely. This requires a PLL bandwidth less than the stepping rate[1] of the modulation signal. Consequently, an optimized loop bandwidth satisfies the following inequalities:

$$\frac{1}{T} \ll BW_{PLL} < \frac{2^{lin} - 1}{T/2} \tag{10}$$

Here, we assume the modulation signal comprises 2^{lin} output quantization levels, and the stepping rate is described as a function of the chirp resolution denoted by *lin* in bits. In the following analysis, we quantify the inequalities in (10) for a triangular chirp profile and examine the impact of the PLL bandwidth on the detection reliability and accuracy. For this purpose, we develop a Simulink-based model of a charge-pump PLL.

[1]The stepping rate refers to the rate at which the digital modulation signal controlling the PLL division ratio is updated.

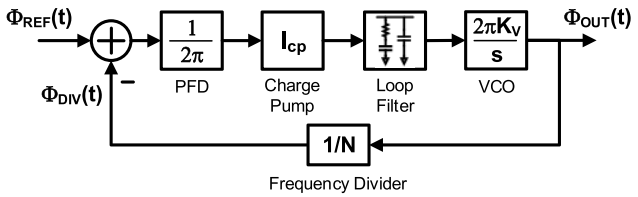


FIGURE 7. Phase-domain PLL model.

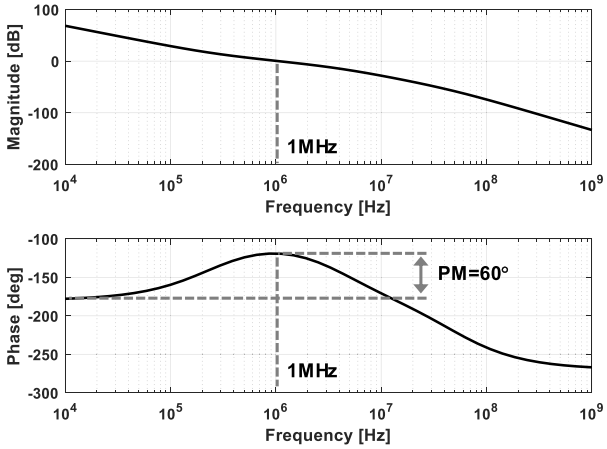


FIGURE 8. Bode plot of the loop gain for a 1MHz loop bandwidth.

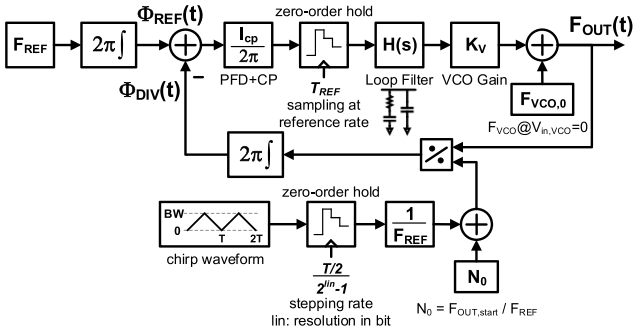


FIGURE 9. Phase/Frequency-domain model of an FMCW chirp synthesizer.

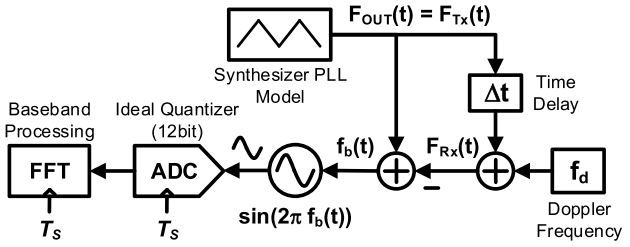


FIGURE 10. Model of an FMCW radar system with chirp synthesizer model.

A. MODEL AND SIMULATION SETUP

In preparation for the PLL bandwidth analysis, we utilize a simple phase-domain model of an analog type-II PLL (Fig. 7) to first determine the PLL configuration (i.e. charge pump current, loop filter component values) for different bandwidths extending from 100kHz to 10MHz. The chosen PLL settings ensure loop stability with 60° phase margin. As an example, Fig. 8 shows the magnitude and phase of the loop gain for a loop bandwidth of 1MHz. Throughout our analysis, we assume a 500MHz PLL reference, a 77GHz PLL output in accordance with the LRAR scenario, and a VCO gain of 1GHz/V.

A time-domain model of a fractional-N PLL for chirp generation simulations would result in long simulation times because the PLL output period and the chirp modulation period differ by several orders of magnitude. For phase noise simulations, efficient computation is possible if simulations are performed in the IF domain. The simulation approach in [18] avoids computations in the RF domain by generating the spectrum of the baseband phase noise (which is referred to as decorrelated phase noise) from the phase noise spectrum of the transmitter while taking noise cancellation effects into account. To allow fast simulation for our PLL bandwidth and chirp linearity analysis, our Simulink-based synthesizer model (Fig. 9) does not operate in the time domain, but in the phase/frequency domain. The output signal of the model represents the PLL output frequency. Reference phase and feedback phase are obtained by integrating the constant reference frequency and the feedback frequency, respectively. A zero-order-hold element in the forward path models the update of the charge pump output at reference rate. In a similar manner, a zero-order-hold element samples a continuous chirp waveform signal in the time and value domains to produce a stair-like modulation signal with the desired stepping rate.

We employ the synthesizer model as a subsystem in a Simulink-based FMCW radar system model (Fig. 10). The system model uses a delay block to model the roundtrip propagation delay of the radar signal, and adds a frequency shift to account for a Doppler effect due to a moving target. The mixing operation in the receive path is modeled by subtracting the receive frequency signal from the synthesizer output, resulting in a signal that represents the beat frequency. To reflect the baseband processing of a real transceiver system, an oscillator block generates a signal with its instantaneous frequency being equal to the obtained beat frequency. An ideal quantizer converts the IF signal to the digital domain before an FFT is performed on the signal.

B. APPROACH FOR RESULT EVALUATION

In our linearity analysis, we modify the chirp modulation period T to implement varying chirp slopes. $T_{S,FFT} = N/F_S$ denotes the time required to collect N data points for an N-point FFT with sample rate $F_S = 1/T_S$. $T_{S,FFT}$ should be as large as possible (ideally equal to the chirp duration $T/2$) to achieve best beat-frequency resolution. Therefore, we adapt F_S to the modulation period used in each case. Since the greatest linearity errors of a triangular chirp occur at the turnaround points, time gating can be applied to block these non-linear portions of the chirp from being processed by the FFT [9]. Accordingly, we have $T_{S,FFT} = m \cdot T/2$, where m denotes the time gating factor ($m < 1$). For the minimum

resolvable beat frequency, we obtain[2]

$$\Delta f_b = \frac{F_S}{N} = \frac{1}{T_{S,FFT}} = \frac{2}{m \cdot T} \tag{11}$$

Using (2) and (4), we obtain the minimum resolvable range resolution from (11) as

$$\Delta R = \frac{c\,T}{4\,BW} \cdot \Delta f_b = \frac{1}{m} \cdot \frac{c}{2\,BW} = \frac{1}{m} \cdot \Delta R_{ideal} \tag{12}$$

Clearly, time gating somewhat coarsens the range resolution for the sake of better effective chirp linearity. We choose $m = 90\%$ in our analysis to process only the inner 90% of each chirp ramp. Regarding the number of FFT points, N, we use a large enough N to ensure the unambiguous detection of the maximum beat frequencies by satisfying the Nyquist criterion $F_S > 2f_{b\_max}$. With $F_S = N/T_{S,\mathrm{FFT}}$ and $T_{S,FFT} = m \cdot T/2$, we can use (2) to reformulate this inequality as

$$N > m \cdot \frac{4\,BW}{c} \cdot R_{max} \tag{13}$$

We use a modulation bandwidth of 500MHz in the analysis, which, according to (4), offers an appropriate range resolution of 0.3m for the LRAR scenario. Since we assume a realistic maximum target range of 200m, we use $N = 2^{11} = 2048$ in this work.

Before trying to quantify (10), it is instructive to take a look at the generated chirp waveforms in Fig. 11 for optimized and non-optimized PLL bandwidths. If the PLL bandwidth is too small (Fig. 11(a)), the generated chirps clearly show poor linearity, impeding accurate detection. If the PLL bandwidth is too large (Fig. 11(c)), the output waveform follows the stair-like modulation signal too closely and the associated non-linearity results in spurious peaks in the FFT spectrum, increasing the risk of detection of ghost targets. An optimized PLL bandwidth (Fig. 11(b)) offers the best chirp linearity.

If we assume that the radar utilizes the beat frequencies resulting from both up- and down-chirps to calculate the target velocity using (3), the velocity resolution required for the application scenario dictates the minimum modulation period of the triangular chirp, as stated by (5). For the LRAR scenario, we assume $\Delta v = 5km/h$ as a sufficient performance parameter, corresponding to $T = 1.4ms$. This is to be considered a slow modulation signal and does not present a challenge to the left half of (10). However, we must choose a small enough PLL bandwidth combined with a sufficiently large number of quantization levels in the modulation signal to ensure the right half of (10) is satisfied. In section *C*, we quantify the right half of (10), using a long modulation period of 2ms. In section *D*, we then focus on fast modulation signals.

[2]The frequency resolution can be improved by using interpolation between FFT bins [19]. We apply this in the radar testbed described in Section VI.

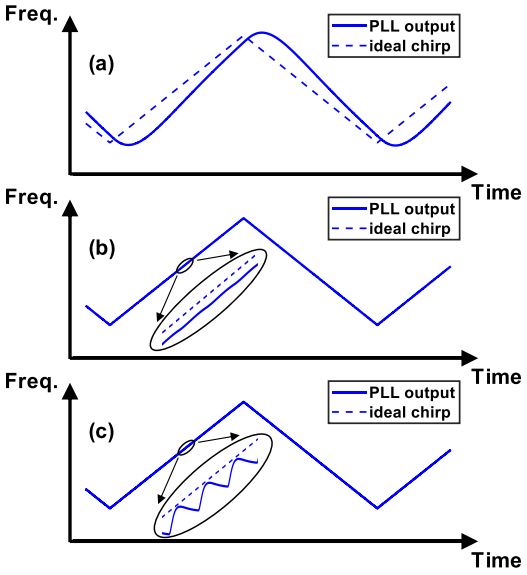


FIGURE 11. Simulated synthesizer output waveforms for too small BW_{PLL} (a), optimized BW_{PLL} (b), and too large BW_{PLL} (c).

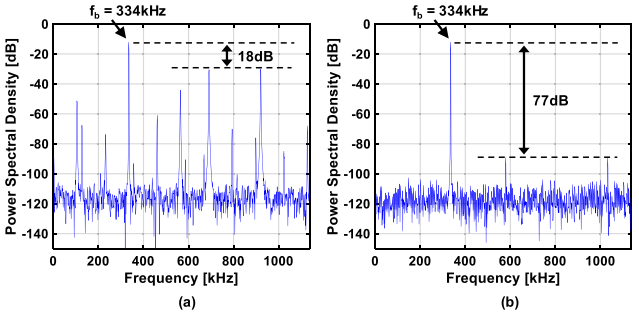


FIGURE 12. FFT spectra for $BW_{PLL} = 1MHz$, T = 2ms, R = 100m, v = 0km/h, and stepping rates of 1.0MS/s (10bit resolution) (a) and 8.2MS/s (13bit resolution) (b), respectively.

C. ANALYSIS FOR SYNTHESIS OF SLOW CHIRPS

A rather low PLL bandwidth and a large resolution of the stair-like modulation signal are critical for the radar performance if we generate slow chirps. This scenario is the subject of the first part of our analysis. Too large a PLL bandwidth can significantly degrade the chirp linearity, as we have seen in Fig. 11(c). The observed non-linearity in the output waveform translates to spurious peaks in the FFT spectrum [10]. As an example, Fig. 12 shows the simulated FFT spectra for the radar system model of Fig. 10 for a PLL bandwidth of 1MHz and two different chirp modulation stepping rates. For a stepping rate of 1MS/s, the right half of (10) is not sufficiently satisfied, and as a result, there are numerous spurious peaks in the spectrum (Fig. 12(a)), degrading the spurious-free dynamic range (SFDR) to be only 18dB. In contrast, a stepping rate of about 8 times the PLL bandwidth greatly reduces the spur levels and yields a high SFDR of 77dB (Fig. 12(b)). If we increase the stepping rate even further, spurious peaks due to chirp non-linearity eventually disappear altogether and the SFDR approaches an upper limit of around 95dB.

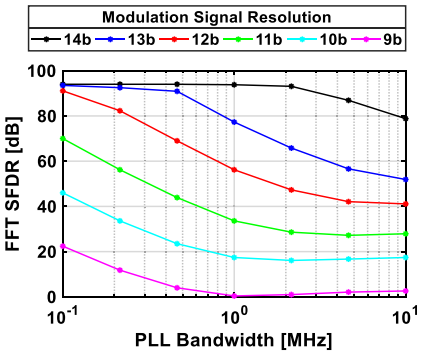


FIGURE 13. SFDR in FFT spectrum as a function of PLL bandwidth and chirp modulation resolution for T = 2ms.

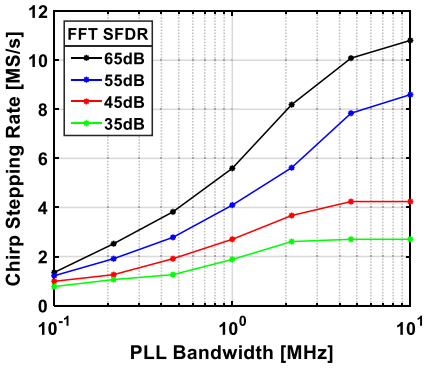


FIGURE 14. PLL bandwidth vs. stepping rate characteristic for constant SFDRs and T = 2ms.

For a given FMCW radar system and application scenario, it can be seen from (6) that the receive signal power depends on the RCS of the target as well as on the target range. According to the RCS diagram in [1], the RCS can vary up to about 30dB around the rear of a car. Moreover, if we assume a target range from 80m to 150m, the receive signal power varies up to an additional 11dB. Because of this combined receive-power variation of more than 40dB, we require a minimum SFDR margin that allows us to distinguish beat frequencies from spurious peaks. In the following, we use an SFDR margin of 45dB that we associate with sufficient chirp linearity.

We sweep the PLL bandwidth from 100kHz to 10MHz and the modulation signal resolution from 9 bits to 14 bits, while using a chirp bandwidth of 500MHz and a modulation period of 2ms. In all these cases, the radar model correctly resolves the target range (R = 100m) within ΔR = 0.3m and the target velocity (v = 10km/h) within Δv = 5km/h. Simulation results in Fig. 13 show the FFT SFDR as a function of the PLL bandwidth for varying modulation resolution, i.e. different stepping rates. For a given PLL bandwidth, the SFDR is significantly worse for lower modulation resolution because the PLL output follows the stair-like modulation signal more closely. The SFDR decreases for the same reason if we increase the PLL bandwidth and keep the modulation resolution constant. For lower resolutions, however, the SFDR levels off at high PLL bandwidths because there is no significant degradation in chirp linearity anymore beyond a certain PLL bandwidth. Also, the SFDR is upper-limited by the noise floor. No noteworthy spurs appear in this case and the upper limit of the SFDR is approximately 95dB.

The above results provide guidance for the optimal choices for PLL bandwidth and modulation resolution. In general, SFDR is best with low PLL bandwidths for slow chirp modulation. However, it should be taken into account that the beat frequency is only about 300kHz in our given scenario, and it is advisable to choose a PLL bandwidth larger than that to limit VCO noise. With a lower PLL bandwidth, the close-in phase noise of the PLL may be too high as too much VCO noise contributes to the PLL output phase noise. Fig. 13 suggests that a PLL bandwidth of around 1MHz and a modulation resolution of at least 12bit (which corresponds to a stepping rate of 4.1MS/s with T = 2ms) are an appropriate design choice for the given scenario.

A similar perspective is provided by Fig. 14, which illustrates the relationship between PLL bandwidth and chirp stepping rate for constant SFDR values. Again it can be seen that a higher PLL bandwidth requires a higher stepping rate for the same SFDR, i.e. to maintain the chirp linearity, and that the SFDR results tend to level off for high PLL bandwidths. Taking 45dB as the minimum required SFDR, we can conclude that a chirp stepping rate exceeding the PLL bandwidth by a factor of 3 to 6 sufficiently satisfies the right half of (10) for the given scenario. As pointed out above, the close-in phase noise performance of the synthesizer must be taken into account as, in practice, this may set a lower bound for the PLL bandwidth.

D. ANALYSIS FOR SYNTHESIS OF FAST CHIRPS

In the second part of our analysis, we examine the radar performance in the case of fast chirps and focus on the left half of (10). Fast FMCW chirps result in higher beat frequencies that are potentially located outside the close-in phase noise region of the synthesizer. However, considering (5), a triangular chirp radar cannot provide reasonable velocity resolution with fast chirps, and one must resort to different approaches for velocity estimation. For this reason, we only consider the accuracy of the range detection as we use the radar model to generate fast chirps and evaluate the radar performance. Again, we use a modulation bandwidth of 500MHz and a target range of 100m. Since the results for the target range are not affected by the target velocity, we set the target velocity to zero. We calculate the rms linearity frequency error from the difference between the synthesizer output waveform and an ideal linear fit while discarding the vicinity of the turnaround points, and express the chirp non-linearity as a percentage of the chirp modulation bandwidth [9].

Fig. 15 shows the chirp non-linearity for varying PLL bandwidths and chirp modulation frequencies. Clearly, fast chirp modulation combined with a low PLL bandwidth results in poor chirp linearity because the PLL is not fast enough to follow the trajectory of the ideal chirp profile

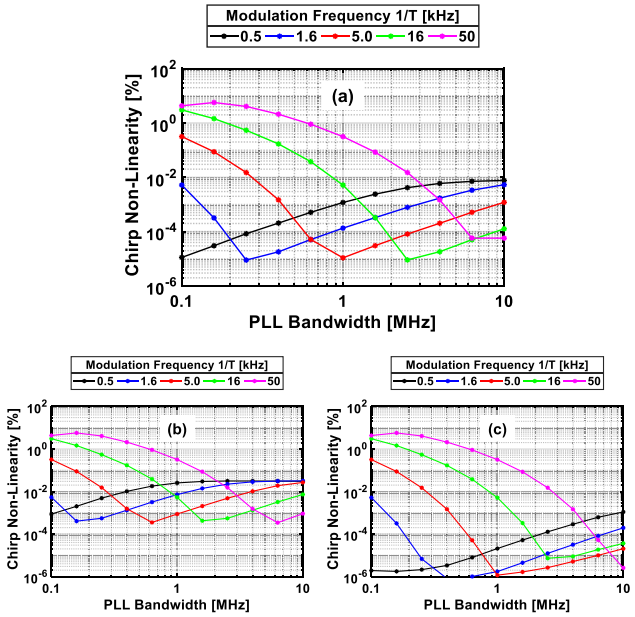


FIGURE 15. Chirp non-linearity as a function of PLL bandwidth and modulation frequency for a modulation resolution of 12bit (a), 10bit (b), and 14bit (c).

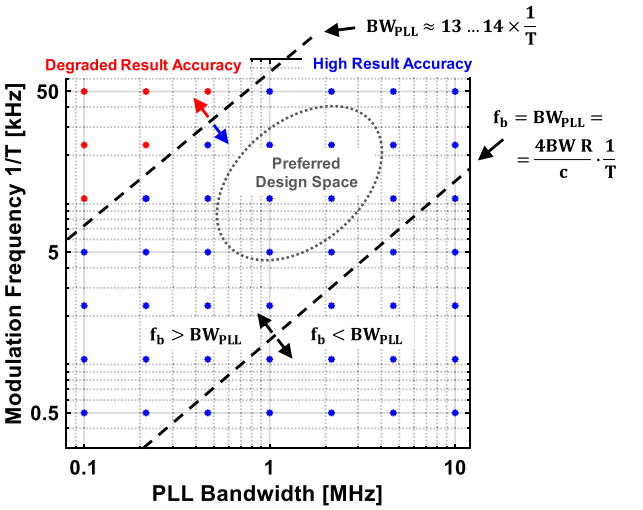


FIGURE 16. Result accuracy in the modulation frequency vs. PLL bandwidth design plane for BW = 500MHz and R = 100m.

(Fig. 11(a)). Moreover, the chirp linearity degrades as the PLL bandwidth becomes very large, increasing the tendency of the PLL to approximate the stair-like modulation signal. Consequently, there is an optimum bandwidth that minimizes the chirp non-linearity. As we would expect from (10), this optimum bandwidth increases with the chirp modulation frequency. Comparing the plots in Fig. 15, we also observe an increase in the optimum PLL bandwidth with the modulation resolution. In addition, the minimum chirp non-linearity greatly improves with the modulation resolution, suggesting the use of a very high stepping rate. However, this result may not accurately reflect a real design scenario as the modeled radar system is noiseless for the sake of simplicity. Also, it should be noted that the best linearity results suggested by Fig. 15(c) exceed the chirp linearity typically required in practice.

As we evaluate the detection accuracy of the radar, we can identify one half of the modulation frequency vs. PLL bandwidth plane that provides a degraded result accuracy (Fig. 16), i.e. the detected target range deviates from the actual range of 100m by more than the range resolution of 0.3m. In this half-plane of the entire design space, the chirp modulation is too fast for the given PLL bandwidth, resulting in poor chirp linearity and beat frequencies that do not accurately represent the target range. The red dots in Fig. 16 mark individual simulated range results with degraded result accuracy. In contrast, the blue dots mark range results that are within the range resolution. The boundary of the two half-planes allows us to quantify the left half of (10). Accordingly, (10) is sufficiently satisfied if the PLL bandwidth exceeds the modulation frequency by a factor of at least 14. For larger factors, however, we can expect more reliable results. At the same time, the PLL bandwidth should be chosen smaller than the beat frequency expected for the given LRAR scenario to take advantage of the fact that fast chirps result in beat frequencies outside the close-in phase noise. With this in mind, we can define a recommended or preferred design space in the plane in Fig. 16, offering both accurate detection results and high beat frequencies. Also, we place this design space around the 1-to-2MHz bandwidth range as a compromise between sufficient VCO phase noise suppression and uncommonly large PLL bandwidths.

V. DIGITAL PLL DESIGN FOR FMCW CHIRP GENERATION

The promise of small, power- and cost-efficient radar solutions has sparked intensive research efforts on PLL-based CMOS synthesizers for FMCW radar over the years. Since FMCW radar requires both fast PLL settling and low close-in phase noise, design approaches need to address these conflicting requirements. The vast majority of high-frequency PLLs are still implemented as analog PLLs, but analog implementations tend to occupy a large chip area, offer limited reconfigurability and are sensitive to temperature and process variations. Digital PLL implementations promise to overcome these shortcomings. However, digital PLLs rely on high-resolution TDCs for low close-in phase noise. The performance of conventional TDCs remains a serious bottleneck for achieving low phase noise with high-frequency digital PLLs, especially if a wide loop bandwidth is desired. Existing high-frequency digital chirp synthesizer PLLs apply two-point modulation to circumvent the trade-off between large loop bandwidth and low close-in phase noise, but depend on calibration [3], [5]. We present a calibration-free digital chirp synthesizer PLL design that overcomes this challenge and offers low close-in phase noise with wide loop bandwidths $>$1MHz by using a 3rd-order noise-shaping TDC. Loop bandwidths up to a few megahertz are typically sufficient for common radar scenarios (Fig. 16). The PLL architecture

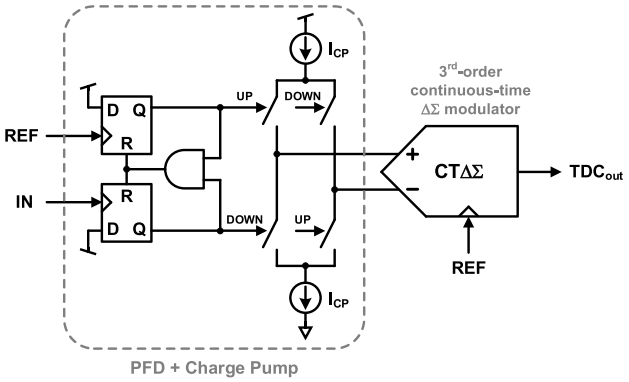


FIGURE 17. Two-step architecture of 3rd-order noise-shaping TDC [20].

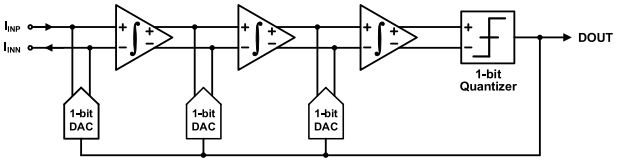


FIGURE 18. Continuous-time 3rd-order feedback architecture of modulator [20].

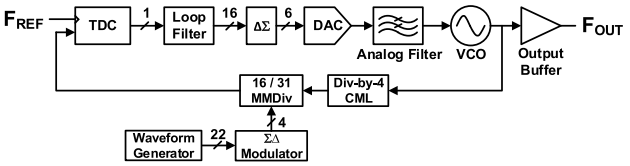


FIGURE 19. Block schematic of the digital 20GHz chirp synthesizer.

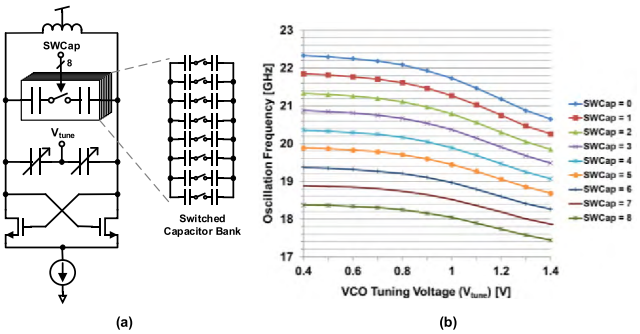


FIGURE 20. VCO schematic (a) and measured frequency tuning characteristic (b).

including the TDC design is a direct adaptation of the work in [20]. In Section VI, we present an experimental setup to test the effectiveness of our synthesizer in a complete radar system and we verify some of the findings from Section IV C.

The noise-shaping TDC implements a two-step approach to time-to-digital conversion (Fig. 17) [20]. The first stage of the TDC is a conventional PFD with a charge pump and takes advantage of the high accuracy offered by this common analog approach to phase detection. This first stage measures the phase difference between the input signal and the TDC clock and provides the result in the form of a differential pulse-width-modulated output current signal. The measured phase difference is given in the dc component (or average value) of the signal. The second TDC stage is a 3rd-order continuous-time $\Delta\Sigma$ modulator and converts the output current pulses of the charge pump to an oversampled noise-shaped 1-bit digital signal. The modulator essentially extracts the average of the analog pulsed-current input while shaping the quantization noise to high frequencies. This way the TDC retains the high accuracy of its first stage and achieves low noise in the band of interest at low frequencies. The shaped out-of-band quantization noise of the TDC is low-pass filtered by the PLL. A digital PLL using this noise-shaping TDC achieves a close-in phase noise similar to that of an analog PLL while offering the advantages of a digital PLL implementation such as area efficiency and reconfigurability.

A block schematic of the 3rd-order continuous-time $\Delta\Sigma$ modulator is shown in Fig. 18 [20]. The modulator is implemented as a 3rd-order modulator to achieve high TDC resolution in the band of interest. It is designed as a distributed-feedback architecture to avoid peaking in the signal transfer function, which improves the spur performance of the PLL. In addition, the single-bit quantizer helps avoid spurs in the PLL output spectrum during fractional-N operation due to its inherent linearity. Details on the circuit implementation of the modulator and measurement results of the TDC can be found in [20].

We implement the digital chirp synthesizer as a single-loop type-II fractional-N PLL (Fig. 19). It uses an external 250MHz reference and generates both a 20GHz output and a divided-down 5GHz output. The digital loop filter of the PLL consists of an accumulator and a digital filter stage introducing a pole-zero pair to stabilize the loop. In each reference cycle, the accumulator increases or decreases its value by the accumulator gain, depending on the 1-bit TDC output. The loop filter parameters are programmable and the accumulator gain serves as a convenient tuning knob to adjust the loop bandwidth of the PLL. A $\Delta\Sigma$ digital-to-analog converter (DAC) converts the filter output to the analog domain and delivers it to the tuning node of the VCO. The VCO is implemented as an LC-oscillator with a tail current source and incorporates capacitive tuning banks for coarse tuning of the VCO oscillation frequency (Fig. 20). The feedback divider consists of a divide-by-4 current-mode-logic stage and a 16-to-31 multi-modulus frequency divider. A 2nd-order $\Delta\Sigma$ modulator generates the control words for the multi-modulus divider to enable fractional-N operation needed for high frequency resolution. The synthesizer includes a programmable on-chip waveform generator logic unit for flexible chirp generation.

The synthesizer is fabricated in 65nm CMOS and occupies an active chip area of 0.53mm^2 (Fig. 21). The chip is packaged in a 4mm $\times$ 4mm 28-pin QFN package. The PLL tuning range extends from 18 to 22GHz and the total power

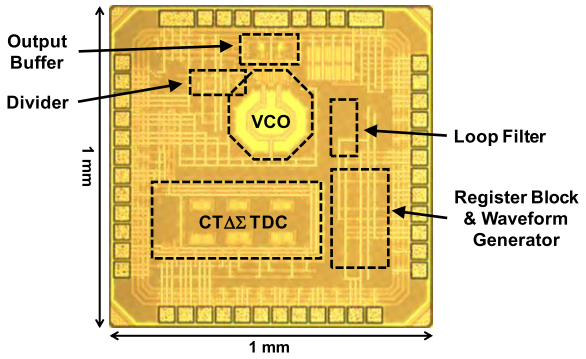


FIGURE 21. Die micrograph.

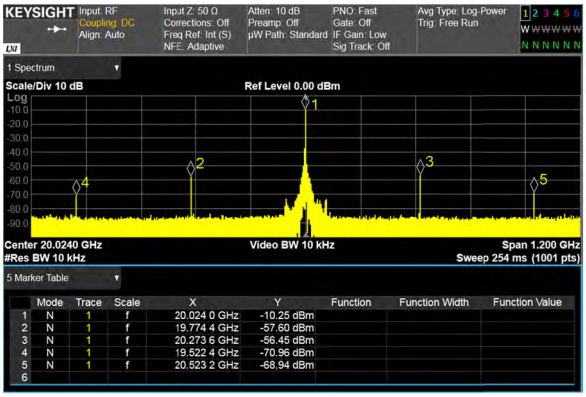


FIGURE 22. Output spectrum at 20GHz.

consumption is 39.6mW. The reference spurs are measured at −45dBc and the fractional spurs are below −60dBc (Fig. 22). The PLL achieves a low close-in phase noise of −88dBc/Hz @ 100kHz with a high loop bandwidth (>1MHz) and fast settling time (<10μs) (Fig. 23). The phase noise peak around 1MHz offset is due peaking in the loop transfer function of the PLL as the loop is configured to have a wide bandwidth with low phase margin for high PLL agility.[3] For a low loop bandwidth, the peaking vanishes and we observe an increased close-in phase noise (−80dBc/Hz @ 100kHz) because more low-frequency VCO noise contributes to the PLL output (Fig. 24).

VI. RADAR TESTBED

We use a complete end-to-end radar testbed combined with discrete components to study and verify the effectiveness of our fully-integrated digital synthesizer design in an FMCW radar system. The testbed generates a 10GHz sawtooth chirp waveform and models a complete radar transceiver including chirp synthesizer, transmitter chain, transmission channel, receiver and digital baseband processing. The 5GHz divided-down output of the synthesizer IC serves as the signal source

[3]Due to the nonlinear VCO gain (Fig. 20(b)), the loop gain and the PLL bandwidth are not constant as the output frequency is modulated. For chirp generation, we choose the accumulator gain of the PLL loop filter such that we have an agile PLL while loop stability is ensured across the entire chirp.

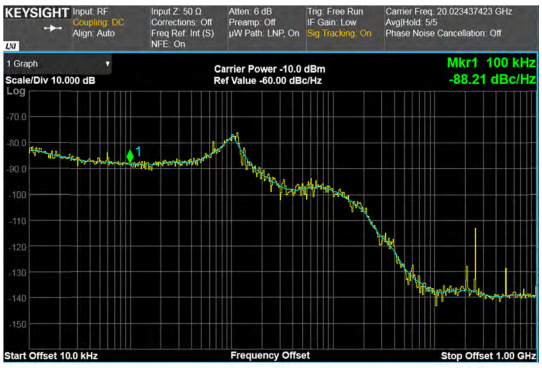


FIGURE 23. Measured phase noise at 20GHz for a wide PLL bandwidth >1MHz.

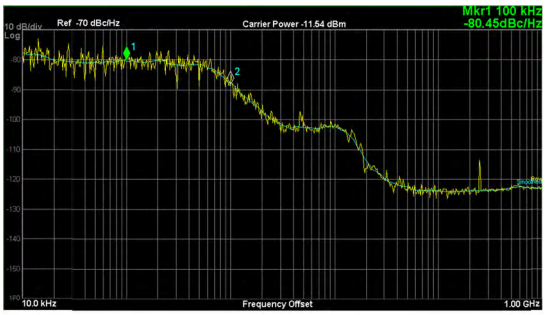
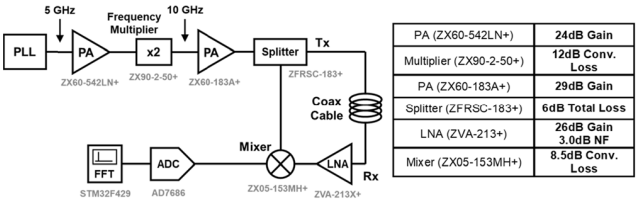


FIGURE 24. Measured phase noise at 20GHz for a low PLL bandwidth.



PA (ZX60-542LN+)	24dB Gain
Multiplier (ZX90-2-50+)	12dB Conv. Loss
PA (ZX60-183A+)	29dB Gain
Splitter (ZFRSC-183+)	6dB Total Loss
LNA (ZVA-213+)	26dB Gain 3.0dB NF
Mixer (ZX05-153MH+)	8.5dB Conv. Loss

FIGURE 25. Block schematic of the radar testbed and component performance data.

of the testbed and commercially available discrete components implement the transmitter and receiver chains as well as the DSP back-end. A block schematic of the testbed is shown in Fig. 25, and pictures of the actual setup are provided in Fig. 26.

The transmitter chain comprises two power amplifiers, a frequency multiplier and a splitter to amplify the synthesizer output signal, double its frequency to 10GHz and provide it to the mixer and the transmission channel. The latter is realized by a long coaxial cable to model the propagation delay of the radar signal on its path to the target and back. MiniCircuits components are used to implement the transmitter chain and receiver front-end. An overview of their performance characteristics at 10GHz is included in Fig. 25. The baseband signal is digitized by an AD7686 from Analog Devices. It features a sample rate of 500kSps and 16-bit nominal resolution. Finally, the testbed uses an STM32F429I Discovery Board

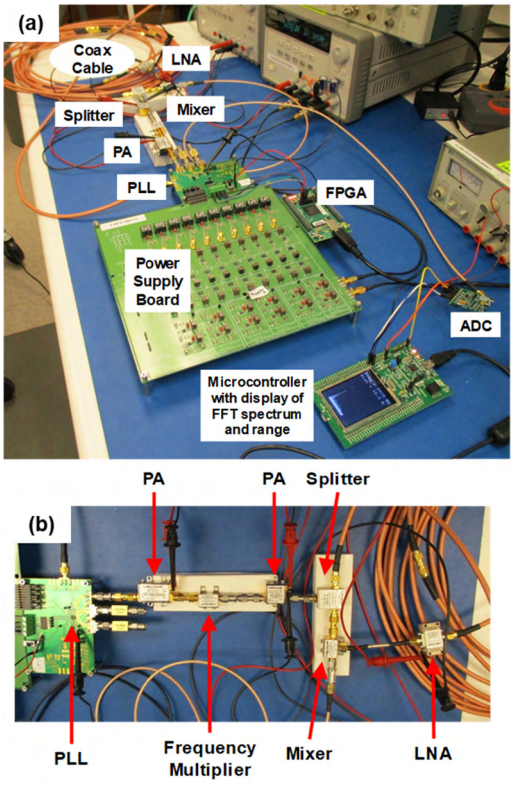


FIGURE 26. Radar testbed: Complete setup (a) and close-up view of the transmit and receive paths (b).

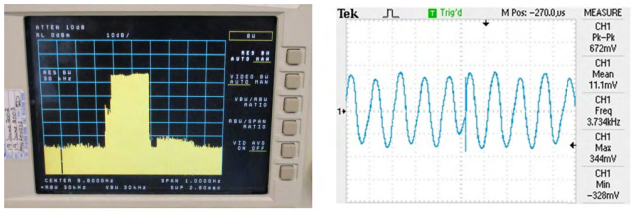


FIGURE 27. FMCW chirp spectrum (a) and IF signal at mixer output (b).

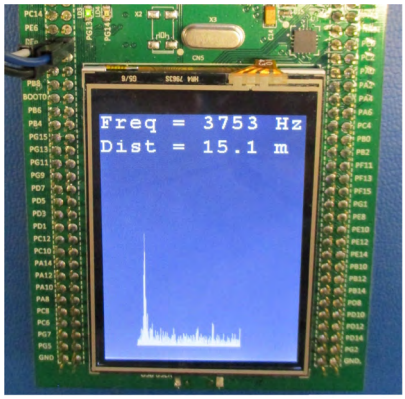


FIGURE 28. Microcontroller display showing beat frequency, range and FFT spectrum.

from STMicroelectronics for FFT processing, range calculation and result display. The STM32F429 microcontroller can provide FFT results in real-time, and the FFT and range results can be readily displayed on the LCD interface of the board.

The synthesizer is configured to generate a sawtooth chirp with a bandwidth of 200MHz and a modulation period of 2.7ms, while the PLL bandwidth is set to 1MHz. These chirp parameters constitute a slow-chirp scenario as studied in our bandwidth and linearity analysis. The PLL output frequency is modulated with 14-bit linearity, resulting in a stepping rate of 6.1MS/s, which exceeds the PLL bandwidth by more than a factor of 6. These settings sufficiently satisfy (10) and we therefore expect reliable range results with no noteworthy spurious peaks in the FFT spectrum. The power spectrum of the chirp is shown in Fig. 27(a). The recorded IF signal at the output of the mixer reveals proper operation of the testbed (Fig. 27(b)).

The microcontroller is programmed to acquire a series of 256 samples from the ADC over 2.7ms, which is the chirp period. It computes the FFT and finds the maximum frequency bin. The FFT spectrum is then fitted to a sinc function around this bin and a more accurate beat frequency is determined through interpolation to improve the range resolution [19]. Based on the given FMCW chirp parameters, the controller calculates the target range that would result in the same signal delay as provided by the coaxial cable in the testbed. FFT spectrum, detected beat frequency and calculated range can be observed on the LCD display of the microcontroller (Fig. 28). After the data sampling period of 2.7ms, the data processing takes about 2.5ms. Therefore, the described algorithm is repeated about every 5ms. During this process, LCD display refresh and data transmission occur in parallel. The implemented algorithm is verified by comparing the beat frequency with the signal frequency at the output of the mixer.

The results obtained from the radar testbed confirm the effectiveness of the implemented radar configuration. In particular, if the length of the coaxial cable between the transmitter and the receiver is changed to model the effect of different propagation delays of the radar signal, the displayed beat frequency and range update as expected and correctly reflect the changes in the propagation delay. As expected, the chosen chirp specifications enable the radar system to reliably resolve the modeled target range with negligible spurious peak levels in the FFT spectrum (Fig. 28), in agreement with the analysis results in Section IV *C*. The chirp synthesizer can successfully drive a radar system to provide reliable results, showing that the described PLL design can effectively be applied in an FMCW radar.

VII. CONCLUSION

Based on the system requirements of an FMCW radar, this paper discusses design considerations for fractional-N chirp synthesizer PLLs. Effective PLLs for chirp synthesis offer low close-in phase noise with high PLL bandwidths and generate highly linear chirps. The presented modeling approach

allows for a straightforward study of the impact of the PLL bandwidth on the accuracy and reliability of target detection. Our analysis for a long-range automotive radar scenario considers both slow and fast chirp modulation. We show that an optimum PLL bandwidth falls below the chirp stepping rate by a factor of at least 3, and it exceeds the modulation frequency by a factor of at least 14. Moreover, a digital chirp synthesizer PLL that uses a noise-shaping TDC and meets the requirements of FMCW radar is presented. Experimental results of a complete end-to-end radar testbed confirm that the synthesizer can effectively drive an FMCW radar system.

REFERENCES

[1] J. Hatch, A. Topak, R. Schnabel, T. Zwick, R. Weigel, and C. Waldschmidt, "Millimeter-wave technology for automotive radar sensors in the 77 GHz frequency band," *IEEE Trans. Microw. Theory Techn.*, vol. 60, no. 3, pp. 845–860, Mar. 2012.

[2] A. G. Stove, "Linear FMCW radar techniques," *IEE Proc. F-Radar Signal Process.*, vol. 139, no. 5, pp. 343–350, Oct. 1992.

[3] D. Cherniak, L. Grimaldi, L. Bertulessi, C. Samori, R. Nonis, and S. Levantino, "A 23-GHz low-phase-noise digital bang–bang PLL for fast triangular and sawtooth chirp modulation," in *IEEE ISSCC Dig. Tech. Papers*, Feb. 2018, pp. 248–250.

[4] J. Vovnoboy, R. Levinger, N. Mazor, and D. Elad, "A fully integrated 75–83 GHz FMCW synthesizer for automotive radar applications with -97 dBc/Hz phase noise at 1 MHz offset and 100 GHz/mSec maximal chirp rate," in *Proc. IEEE Radio Freq. Integr. Circuits Symp. (RFIC)*, Jun. 2017, pp. 96–99.

[5] W. Wu, R. B. Staszewski, and J. R. Long, "A 56.4-to-63.4 GHz multi-rate all-digital fractional-N PLL for FMCW radar applications in 65 nm CMOS," *IEEE J. Solid-State Circuits*, vol. 49, no. 5, pp. 1081–1096, May 2014.

[6] B. P. Ginsburg *et al.*, 'A multimode 76-to-81GHz automotive radar transceiver with autonomous monitoring," in *IEEE ISSCC Dig. Tech. Papers*, Feb. 2018, pp. 158–160.

[7] J. Lee, Y.-A. Li, M.-H. Hung, and S.-J. Huang, "A fully-integrated 77-GHz FMCW radar transceiver in 65-nm CMOS technology," *IEEE J. Solid-State Circuits*, vol. 45, no. 12, pp. 2746–2756, Dec. 2010.

[8] T. Mitomo, N. Ono, H. Hoshino, Y. Yoshihara, O. Watanabe, and I. Seto, "A 77 GHz 90 nm CMOS transceiver for FMCW radar applications," *IEEE J. Solid-State Circuits*, vol. 45, no. 4, pp. 928–937, Apr. 2010.

[9] S. O. Piper, "FMCW linearizer bandwidth requirements," in *Proc. IEEE Nat. Radar Conf.*, Mar. 1991, pp. 142–146.

[10] S. O. Piper, "Homodyne FMCW radar range resolution effects with sinusoidal nonlinearities in the frequency sweep," in *Proc. Int. Radar Conf.*, 1995, pp. 563–567.

[11] M. I. Skolnik, *Introduction to Radar Systems*, 3rd ed. Boston, MA, USA: McGraw-Hill, 2002.

[12] F. M. Gardner, *Phaselock Techniques*. Hoboken, NJ, USA: Wiley, 1966.

[13] T. A. D. Riley, M. A. Copeland, and T. A. Kwasniewski, "Delta-sigma modulation in fractional-*N* frequency synthesis," *IEEE J. Solid-State Circuits*, vol. 28, no. 5, pp. 553–559, May 1993.

[14] E. Laskin *et al.*, "Nanoscale CMOS transceiver design in the 90–170-GHz range," *IEEE Trans. Microw. Theory Techn.*, vol. 57, no. 12, pp. 3477–3490, Dec. 2009.

[15] M. C. Budge and M. P. Burt, "Range correlation effects in radars," in *Proc. Rec. IEEE Nat. Radar Conf.*, Apr. 1993, pp. 212–216.

[16] K. Thurn, R. Ebelt, and M. Vossiek, "Noise in homodyne FMCW radar systems and its effects on ranging precision," in *IEEE MTT-S Int. Microw. Symp. Dig.*, Jun. 2013, pp. 1–3.

[17] A. Ergintav, F. Herzel, D. Kissinger, and H. J. Ng, "An investigation of phase noise of a fractional-N PLL in the course of FMCW chirp generation," in *Proc. IEEE Int. Symp. Circuits Syst. (ISCAS)*, May 2018, pp. 1–4.

[18] M. Gerstmair, A. Melzer, A. Onic, R. Stuhlberger, and M. Huemer, "Highly efficient environment for FMCW radar phase noise simulations in IF domain," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 65, no. 5, pp. 582–586, May 2018.

[19] H.-H. Ko, K.-W. Cheng, and H.-J. Su, "Range resolution improvement for FMCW radars," in *Proc. Eur. Radar Conf.*, 2008, pp. 352–355.

[20] M. B. Dayanik, N. Collins, and M. P. Flynn, "A 28.5–33.5GHz fractional-N PLL using a 3^{rd} order noise shaping time-to-digital converter with 176fs resolution," in *Proc. Conf. 41st Eur. Solid-State Circuits Conf. (ESSCIRC)*, Sep. 2015, pp. 376–379.

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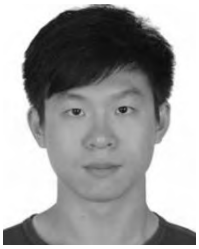

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