A Battery-Powered Opto-Electrophysiology Neural Interface with Artifact-Preventing Optical Pulse Shaping

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Abstract

We present a neural interface IC for high-precision optical stimulation and electrical recording from implanted optoelectrodes with the highest system integration to date. The system combines 12 high-resolution constant-current LED driver channels, 32 recording channels, and an efficient PMU for operation from a low voltage Li battery on a wireless platform. A novel LED driver architecture features a high-efficiency wide-current-range fully-integrated voltage regulator and a high-resolution pulse shaper to minimize recording artifacts from sharp current pulse edges. A prototype, fabricated in 0.18µm CMOS, occupies 7.35mm^2. The LED driver has a peak efficiency of 50% and consumes 31µW quiescent power. We demonstrate *in-vivo* that the pulse-shaping scheme prevents stimulation artifacts. **Key Words:** neural interface, LED driver, optogenetics.

Introduction

Optogenetics offers a precision neuroscientific tool for mapping brain circuits and studying neurological disorders through selectively exciting or inhibiting target neurons with cellular resolution [1]. Micromachined optoelectrodes, which integrate on-shank µLEDs with electrical recording sites [2], provide a bidirectional multi-channel neural interface and single-neuron stimulation precision in a compact form factor. Recently, optogenetics systems have shown progress towards enabling wireless freely-moving animal behavior experiments, but still suffer from large mass, low channel count, and high power consumption [3-6]. Additionally, optical pulse stimulation artifacts due to inter-channel capacitive coupling and photoelectric effects, corrupt signals and hamper closed-loop operation and off-line signal analysis. In this work, we introduce an opto-electrophysiology interface IC to address these challenges by (1) combining the recording and LED driver channels on the same chip along with power management unit (PMU), (2) providing an efficient wide-current-range LED drivability from a low-voltage battery supply by integrating inductor-less step-up voltage regulators, and (3) incorporating an arbitrary waveform generation circuit which suppresses artifacts by current pulse shaping.

System Architecture

Our interface IC prototype provides a mixed-signal optoelectrode interface for a proposed wireless platform powered by an ultra-lightweight Li-ion battery (Fig. 1). As shown in Fig. 2, it includes 32 recording channels, 12 LED drivers with integrated switched-capacitor (SC) regulators, and low-dropout (LDO) linear regulators for remaining modules.

The recording circuit provides wideband (1Hz-15kHz) recording from 2 groups of 16 channels. Each group shares a reference electrode which is buffered through an amplifier and subtracted from signals before they are time-multiplexed to share a common PGA and a 10-bit SAR ADC. The digital outputs are serialized through an SPI slave controller.

The 12 LED drivers address the unique challenges of µLED optogenetics stimulation. The drivers provide constant-current pulses, ranging from 0-1mA at 10-bit resolution (LSB = 1µA) and with a rise-time of <50µs necessary to observe quick

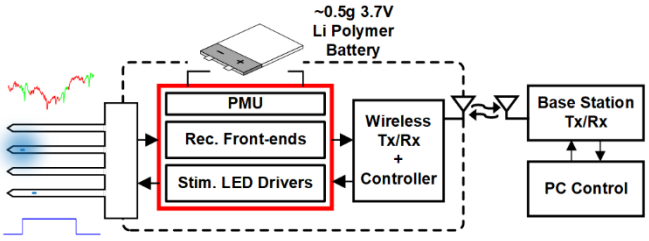

Fig. 1. Proposed interface IC (red) as part of a wireless opto-electrophysiology system.

neuronal reactions. The architecture is subdivided into a high-precision current-pulse-shaping circuit and a step-up voltage regulator providing the high supply voltage and current necessary to drive µLEDs. VDAC and V-I converter generate a current pulse which is multiplied and upconverted to high voltage. The split between low-voltage pulse generation circuitry and high output voltage regulator and current-mirror allows integration on a low-voltage 0.18µm CMOS process.

The integrated LDOs provide 3 voltage-domain power supplies to the recording and LED-driving control circuitry. They share a common bandgap-reference circuit and require off-chip output capacitors.

LED Driver Circuit Design

A. High-resolution DAC for Optical Pulse Modulation

While PWM current pulse modulation is typically used in optical stimulation, we introduce a novel high-resolution pulse shaping circuit (Fig. 3) for artifact reduction in recording. In the regular *PWM mode*, a 10-bit resistor divider DAC and an amplifier set a constant current through R_c. A fast pulse is generated by switching this current between the mirror and the low supply voltage. In *pulse shaping mode*, a smooth arbitrary waveform is generated by dithering the 2.5b thermally-coded sub-mux of the resistive ladder with an oversampling 1st-order digital ΣΔ modulator. A 2-pole RC low-pass module filters the noise-shaped DAC output. The V-I converter translates the filtered voltage into current. Since *pulse shaping mode* is enabled only between pulse transitions, it consumes negligible additional power. Due to an inherent amplifier offset, the V-I converter may generate a static current at 0V input. This is calibrated in our design by introducing an intentional negative offset and adjusting the DAC input appropriately. Digital-control of R_c calibrates gain variation due to resistor mismatch.

B. Integrated Voltage Regulator

The proposed channel-specific step-up voltage regulator (Fig. 4) is highly efficient over a large range of driving currents and does not need off-chip inductors and capacitors. The regulator consists of two 2-phase SC voltage doublers regulated by an externally-clocked dynamic comparator. Due to the high above-supply voltage (VREG) needed for the level-shifting current mirror, a set of level shifters and inverters drive the thick-oxide transistor switches. The output voltage (VREG) is fed through a resistive divider into a zero-on-reset comparator to provide pulse-frequency (PFM) control. As opposed to [7], a dynamic comparator is used to further reduce quiescent current The external 200MHz clock is shared

between all channel regulators and voltage DACs.

Measurements

The prototype is fabricated in 0.18µm CMOS and occupies 7.35mm^2 (Fig. 5). The recording circuit occupies 0.012mm^2/ch. and consumes 23.6 µW/ch. Fig 6(a) shows its measured frequency response and noise spectrum. The LED driver occupies 0.089mm^2. In *PWM mode* the measured 10bit DNL/INL are less than 0.403/1.37. In *pulse-shaping mode* the measured DAC output SNDR is 43dB SNDR (Fig. 6(b)). It consumes overall quiescent power of 31µW at 3.7V supply, maintains full current drivability over 3.6-3.8V voltage variation, and achieves 50% peak efficiency. Fig. 6(c) shows the power consumption distribution. Fig. 7 shows the LED current driven in PWM mode with under 30µs rise-time square pulses and in pulse-shaping-mode with generated Gaussian-like pulse. *In-vivo* recordings from anesthetized mouse hippocampus showed the increased neural activity in response to optical stimulation and an eliminated artifact when Gaussian-like pulses are used (Fig. 8). Finally, the summary and comparison table (Fig. 9) outlines the state-of-the-art specifications and system-level integration.

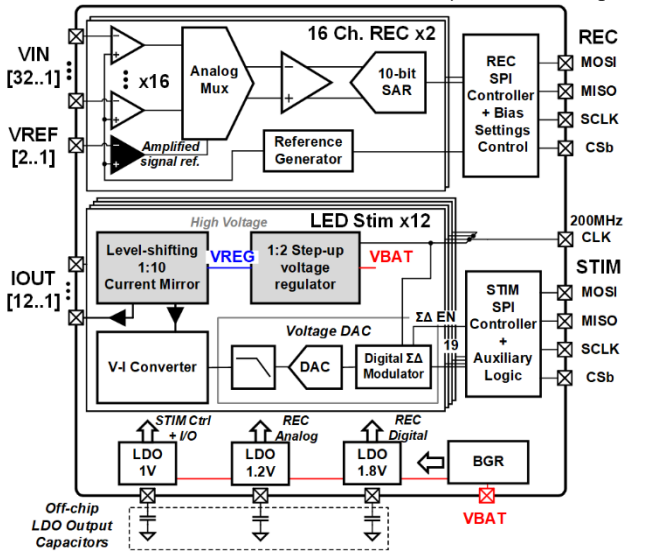

Fig. 2. Proposed chip architecture block diagram. Blocks in grey utilize thick-oxide transistors for high voltage operation.

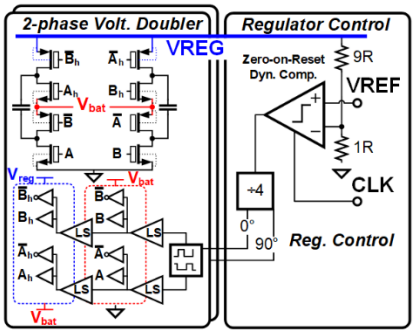

Fig. 4. Integrated SC voltage regulator circuit diagram.

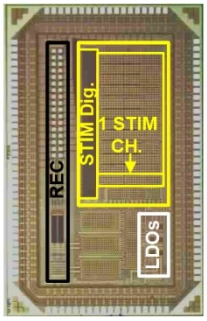

Fig. 5. Die photo.

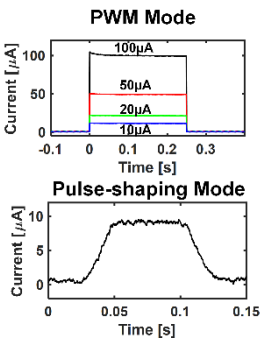

Fig. 7. LED current driven by a sharp square pulse (*PWM mode*) and Gaussian-shaped pulse (*pulse shaping mode*).

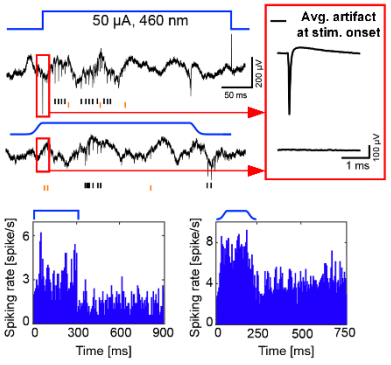

Fig. 8. *In-vivo* recordings show same neural response for both PWM and Gaussian pulse shapes while the artifacts are absent.

References

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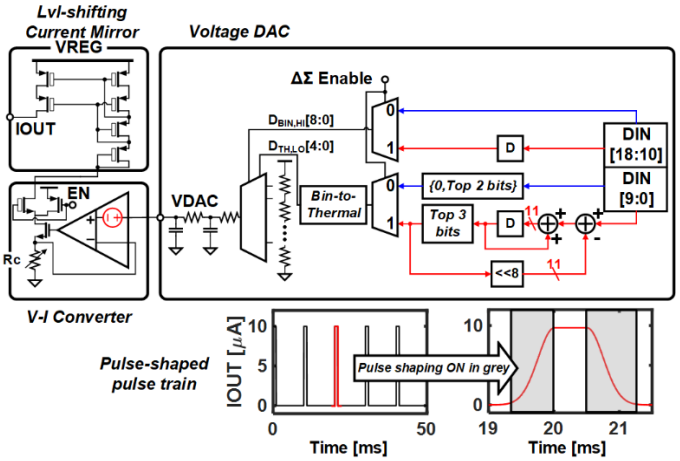

Fig. 3. Circuit schematics of voltage DAC, V-I converter, and the level-shifting current mirror. Shown below is a simulated Gaussian-like pulse generated by high-resolution DAC in pulse-shaping mode.

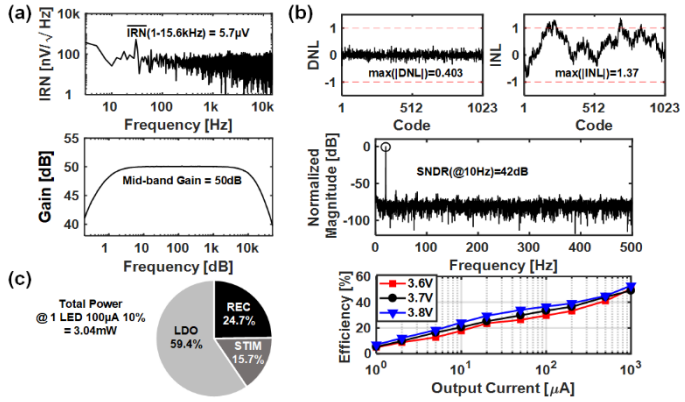

Fig. 6. Measured (a) recording circuit gain and input-referred noise, (b) LED driver *PWM mode* DNL/INL, sine output spectrum in *pulse-shaping mode*, and power efficiency, and (c) total power consumption.

		[3]	[4]	[5]	[6]	**This Work**
Tech.	Rec.	N/A	0.35µm	COTS	0.18µm	**0.18µm**
	Stim.	0.8µm		COTS	COTS	
	PMU	0.8µm	N/A	COTS	COTS	
# rec/stim ch.		-/2	4/6	32/32	32/48	**32/12**
Power source		RF/ 3.8V bat.	N/A	3.7V bat.	9V bat.	**3.7V bat**
Stim. Range/Res.		0-51mA 10-bit	0-1mA 8-bit	HW Preset	0-1mA 10-bit	**0-1mA 10bit**
Stim. Modulation		PWM, amplt.	PWM, amplt.	PWM	PWM, amplt	**Arb. wave**
Rec. BW/Res		N/A	500 Hz (1kS/s)	20kHz (30kS/s)	20kHz (30kS/s)	**15kHz (32kS/s)**
Rec. Res.		N/A	10-bit	16-bit	16-bit	**10-bit**

Fig. 9. Summary and comparison table.