A 0.19mm² 128mW 0.8-1.2GHz 2-Beam 8-Element Digital Direct to RF Beamforming Transmitter in 40nm CMOS

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***Abstract*— An order of magnitude improvement in area and power consumption per element is achieved by digital phase shifting combined with bandpass ΔΣ modulation and N-path filtering. The 8-element beamforming transmitter allows accurate steering of multiple independent beams. Key to the efficiency are the pairing of area-efficient bandpass ΔΣ modulation with N-path filtering to suppress quantization noise and careful frequency management to allow efficient digital phase shifting and up-conversion. The 40nm CMOS prototype generates two independent 1.2GHz beams, it consumes 128mW and occupies an active area of only 0.19mm², consuming only 16mW and 0.02mm² per element.**

***Index Terms*— Beamforming, RF-DAC, Delta Sigma Modulation, N-path filter**

I. Introduction

Transmit beamforming with accurate, multiple, independent beams is essential for high-speed wireless communication, especially for MIMO and 5G. Large transmit arrays are attractive because the per-element transmit power reduces with N^2, however this improvement requires a very low per-element power/area overhead. The requirements for beam accuracy and multiple beams are best met by digital beamforming. However, conventional digital transmit beamforming requires extensive DSP, large DACs as well as up-converters and filters and so tends to be large and power hungry.

This work combines digital phase shifting with digital bandpass ΔΣ modulation and N-path filtering to enable an 8-element 2-beam mostly-digital beamforming transmitter with record power and area efficiency and accurate beamforming. The 40nm CMOS prototype generates two independent 800MHz-1.2GHz beams, consumes 128mW and occupies an active area of $0.19\mathrm{mm}^2$. The 16mW and $0.02\mathrm{mm}^2$ consumed per element represent an order of magnitude improvement.

Fig. 1 shows the system architecture. The transmitter is made of 8 identical stripes (one per antenna element); each stripe phase-shifts, up-samples, up-converts, converts to analog and finally filters each transmit signal. We combine digital phase shifting, digital bandpass ΔΣ modulation, 1.5b DACs and N-path filters to enable precise beam patterns, with low die area and low power consumption. Moreover, this approach supports multiple independent beams, each potentially with its own unique transmit data.

While impressive progress has been made on Direct Digital to RF (DDRF) transmitters [1-4], existing approaches require too much area and consume too much power for transmit beamforming. [1] addresses DAC up-mixing artifacts, but uses a large DAC and occupies $0.93\mathrm{mm}^2$. [2] uses a smaller 10bit DAC and programmable ΔΣ modulator with out-of-band notch filtering for an $0.82\mathrm{mm}^2$ area. [3] delivers charge through a 12b resistive DAC and occupies $0.22\mathrm{mm}^2$, but requires off-chip DSP for charge calculation. [4] uses bandpass digital ΔΣ modulation but requires off-chip analog filtering to suppress the substantial shaped quantization noise. All these approaches are restricted to single element use and none support transmit beamforming.

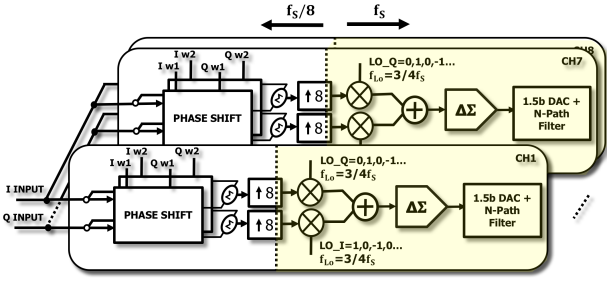

Fig. 1. Transmit beamformer system architecture.

II. Implementation

Our new approach combines digital bandpass ΔΣ modulation with digital phase shifting and up-conversion for power and area efficient direct digital to RF beamforming. Careful frequency planning greatly reduces the power and area of the digital processing. We use a 1.5b DAC, driven by a digital bandpass modulator for its very small area and immunity to mismatch. We counteract the shaped quantization noise of the 1.5b DACs with an array on-chip bandpass N-path filters. We solve the problem of spurs in the 1.5b modulator by efficiently introducing Gaussian dither.

A. System Architecture

In each stripe, I/Q baseband data is phase shifted by multiplication with two sets of weight coefficients to form two independent beams. After digital summing, the phase modulated I/Q streams are up-sampled by 8 using linear interpolation. These streams are up-mixed to RF by multiplication with digital I/Q LO sequences. Careful choice of the sampling rate and RF frequency allows the LO signals to be represented by -1,0,1,0..., greatly simplifying multiplication and summing. The sum of the up-converted I and Q streams is noise-shaped by a digital bandpass $\Delta\Sigma$ modulator to drive a 1.5 bit DAC which directly generates the analog RF signal. Mixing with I and Q LOs eliminates the high frequency image. Finally, the out-of-band quantization noise of the bandpass $\Delta\Sigma$ is suppressed by an N-path filter.

B. Digital Phase Shifting and Up-mixing

We take advantage of simple processing and optimal frequency planning for compact, low power beamforming DSP. Digital circuitry feeding each modulator applies phase shift, combines data for multiple beams, and up-samples and up-converts, as illustrated in Fig. 2. Digital phase shifting and processing has the advantages of accuracy and flexibility, however fast digital processing takes a lot of energy. We choose sampling rates as well as the relationship between sampling rate and RF frequency to simplify processing and reduce both phase shifting and modulator power consumption.

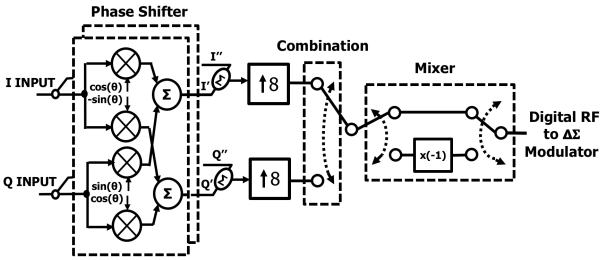

Fig. 2. Digital phase shifting, up-sampling and up-conversion.

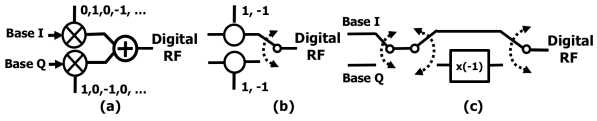

Fig. 3. (a) Digital up-conversion and summing, (b) simplified with MUXing and (c) final implementation.

Phase shifting is at the reduced rate of $f_S/8$ (200MHz) to reduce power consumption. Multiplication with programmable 5b I and Q weights phase-shifts the baseband I/Q transmit data. The weight coefficients are calculated from the desired angle for the main transmit lobe(s) and quantized into 5b. Two simultaneous beams are realized by multiplying with two sets of weights. After multiplication, the I/Q data from the different beams is summed to form single I and Q streams. Applying linear interpolation, these streams are up-sampled by 8x to the 1.6GHz (f_S) sampling rate of the digital bandpass $\Delta\Sigma$ modulator.

We choose the combination of a 1.6GHz sample rate and a 1.2GHz RF frequency to enable simple and low power and low area up-mixing to RF. As in Fig. 1, we digitally up-mix the phase-shifted baseband signals to the RF frequency of 1.2GHz. This is done by multiplying the up-sampled I and Q signals with digital I and Q LO sequences.We take advantage of the relationship between the sampling frequency f_S and the RF carrier frequency f_C to simplify this processing. In Fig. 4 we see that an $f_S/4$ sine wave sampled at f_S is represented by the sequence -1,0,1,0... We also see that a sampled $3/4f_S$ sine wave is represented by this sequence. Thus, we use apply orthogonal (i.e. 1,0,-1,0 etc.) I and Q sequences to mix up the baseband signals to $3/4f_S$ (1.2GHz). This allows the beamform processing and modulator to run at 1.6GHz instead of 4.8GHz.

We sum the mixed-up I and Q sequences to form the digital RF output (Fig. 1). However, we note because the I and Q sequences are orthogonal and only one is non-zero at any time to simplify implementation. Ignoring the 0 values, the digital RF sequence formed by MUXing between and I and Q streaming and alternately multiplying by 1 and -1. (Fig. 2 and Fig. 3)

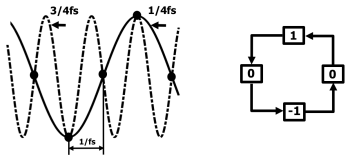

Fig. 4. Illustration of subsampling of the $3/4f_S$ LO and the resulting state transition sequence of the digital LO.

C. Bandpass $\Delta\Sigma$ Modulator

Our approach uses bandpass digital $\Delta\Sigma$ modulation to drive a compact 1.5b DAC and suppresses the quantization noise with N-path filtering. The digital bandpass modulator provides the noise-shaped 3-level digital input to drive the DAC. The modulator provides 3-level noise-shaped copies of the input signal at 1/4 and 3/4 of the sampling rate, f_S. As discussed, these sample to signal ratios greatly simplify the up-conversion mixer.

The bandpass $\Delta\Sigma$ modulator is formed as a single loop, with a single feedback path around a 4^{th} order Chebyshev NTF bandpass filter, as shown in Fig. 5. Since the stability of the modulator is sensitive to the peak out-of-band gain,

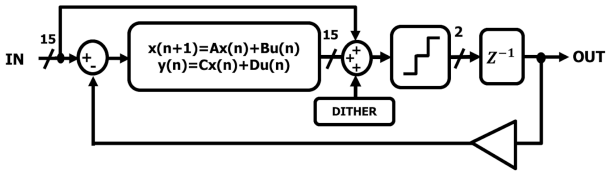

Fig. 5. Block diagram of 4^{th} order digital bandpass $\Delta\Sigma$ modulator.

choosing a filter that is maximally flat out of band will allow the most in-band noise reduction before instability. This, combined with an even distribution of in-band noise, makes the Inverse Chebyshev (aka Chebyshev Type II) the most spectrally efficient choice. The digital 4^{th} order Chebyshev NTF is designed with a rejection of 47dB and bandwidth of 38MHz. The center frequency (f_C) and the sampling frequency are scalable with $f_C/f_S = 3/4$. The discrete State Space (DSS) model of the modulator is directly implemented in Verilog.

Although a 1.5b DAC has the advantage of resilience to mismatch, such a low quantizer resolution in a $\Delta\Sigma$ modulator leads to spurs. Generally, in the design of a $\Delta\Sigma$ modulator, we assume that the quantizer introduces white Gaussian noise. However, this assumption is only valid if the quantizer resolution is large. A low-resolution quantizer causes spurious tones as illustrated in Fig. 6 for a 1.5b quantizer. We eliminate the spurs, by adding one LSB wide Gaussian dither to the input of the quantizer. We efficiently generate this Gaussian random dither on-chip by summing the uniform random noise outputs of four 20b-23b Linear Feedback Shift Registers (LFSRs) as shown in Fig. 6.

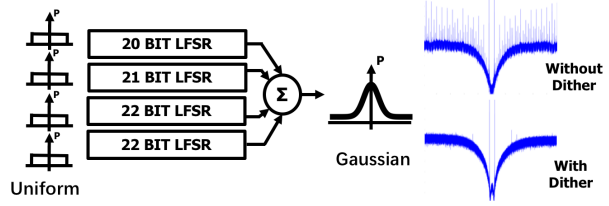

Fig. 6. Generation of Gaussian dither and the improvement in the bandpass modulator spectrum thanks to the introduction of dither.

D. DAC and N-path Filter

The combination of a 1.5b $\Delta\Sigma$ DAC and N-path filtering leads to small and efficient DACs. Unique in our approach, we combine a digital bandpass $\Delta\Sigma$ modulator, a 1.5bit DAC and an N-path filter in each transmit stripe for small area, high accuracy and low out-of-band noise. The 1.6GHz digital bandpass modulator directly drives the 1.5b DAC to form the 1.2GHz digital RF output. Compared to a

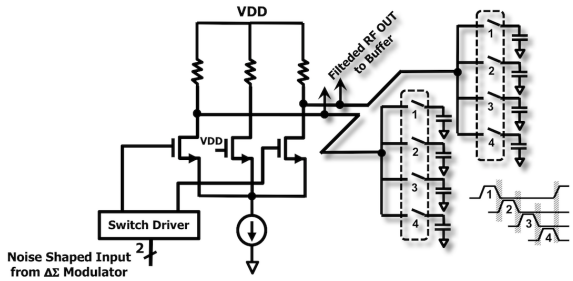

Fig. 7. Circuit implementation of 1.5bit DAC and N-path filter.

single-bit DAC, a 3-level DAC generates less quantization noise and thanks to its single current source still avoids the problem of unit mismatch seen in higher resolution DACs. The digital bandpass modulator and 1.5b DAC have several advantages: (i) no mismatch error (ii) direct modulation to RF without need for analog up-conversion and (iii) flexible center frequency. However, a challenge is that bandpass modulators generate significant out of band quantization noise. We solve this problem by elegantly combining the DAC with an N-path filter. The N-path filter is a compact, high-Q bandpass filter and inherently tracks the center frequency of the modulator, effectively the suppressing the shaped quantization noise.

The N-path filter and DAC are shown in more detail in Fig. 7. The DAC is directly driven by the three-level 1.6GHz digital signal from the bandpass $\Delta\Sigma$ modulator. The three-level DAC has a single current source and three switches connect to the two differential load resistors and the dummy load. A differential four-capacitor N-path filter sequentially connects filter capacitors to the load resistors to provide a filter passband centered on the RF carrier. The four 1.2GHz non-overlapping clocks for the N-path filter are derived from a 4.8GHz clock which in turn is 3x the modulator sampling clock. The DAC load resistance of 1kΩ and the 2pF filter capacitors set 3dB passband to be 38 MHz. Clocking is shared across the transmit array to improve beam accuracy.

III. Measurement Results

This prototype implemented in 40nm CMOS (Fig. 10) occupies 0.19mm^2, and the digital core size is 0.12mm^2. Except for the 1.5b DAC and N-path filter, the design is synthesized from Verilog code and laid out with automated place-and-route tools. The overall power consumption is 128mW for a 1.2GHz output. Fig. 9 shows the measured constellation when a 64 QAM modulated digital baseband signal is applied to the chip. The digital transmit data is filtered with a Gaussian filter with a rolloff factor of 0.22. With a 64-QAM signal at 1.205GHz, an EVM of -23.6dB is measured for a symbol-rate of 320k/s. For the same

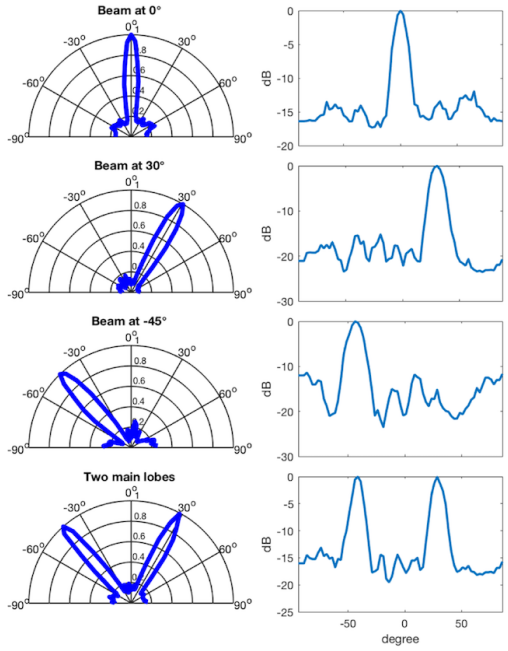

Fig. 8. Measured transmit beam patterns at 0 degrees, 30 degrees, -45 degrees and with two simultaneous main lobes.

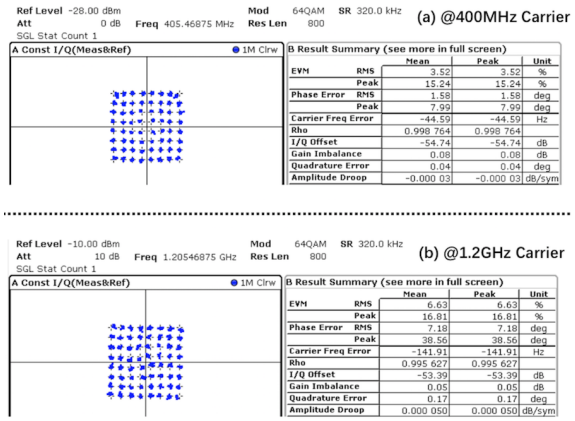

Fig. 9. 64 QAM constellation plot with 320k symbol rate, EVM=3.52% @400MHz carrier (top) and EVM=6.63% @1.2GHz carrier (bottom).

conditions, the measured EVM is -29.0dB for a 405MHz carrier. The measured beam patterns for 0, 30 and 45 degrees and for two separate beams are shown in Fig. 8. These measurements assume eight in-line dipolar antennas, spaced at half wavelengths. The measurement step size is 2.5 degrees. These measurements show great consistency with near-ideal beam patterns.

IV. Conclusion

Table I summarizes the measured performance. Die area per antenna is an order of magnitude smaller than the state-of-the-art. Apart from the DAC and the N-path filter the design is generated with digital synthesis and place and route tools. This work demonstrates the promise of digital techniques for highly compact, flexible and efficient direct-to-RF digital beamforming.

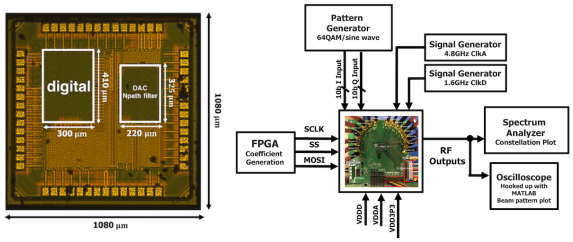

Fig. 10. Die micrograph and measurement setup.

TABLE I
Measured Performance Summary

Architecture	Digital transmit beam forming			
Technology	40nm CMOS			
RF Bandwidth [MHz]	40			
Carrier frequency [GHz]	0.8-1.2			
Input data	200MS/s 10bit I/Q baseband			
Beamforming	8 channels			
Coefficient resolution[bits]	10 bit, 5 bit I and Q			
# of simultaneous beams	2			
EVM (dB, 64 QAM)	-29			
CIM3[dBc]	< -32			
Supply[V]	1			
Power consumption (mW)			0.8GHz	1.2GHz
	Digital	All	63	107
		Channel	8	13
	Analog	All	20	21
		Channel	2.5	2.6

Acknowledgment

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