15.3 A 36.3-to-38.2GHz -216dBc/Hz² 40nm CMOS Fractional-N FMCW Chirp Synthesizer PLL with a Continuous-Time Bandpass Delta-Sigma Time-to-Digital Converter

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Automotive radar and other mm-wave applications require high-quality frequency synthesizers that offer fast settling and low phase noise. Analog PLLs still dominate in the mm-wave range, but all-digital PLLs (ADPLLs) promise greater flexibility and area efficiency. However, existing mm-wave ADPLLs are large, fail to offer low in-band phase noise [1] or must rely on extensive calibration [2]. Performance limitations of conventional TDCs still remain a major roadblock for the adoption of high-frequency ADPLLs. To address this problem, this work introduces a noise-shaping TDC based on a 4th-order bandpass ΔΣ modulator (BPDSM) to achieve low integrated noise (183fs$_{rms}$) and high linearity. Our approach enables low in-band phase noise (-85dBc/Hz @ 100kHz) for wide loop bandwidths (>1MHz) in a calibration-free single-loop digital 36.3-to-38.2GHz PLL. The prototype PLL effectively generates fast (500MHz/55µs) and precise (824kHz$_{rms}$ frequency error) triangular chirps for FMCW radar applications.

We sample the reference clock with a continuous-time bandpass ΔΣ modulator to measure phase giving the following advantages: 1) The proposed bandpass ΔΣ TDC (BPDSTDC) avoids low-frequency TDC noise contamination by treating the reference as an analog signal and sampling it at 4 times the reference frequency before down-converting it in the digital domain. Phase detection in conventional analog and digital PLLs is contaminated by low-frequency noise because the reference clock samples the feedback signal at the same frequency. Analog down-conversion to DC is implicit in conventional PLLs, causing noise sources close to DC, primarily flicker noise, to interfere with the phase-difference measurement. 2) It solves the bandwidth-related challenges of conventional reference-sampling ADCs. Such Nyquist-type ADCs require a large bandwidth to track the input edges (Fig. 15.3.1) or, like [3], resort to a preceding phase-frequency detector (PFD) with a charge pump (CP). This is possible because the BPDSM oversamples a narrow bandwidth around a center frequency with a large oversampling ratio and shapes the quantization noise out of band, achieving high resolution in the center bandwidth. 3) In contrast to delay-line-based TDCs, there is no requirement for calibration. 4) It offers an extended phase detection range of ±2π compared to ±π/2 with conventional reference-sampling ADCs, resulting in robust PLL locking behavior without the need for an additional loop for frequency acquisition.

The BPDSTDC consists of a BPDSM followed by digital down-conversion (DCC) (Fig. 15.3.1). In our PLL, the feedback signal serves as the TDC clock, and the BPDSM outputs a digitized version of a sinusoidal reference, sampled at 4 times the reference frequency F_{REF}. The output is a measure of the phase alignment between the feedback and the reference and is then digitally down-converted by multiplying by a (+1,0,-1,0) digital sequence, which provides a DC value proportional to the captured phase information. The low-pass characteristic of the PLL filters out the shaped TDC noise. The BPDSM provides a 5MHz bandwidth around the reference frequency of 120MHz. This translates to a 2.5MHz TDC bandwidth, offering sufficient margin for PLL bandwidths >1MHz. Since the loop locks with $F_{FB} = 4\times F_{REF}$, the BPDSTDC shows an extended phase detection range of ±2π of the feedback phase (Fig. 15.3.1), resulting in a wider PLL locking range.

The prototype IC is implemented as a single-loop type-II fractional-N PLL (Fig. 15.3.2). Since the feedback signal serves as the BPDSM clock, shaped noise from the ΔΣ fractional-N divider might increase the in-band phase noise of the PLL. We reduce the fractional-N quantization noise with a divider chain that uses a phase interpolator to implement divider ratios with small incremental steps of 1/4. Hardware measurements show that this improves in-band phase noise by 18dB in comparison to a divider-ratio step size of 4, and that there is no difference in the measured in-band phase noise for integer-N and fractional-N modes. We generate 8 phases as the VCO output is divided by 8, and use a pipelined phase interpolator [4] with two phase-interpolator (PI) units to quadruple the number of selectable phases to 32 (Fig. 15.3.2). With the preceding division by 8, phase rotation allows us to emulate the divider-ratio step size of 8/32 = 1/4. Since the phase rotation occurs ahead of the final divider stage, we perform only one phase shift per divider output cycle to retain the step size of 1/4 for the entire divider chain. A 2nd-order ΔΣ modulator controls the phase rotation for fractional-N division. Finally, on-chip chirp control logic modulates the PLL division ratio to generate the desired FMCW waveform profile.

The BPDSM is implemented as a 4th-order continuous-time modulator (Fig. 15.3.3) to obtain 2nd-order noise-shaping in the BPDSTDC. The inherent anti-aliasing of the continuous-time BPDSM suppresses reference distortion. The modulator employs single-opamp resonators [5] to reduce power and area. A feedforward path around the second resonator allows the omission of the return-to-zero (RZ) DAC at the modulator input for the benefit of reduced input-referred noise. A transconductance amplifier sums the output currents of the resonators, and its output voltage is digitized by a 5-level flash quantizer. As also shown in Fig. 15.3.3, the PI units forward both input phases and generate an intermediate phase [4]. Each PI unit consists of three PI core circuits, two of which operate in phase-forwarding mode, while the third interpolates the two input phases. The logic gates at the PI core inputs avoid short-circuit currents to improve the linearity of the phase interpolation [4].

The prototype IC is fabricated in 40nm CMOS (Fig. 15.3.7). The BPDSM occupies 0.02mm² and consumes 7.6mW from a 1.1V supply. Stand-alone measurements of the BPDSM with a 120MHz input and an external 480MHz clock show 63dB SNDR (10.2b ENOB) for a 5MHz bandwidth (Fig. 15.3.4). The output power spectrum of the BPDSTDC is obtained by applying a phase-modulated clock around a 480MHz carrier, revealing ideal 2nd-order noise-shaping (Fig. 15.3.4). The BPDSTDC achieves a low measured integrated rms noise of 183fs in a 1MHz signal bandwidth, positioning our TDC among the best of noise-shaping TDCs in Fig. 15.3.4. Thanks to the low TDC noise, the PLL achieves a low measured in-band phase noise of -85dBc/Hz at 100kHz offset for a 38.1GHz output and a loop bandwidth >1MHz (Fig. 15.3.5), corresponding to a normalized phase noise of only -216dBc/Hz². Phase noise peaking around 1MHz offset derives from peaking in the loop transfer function as the loop dynamics are chosen to obtain an agile PLL having a wide bandwidth with low phase margin. A comparison with prior art in Fig. 15.3.6 ranks these phase noise results among the best achieved in a mm-wave CMOS fractional-N PLL. The prototype PLL consumes a total power of 68mW and occupies 0.18mm².

To verify the quality of the chirp synthesis, our PLL generates a triangular FMCW chirp profile with a 500MHz bandwidth from 37.65 to 38.15GHz and chirp slopes up to 10MHz/µs (Fig. 15.3.5). Chirp measurements reveal the chirp precision with a frequency error of only 824kHz$_{rms}$ for a 9.1MHz/µs slope, showing the effectiveness of the PLL for fast and precise chirp generation. Our BPDSTDC successfully leverages the high resolution of a BPDSM gained from oversampling and noise-shaping to demonstrate low-phase-noise performance in a wide-bandwidth digital PLL, without need for extensive calibration. The prototype PLL achieves an excellent combination of normalized phase noise and area for a >10GHz digital PLL when compared to prior art in Fig. 15.3.6. The normalized phase noise at 100kHz reaches that of the analog fractional-N PLL, and of the digital PLLs only the 9GHz digital PLL achieves similar normalized phase noise.

Acknowledgements:
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References:
[1] W. Wu, et al., "A 56.4-to-63.4 GHz Multi-Rate All-Digital Fractional-N PLL for FMCW Radar Applications in 65 nm CMOS," *IEEE JSSC*, vol. 49, no. 5, pp. 1081-1096, May 2014.
[2] A. Hussein, et al., "A 50-to-66GHz 65nm CMOS All-Digital Fractional-N PLL with 220fs$_{rms}$ Jitter," *ISSCC*, pp. 326-327, Feb. 2017.
[3] Z. Xu, et al., "A 3.6 GHz Low-Noise Fractional-N Digital PLL Using SAR-ADC-Based TDC," *IEEE JSSC*, vol. 51, no. 10, pp. 2345-2356, Oct. 2016.
[4] A. Narayanan, et al., "A Fractional-N Sub-Sampling PLL using a Pipelined Phase-Interpolator With an FoM of -250 dB," *IEEE JSSC*, vol. 51, no. 7, pp. 1630-1640, July 2016.
[5] H. Chae, et al., "A 12 mW Low Power Continuous-Time Bandpass ΔΣ Modulator With 58 dB SNDR and 24 MHz Bandwidth at 200 MHz IF," *IEEE JSSC*, vol. 49, no. 2, pp. 405-415, Feb. 2014.

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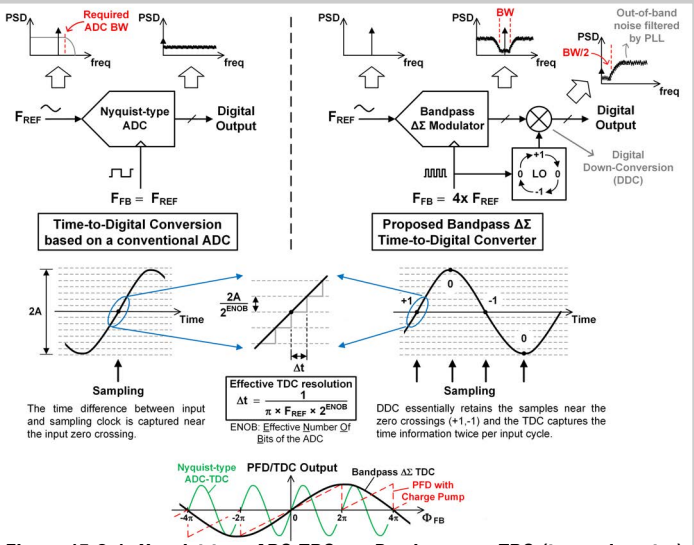


Figure 15.3.1: Nyquist-type ADC-TDC vs. Bandpass ΔΣ TDC (top and center) and phase transfer curves (bottom).

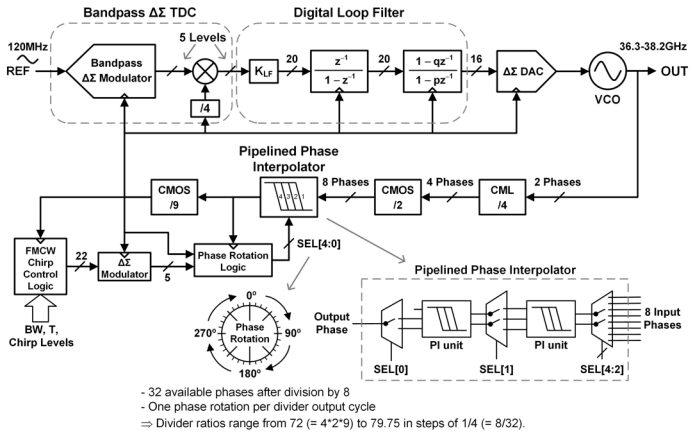


Figure 15.3.2: Fractional-N chirp synthesizer PLL (top) and pipelined phase interpolator (bottom right).

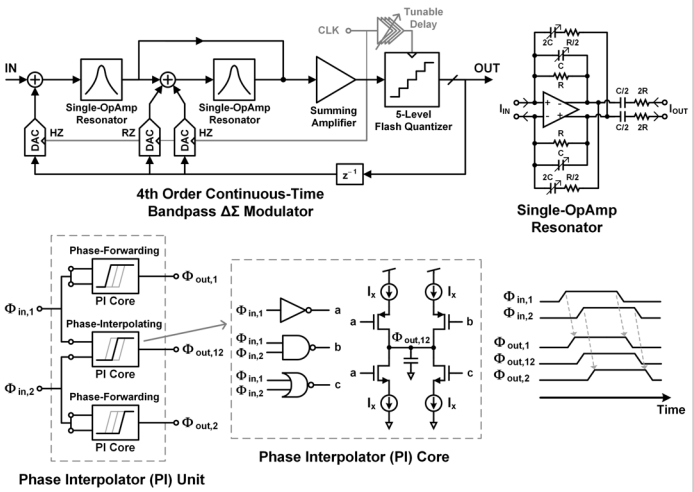
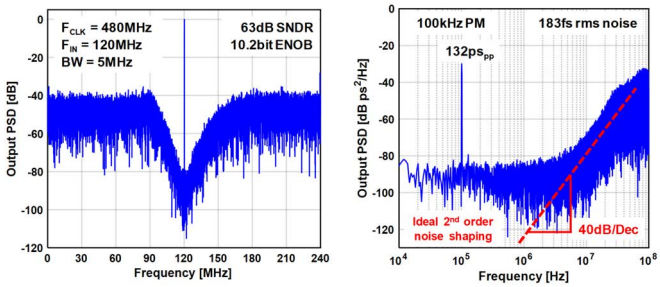


Figure 15.3.3: Bandpass ΔΣ modulator with resonator circuit (top) and PI unit cell with PI core circuit (bottom).



	This work	RFIC'15 Wu	ESSCIRC'15 Dayanik	CICC'13 Yu	ISSCC'12 Elshazly
TDC Type	CTΔΣ	Flash-ΔΣ	CTΔΣ	GSRO	SRO
Technology [nm]	40	40	65	65	90
Integrated RMS noise [fs]	183*	103	176	148	315
Bandwidth [MHz]	2.5	1.25	1	4	1
Sampling frequency [MHz]	240**	50	270	400	500
Power [mW]	7.6	1.32	8.4	6.55	2
Area [mm²]	0.02	0.08	0.055	0.05	0.02

* In a 1MHz bandwidth
** Effective sampling rate

Figure 15.3.4: Measured BPDSM and BPDSTDC output power spectra (top) and comparison of noise-shaping TDCs (bottom).

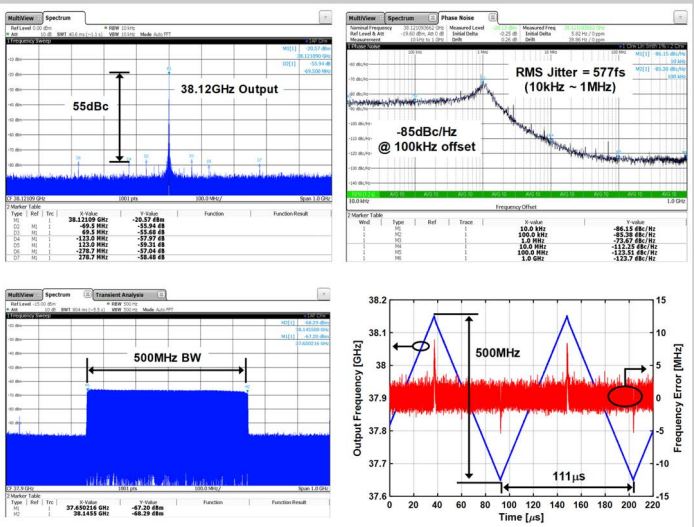


Figure 15.3.5: PLL output spectrum with measured phase noise (top) and FMCW chirp spectrum and profile (bottom).

	This work	ISSCC'16 Yeo	JSSC'14 Wu	ISSCC'11 Sakurai	JSSC'10 Lee	JSSC'10 Mitomo
PLL Architecture	Digital Frac-N	Digital TPM	Digital TPM	Mixed-Mode	Analog Frac-N	Analog Int-N +DDFS
TDC Type	CTΔΣ	Linear	Delay Chain	Delay Chain	--	--
Calibration required	No	Yes	Yes	No	No	No
Technology [nm]	40	65	65	65	65	90
Frequency range [GHz]	36.3-38.2	8.4-9.4	56.4-63.4	82.1-83.8	75.6-76.3	78.1-78.8
Ref. frequency [MHz]	120	277	10-100	26	700	77
Spur level [dBc]	-55	--	-74	--	-40	--
Phase Noise @100kHz [dBc/Hz]	-85	-102	-72	-52	-88	-68
Norm. Phase Noise @100kHz [dBc/Hz²] *	-216	-216	-207	-196	-217	-207
Supply [V]	0.9/1.1/1.2	1.2	1.2	1.2	1.2	1.2
Power [mW]	68	14.8	48	152	73	101
Area [mm²]	0.18	0.18	0.48	1.7	0.16**	0.63**
Chirp period [µs]	50-2000	5 - 220	210-4100	2000-10000	1000-1500	500
Chirp slope [MHz/µs]	9.1	32.63	4.76	1.5	0.97	2.46
RMS freq. error [MHz]	0.82	1.9	0.38	0.18	0.3	1.05

* Phase Noise – 20log(Division Ratio) – 10log(F_{REF})
** Estimated from die micrograph

Figure 15.3.6: Performance comparison with prior-art CMOS FMCW chirp synthesizer PLLs.

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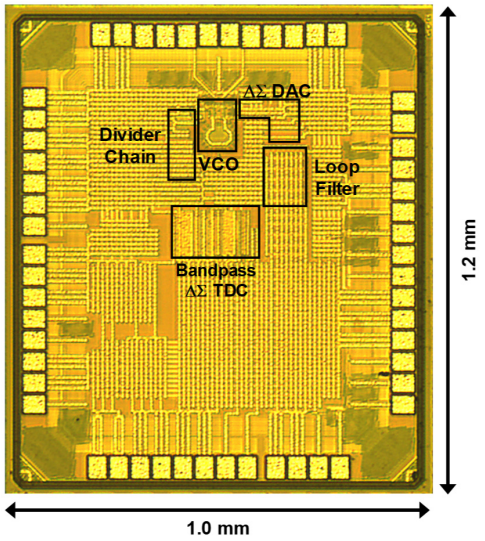

Figure 15.3.7: Die micrograph.

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