Digital Fractional-*N* PLLs Based on a Continuous-Time Third-Order Noise-Shaping Time-to-Digital Converter for a 240-GHz FMCW Radar System

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***Abstract*— Frequency-modulated continuous-wave (FMCW) radar requires low in-band phase noise, fast-settling high-frequency phase-locked loops (PLLs). We propose a new third-order continuous-time time-to-digital converter (TDC) that shapes quantization noise so that the TDC quantization noise no longer determines the in-band phase noise of a digital PLL. The new TDC allows a digital PLL to have an in-band phase noise performance similar to that of an analog PLL. Prototype 30- and 40-GHz PLLs, fabricated in 65-nm CMOS as sources for a 240-GHz scanning FMCW radar, consume 34.8 and 40 mW, respectively. The 30-GHz prototype PLL has a normalized phase noise of −213 dBc/Hz^2 (at 100-kHz offset) and an FoM$_{\text{Jitter}}$ of −230 dB (from 10 kHz to 1 MHz), thanks to the measured 182 fs integrated rms noise of TDC.**

***Index Terms*— Continuous-time sigma delta (CTΣΔ), fractional-*N*, frequency-modulated continuous-wave (FMCW) radar, high-frequency digital phase-locked loop (PLL), noise shaping, time-to-digital converter (TDC).**

I. Introduction

RECENT improvements in silicon technology have enabled highly integrated millimeter-wave (mm-wave) radar transceiver circuits [1]–[3]. In particular, frequency-modulated continuous-wave (FMCW) radar [4], [5] is very attractive because of its coherent transceiver structure. In FMCW radar, the range and velocity resolution depend on the quality of a linear frequency sweep known as a chirp signal. Over the years, fractional-*N* phase-locked loops (PLLs) have emerged as useful tools for generating this chirp signal, because a PLL can efficiently create and linearly modulate a high-frequency clock. However, although mostly digital PLLs are much smaller and far more flexible than analog PLLs, a fundamental problem for digital PLLs is the conflict between settling speed and in-band phase noise. The root of this problem is the large quantization noise of existing time-to-digital converters (TDCs). This paper focuses on improving the in-band phase noise and lock time of digital fractional-*N* PLLs, thereby improving the range and velocity resolution of FMCW radar. We introduce a new TDC architecture that breaks the TDC quantization noise limitation of a digital fractional-*N* PLL.

The conflict between wide loop bandwidth and low in-band phase noise has limited high-frequency (>10 GHz) PLLs [6] to integer-*N* operation for low-phase noise or restricted loop bandwidths and settling speed [7]. This occurs because in fractional-*N* PLL, a wide loop bandwidth passes more of the quantization noise from the ΣΔ-modulator-controlled divider, and more of the reference clock jitter and charge pump (CP) noise. Recent study decouples settling time and phase noise by using two-point modulation (TPM) [8]. However, TPM either requires gain calibration [9] or extra settling time [8] and thereby restricts the TPM schemes to only a single type of chirp signal.

Digital PLLs are limited by the accuracy and noise of existing TDCs [10]. Although some sub-picosecond TDCs have been reported [11], high-frequency digital PLLs (>10 GHz) tend to have at least a 10 dB higher in-band phase noise [12] than their analog counterparts. Reference [13] introduces a 60-GHz digital fractional-*N* PLL but requires several calibration techniques for the TDC to achieve low in-band phase noise. Reference [14] introduces a transformer-based fractional-*N* digital PLL to achieve good phase noise and wide tuning range with minimal area but relies on a 10-nm FinFET technology. Hybrid PLLs combine the advantages of both analog and digital PLLs [15], but the use of two loops increases design complexity and overall area. In practice, today's high-frequency (>10 GHz) PLLs are analog [6], [7] and the flexibility and small area of digital PLLs have yet to be achieved.

To overcome these challenges, we introduce a new noise-shaping TDC based on a third-order continuous-time sigma delta (CTΣΔ). This new noise-shaping TDC technique reduces the in-band phase noise of the digital PLL to that of an analog PLL. Thanks to the new TDC, the PLL benefits from digital circuit advantages such as compact size, configurability, and reliability while satisfying the low phase noise and fast settling time requirements. The new PLL architecture generates the complex waveforms needed for a high-performance mm-wave radar. To show the effectiveness of this new technique, we present high-frequency digital PLL

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prototypes as signal sources for an imaging and navigation 240-GHz scanning radar.

This paper is organized as follows. In Section II, we briefly review the PLL characteristics required for the chirp waveform and then outline the architecture of the 240-GHz scanning radar for which our prototype PLLs are designed [16]. Section III introduces the proposed third-order CT$\Sigma\Delta$-based noise-shaping TDC architecture. Section IV focuses on the fractional-N PLL architecture along with its sub-blocks. In Section V, we analyze the noise contribution of our TDC within an integer-N PLL and show that the quantization noise is negligible in our TDC. We show that a digital PLL with the proposed TDC can achieve the same phase noise performance as an analog PLL. Section VI describes the ramp generator block within the PLL. Finally, in Section VII, we present measurement results of the prototype TDC and PLLs and conclude this paper in Section VIII.

II. PLL as Chirp Generator for an FMCW Radar

A. Requirements for PLL as Radar Chirp Generator

Range resolution (ΔR) and velocity resolution (ΔV) are important parameters that define the performance of an FMCW radar. These parameters are determined by the speed, phase noise, and linearity of the chirp signal. The absolute frequency sweep (ΔF) and linearity of the chirp signal define the range resolution (ΔR) according to $\Delta R = c/(2 * \Delta F)$, while the modulation period (T_P) and the operating center frequency (F_C) affect the velocity resolution (ΔV) according to $\Delta V = c/(2 * T_P * F_C)$, where c is the speed of light [17].

For short-range (<200 m) FMCW radar systems, a fast chirp signal ($T_P < 150\ \mu$s) is desirable because this keeps the down-converted received baseband signal above the flicker noise range of the active devices [5]. In addition, a fast chirp suppresses the additional noise due to the reflected power or ground clutter from large targets beyond the radar range [18]. In addition to speed, chirp linearity is critical because any nonlinearity in the chirp signal creates frequency errors in down conversion and worsens the radar resolution [19]. To keep frequency deviation of a chirp signal within 1% relative to a perfect sawtooth waveform, the PLL loop bandwidth needs to be at least 100 times larger than the chirp modulation frequency [19]. Moreover, the ramp signal should have low phase noise because phase noise makes it difficult to detect moving targets and estimate velocity in the presence of ground clutter [20], [21]. Therefore, emerging high-performance radars require fast, linear, and low-noise chirp waveforms. However, generating fast chirp waveforms with good linearity and low phase noise is challenging (Fig. 1) especially for high-frequency PLLs.

B. 240-GHz Radar Architecture

Recent developments in silicon technology have enabled a commercial short-range (<200 m) 77-GHz FMCW radar. However, there is a need for even higher frequencies to reduce antenna size and weight. Our prototype PLL supports a 240-GHz scanning FMCW radar that uses a compact and lightweight traveling-wave frequency-scanning antenna array

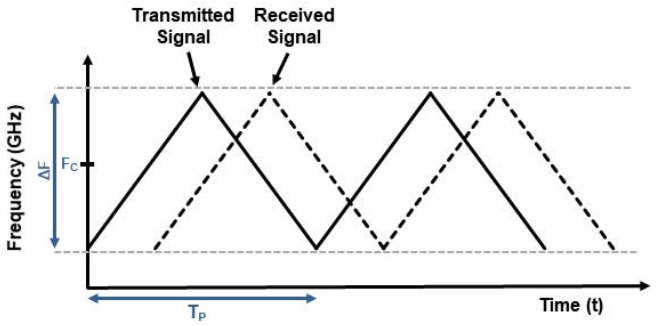

Fig. 1. Transmitted and received signals in an FMCW system with triangular chirp signal.

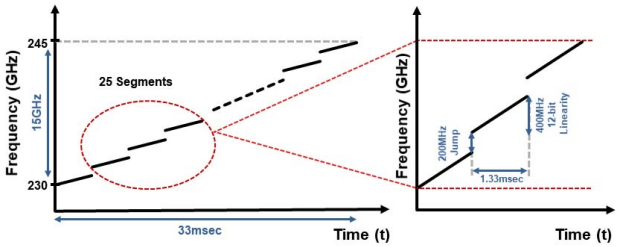

Fig. 2. Traveling-wave frequency scanning antenna and the required 25-segment linear chirp signal.

so that the beam is also scanned (i.e., steered) by varying the feed frequency [16]. This 240-GHz radar scans a 2° beam over a ±25° field of view at 30 frames/s (fps). Beam scanning [16] relies on the fixed time delay between antenna slots and varying the feed frequency from 230 to 245 GHz scans the beam over the 50° range (Fig. 2). Each beam angle has a 40-cm range resolution.

The combination of scanning and FWCW make it challenging to generate the frequency waveform. A combination of a frequency doubler and a tripler multiplies the 38.33–40.83-GHz PLL output to the required 230–245-GHz frequency range. The radar uses 25 400-MHz chirp segments, each separated by 200 MHz (Fig. 2) [16]. A 33-ms period enables the 30-fps rate. Thanks to the frequency multiplication in the 240-GHz radar architecture (Fig. 3), the PLL needs only to generate a 25-step 38.33–40.83-GHz sawtooth signal with each segment a 66.66-MHz linear chirp (400 MHz/6 = 66.66 MHz). There is a 33.33-MHz frequency step (200 MHz/6 = 33.33 MHz) between each segment. Although the entire frequency sweep has a period of 33 ms, the frequency step between each segment requires the PLL lock time to be less than 4 μs to minimize the spectral leakage to unwanted angles and to enhance the directivity of the radar. A 1-MHz PLL loop bandwidth is chosen to satisfy this 4-μs lock time requirement.

III. Time-to-Digital Converter

In this section, before introducing our third-order CT$\Sigma\Delta$-based noise-shaping TDC, we briefly review the conventional TDC. Then, we introduce our noise-shaping TDC architecture and explain how it shapes quantization noise.

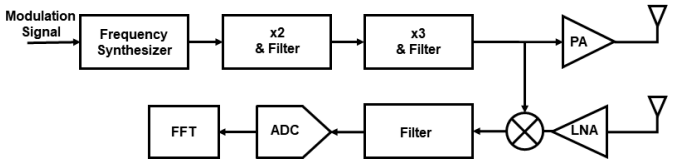

Fig. 3. Block diagram of the 240-GHz FMCW radar system.

A. Overview of Time-to-Digital Converters for Digital PLLs

In general, the quantization noise of a TDC determines the in-band phase noise of a wideband digital PLL. Various architectures have been proposed to improve the TDC time resolution. A delay-line TDC is a simple solution, but its resolution highly depends on unit cell delay (e.g., 6 ps for 40 nm and 11 ps for 65-nm CMOS technology). A Vernier TDC improves time resolution by delaying both input and reference clocks, but this doubles the number of delay cells required [22]. Reference [23] combines a coarse and a fine TDC with a time amplifier, but the time amplifier limits the linearity of the TDC. In [24], a synchronous pipeline TDC is presented to improve the time resolution. As all these approaches are Nyquist TDCs, and therefore, the quantization noise of the delay cells and their linearity limits the resolution. For this reason, Nyquist TDCs are restricted to a time resolution of around 1 ps. References [11], [25], and [26] introduce noise shaping to further improve time resolution beyond that of Nyquist TDCs. Although, these approaches reduce the integrated rms noise within the TDC bandwidth to sub-picosecond levels, they either suffer from dead-zone problems [25] that reduce the effective resolution or they cannot support a full 2π phase range of the reference clock [11]. Reference [26] is vulnerable to leakage of the quantization noise from the first stage to the output due to imperfect matching between the analog and digital transfer functions.

B. Third-Order Continuous-Time Sigma Delta-Based Noise-Shaping TDC

We introduce a third-order noise-shaping TDC [27] that takes advantage of noise shaping in a CT$\Sigma\Delta$ modulator to achieve excellent (<200 fs) integrated rms noise. Our new approach removes the quantization noise limitation of the TDC and allows us to reach the noise performance of an analog PLL with a digital PLL. In the new TDC (Fig. 4), a phase–frequency detector (PFD) converts the phase difference between the TDC input and the reference clock to a pulsewidth-modulated (PWM) signal where the PWM duty cycle (i.e., the dc component) represents the phase difference. A CP converts this PWM voltage signal to the current domain and feeds it to a single-bit third-order CT$\Sigma\Delta$ modulator. Finally, the CT$\Sigma\Delta$ modulator filters the higher order harmonics of the PWM signal and digitizes the dc component while shaping the quantization noise. Thanks to the noise-shaping benefits of a CT$\Sigma\Delta$ modulator, we suppress both quantization noise and comparator thermal noise.

The first two blocks of the TDC are a conventional PFD and a CP circuit (Fig. 5). The PFD is formed with two D-flip-flops

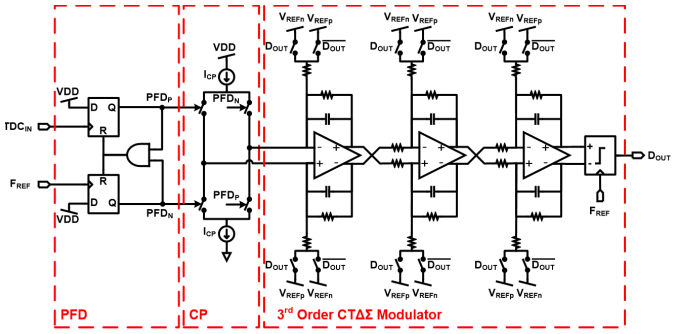

Fig. 4. Schematic of the third-order CT$\Sigma\Delta$-based noise shaping TDC.

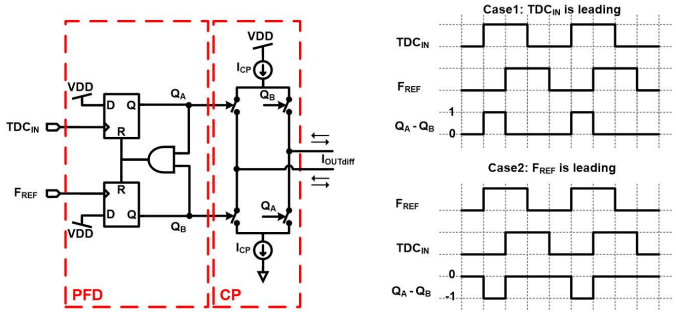

Fig. 5. Schematic of the PFD with two possible timing diagrams.

and an AND gate and generates a PWM voltage signal. The duty cycle of the PWM signal depends on the phase difference between the input (i.e., $\mathrm{TDC_{IN}}$) and the reference clock (i.e., F_{REF}), while the location of the pulse (i.e., whether it is at the Q_A or Q_B output) indicates whether the TDC input or the reference clock is leading. After the PFD, a CP converts the PWM voltage to a current waveform and feeds this current signal to the CT$\Sigma\Delta$ modulator.

The CT$\Sigma\Delta$ modulator filters the PWM waveform and digitizes the dc component, which represents the phase difference between the PLL reference and the feedback signal. As with any PWM signal, the output of the PFD and CP, shown in Fig. 6, can be represented as a sum of cosines

$$x(t) = a_0 + \sum_{n=1}^{\infty} a_n \cos\ (2\pi F_{\mathrm{REF}} t n)$$

where

$$a_0 = Ad, \quad \text{and } a_n = \frac{2A}{n\pi} \sin(n\pi d) \tag{1}$$

where the a_n coefficients are the amplitudes of cosine waves with frequencies that are multiples of the reference frequency (i.e., F_{REF}), d is the duty cycle, and A is the amplitude of the PWM signal. As Fig. 6 and (1) show, the dc component (i.e., a_0) is linearly related to the duty cycle of the PWM signal and, therefore, represents the phase difference between the TDC input and the reference clock. On the other hand, the amplitudes of the higher order harmonics are nonlinear functions of the phase difference, and so these harmonics should be filtered out.

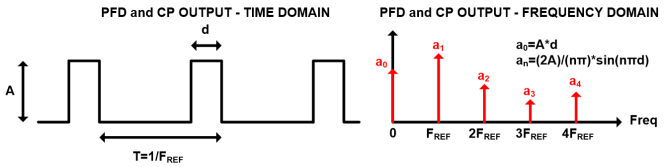

Fig. 6. PFD and CP output in time domain and frequency domain.

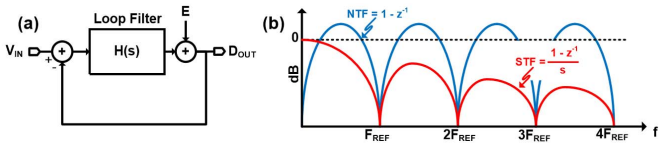

Fig. 7. (a) CTΣΔ modulator linearized model. (b) Signal and noise transfer functions of a first-order CTΣΔ modulator.

CTΣΔ modulators filter and digitize an analog input and shape quantization noise. A CTΣΔ modulator [Fig. 7(a)] can be modeled as a two-input (i.e., $V_{\rm IN}$ and E) and one-output (i.e., $D_{\rm OUT}$) system, where $V_{\rm IN}$ is the analog input and E represents the uniformly distributed quantization noise. The digital output (i.e., $D_{\rm OUT}$) of a CTΣΔ modulator is a linear combination of $V_{\rm IN}$ and E

$$D_{\rm OUT} = {\rm STF} * V_{\rm IN} + {\rm NTF} * E \tag{2}$$

where STF is the signal transfer function and NTF is the noise transfer function.

For a first-order CTΣΔ modulator [28], [29], the STF and NTF are

$${\rm STF} = \frac{1 - z^{-1}}{s} \quad \text{and} \quad {\rm NTF} = 1 - z^{-1} \quad \text{where } z = e^{s}. \tag{3}$$

As Fig. 7(b) and (3) show, the STF has a low-pass characteristic with notches at the reference clock frequency (i.e., $F_{\rm REF}$) and its harmonics, while the NTF has a high-pass characteristic.

Our TDC architecture uses the signal and noise transfer functions of the CTΣΔ modulator to both enhance the TDC resolution and filter out the higher order harmonics of the PFD/CP output while digitizing only the dc component. Both the CTΣΔ modulator and the PFD use the same reference clock. Thanks to its STF, the CTΣΔ modulator filters out multiples of the reference frequency (i.e., $F_{\rm REF}$) of the PWM signal [Fig. 8(a)]. In other words, the notches of the STF cancel out the reference frequency multiples in the PFD signal. As a result, the CTΣΔ modulator digitizes only the dc component of the PWM signal. In addition, the NTF of the CTΣΔ modulator shapes quantization noise [Fig. 8(b)] via high-pass filtering and, therefore, enhances the TDC resolution within the PLL bandwidth. As shown in Fig. 8(c), the CTΣΔ modulator digitizes the phase difference between the reference clock and TDC input while achieving excellent time resolution within the PLL bandwidth. Although the NTF amplifies high-frequency quantization noise, this shaped noise is filtered by the digital loop filter of the PLL, as explained in Section IV.

We carefully choose the loop filter transfer function [i.e., $H(s)$ in Fig. 7(a)] and its implementation style to shape the quantization noise and to suppress the CP current noise.

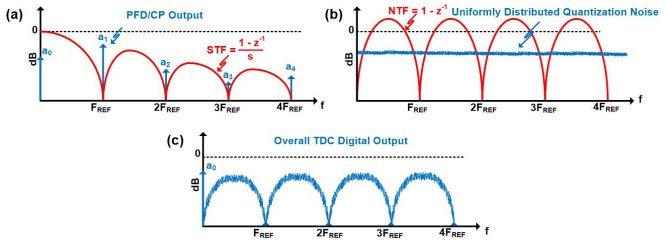

Fig. 8. (a) PFD/CP frequency-domain output and CTΣΔ modulator STF. (b) Normally distributed quantization noise and CTΣΔ modulator NTF. (c) Overall TDC digital output in frequency domain.

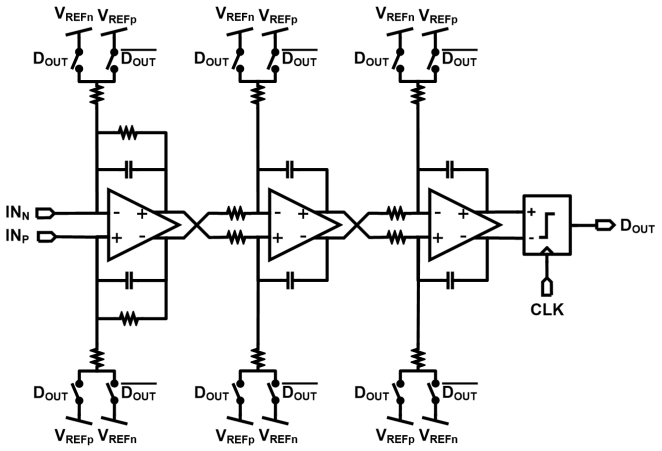

Fig. 9. Schematic of third-order 1-bit CTΣΔ modulator.

Compared to the first- and second-order modulators, the third-order CTΣΔ modulator (Fig. 9) is much less susceptible to limit cycles, which would create distortion in the modulator output and limit dynamic range [29]. More importantly, the third-order noise shaping enables a finer resolution in the chosen bandwidth. In this paper, we set the CTΣΔ modulator's effective bandwidth equal to the PLL's 1-MHz closed-loop bandwidth. Also, the third-order modulator has a third-order low-pass filter (LPF) characteristic in its signal transfer function which suppresses CP noise. The third-order loop filter is implemented as a distributed feedback topology with active *RC* integrators. Unlike feed-forward topologies, the distributed feedback architecture does not suffer from STF peaking. To improve the linearity of the TDC, we use a single-bit quantizer and an inherently linear single-bit resistive-feedback digital-to-analog converter (DAC).[1]

The proposed TDC is an oversampling TDC and, hence, requires a reference clock frequency higher than its bandwidth. Fortunately, this TDC is specifically designed to be used in a digital PLL which itself is an oversampled system. Although increasing the reference clock frequency helps to reduce the TDC quantization noise, it comes with the cost of increased power consumption. However, if needed, this effect can easily be mitigated by using slower reference clock frequency along with a multi-bit quantizer and a lower order loop filter in the CTΣΔ modulator. In our application (i.e.,

[1] As with analog PLLs, the PLL performance is susceptible to current mismatch of the CP current sources. These currents are trimmable in the prototype.

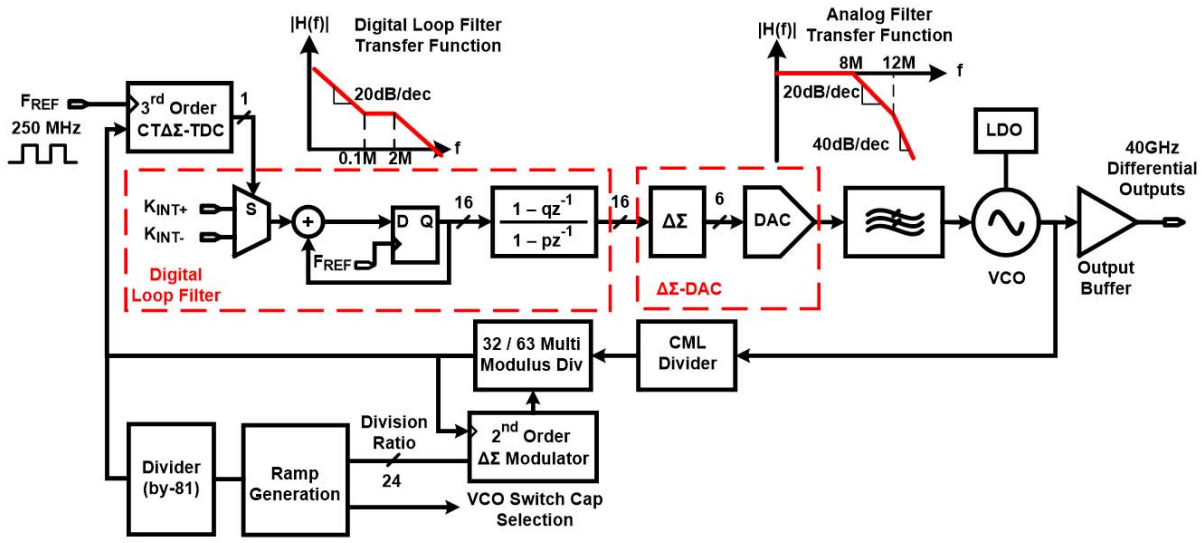

Fig. 10. Block diagram of the 34.2–39-GHz PLL prototype for a MAST radar system.

240-GHz FMCW radar), the power consumption of the PLL is negligible compared to that of the frequency doubler, tripler, and PA, and therefore, we use a 1-bit quantizer for better linearity.

IV. PLL Architecture and Implementation

This section describes how the design of the PLL (Fig. 10) and how it filters the high-frequency shaped quantization noise of the TDC. The third-order CT$\Sigma\Delta$-TDC uses the PLL reference clock (i.e., F_{REF}) as its sampling clock and converts the phase difference between F_{REF} and feedback divided clock to an oversampled, noise-shaped 1-bit digital output stream. The CT$\Sigma\Delta$-TDC shapes the quantization noise to higher frequencies, and the fourth-order (analog and digital) PLL loop filter suppresses this shaped noise. The CT$\Sigma\Delta$-TDC quantizer output directly feeds to a digital accumulator that functions as an integrator to make the PLL a type-II system. Every clock cycle, the 1-bit TDC quantizer output determines the sign of a digital word, K_{INT}, that is added to the accumulator. The coefficient, K_{INT}, sets the open-loop gain of the PLL, and therefore, the closed-loop bandwidth can be easily adjusted. After the integrator, a 16-bit digital filter with a pole at 2.2 MHz and a zero at 110 kHz stabilizes the type-II loop by setting the closed-loop bandwidth of the PLL to 1 MHz and the phase margin to 50° (Fig. 11). After this digital filter, a second-order $\Sigma\Delta$-DAC converts the filtered digital signal into the analog domain to control the voltage-controlled oscillator (VCO). Completing the PLL loop, the VCO output is divided by a prescaler and then by a modulo-N divider before being fed back to the TDC input.

There are three main sources of high-frequency noise source in the PLL: the TDC, the $\Sigma\Delta$-DAC, and the $\Sigma\Delta$-modulator-driven modulo-N divider. Our prototype PLL filters these noise contributions in both digital and analog domains. Since the prototype TDC has a third-order noise-shaping architecture, the PLL requires at least a fourth-order LPF, or in other words four poles. The prototype PLL is a type-II system and, therefore, inherently has two poles at dc, one due to the digital accumulator and the other due to the VCO.

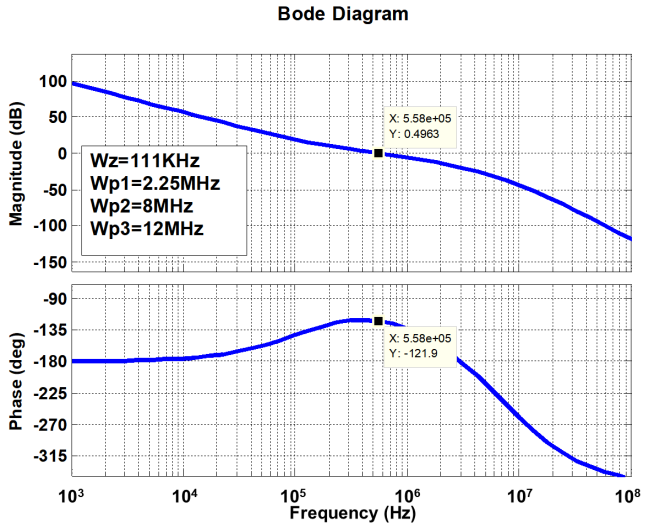

Fig. 11. Bode plot of the PLL open-loop transfer function.

To achieve fourth-order filtering, in addition to the digital pole implemented by the accumulator, there is a second-order, analog, *RC* LPF with poles at 8 and 12 MHz (Fig. 10). This second-order low-pass analog filter suppresses not only the TDC quantization noise but also the shaped quantization noise of the $\Sigma\Delta$-DAC. This $\Sigma\Delta$-DAC before the VCO [30] is a second-order modulator. Therefore, a second-order analog filter combined with the VCO transfer function (i.e., an integrator) creates a third-order filter that sufficiently attenuates the shaped high-frequency $\Sigma\Delta$-DAC noise.

Shaped noise from the modulo-N divider is fourth-order filtered by the PLL filters (i.e., both digital and analog), and also filtered by the STF of CT$\Sigma\Delta$ modulator in the TDC. However, the use of so many filters in a PLL requires careful selection of the filter pole locations so that the CT$\Sigma\Delta$ modulator's third-order STF does not affect the PLL loop dynamics. For instance, the first dominant pole of the CT$\Sigma\Delta$ modulator's STF is placed at 20 MHz, which is 20 times larger than the targeted PLL bandwidth. The poles of the second-order analog LPF are located at 8 and 12 MHz.

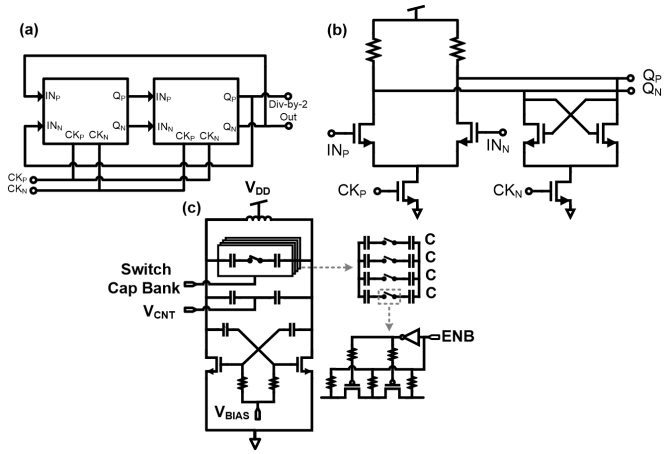

Fig. 12. (a) Schematic of divide-by-2 circuit. (b) Schematic of the CML latch in the divide-by-2 circuit. (c) 34.2–39-GHz *LC*-VCO.

In the feedback path, a high-speed differential current-mode logic (CML) divider formed by two consecutive divide-by-2 circuits [Fig. 12(a)], where each divide-by-2 circuit is composed of two high-speed differential latches [Fig. 12(b)], divides the output of the *LC*-VCO by 4. The divided output is fed to a CMOS 32/63 multi-modulo divider. A digital ramp generator controls the multi-modulo divider for fractional-N operation and also sets the coarse control of the VCO via a switchable capacitor bank. The VCO is an NMOS *LC*-VCO for low phase noise and high speed [Fig. 12(c)]. An amplitude redistribution technique [31] sets the gate dc voltage of the cross-coupled transistors to be less than their drain voltages thereby reducing the VCO phase noise by keeping the cross coupled transistors away from the triode region. A switched-capacitor bank increases the frequency range of the VCO. The PLL directly controls the varactor voltage, whereas the switched capacitor bank is programmed by the ramp generator.

Even though the proposed PLL architecture is similar to an analog PFD/CP PLL, unlike an analog PLL, the PLL loop bandwidth of this digital PLL can be easily adjusted from very low frequencies (i.e., 1 kHz) to moderate frequencies (i.e., 5 MHz) without increasing the PLL area while still satisfying the in-band phase noise performance of an analog PLL. This is because, in this PLL, the pole and zero locations are set by a digital filter rather than by the capacitor and resistor sizes as in an analog PLL.[2]

V. Analysis of Third-Order CTΣΔ-TDC Noise Within a PLL

We now analyze the noise performance of the TDC within an integer-N digital PLL to show that the quantization noise of the TDC does not determine the in-band phase noise of the digital PLL. In fact, a digital PLL with this TDC architecture can reach the noise performance of an analog PLL because in-band phase noise of both traditional analog and digital

[2]For instance, for a 1-kHz loop bandwidth, an analog PLL requires a 360-nF capacitance assuming 4-kΩ zero resistance) to set the zero location at 110 Hz (i.e., 1/10th of the PLL bandwidth).

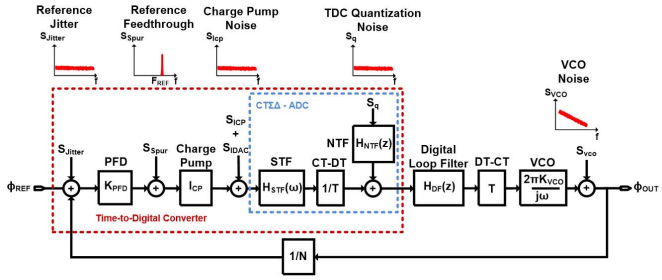

Fig. 13. Small signal model of the CTΣΔ-TDC within an integer-N digital PLL.

PLLs with the proposed TDC is limited by CP noise and PFD noise. Even though the CTΣΔ modulator in our TDC architecture has additional noise sources such as quantization noise, DAC noise, and loop-filter opamp noise, these can be either shaped to higher frequency and filtered out by the PLL filter or minimized during design.

We analyze the noise performance of the TDC in an integer-N digital PLL using the small signal model shown in Fig. 13. Since our architecture uses a 1-bit quantizer, the quantization noise of the comparator is much bigger than its thermal noise, and therefore, these are combined in this analysis. To further simplify the analysis, the divider noise is referred to the PFD and the CTΣΔ modulator's DAC noise is combined with the CP noise. Usually, the input of a CTΣΔ modulator is a voltage source, therefore, the DAC noise current and input voltage noise need to be separated. In our TDC architecture, the CP current is the input to the CTΣΔ modulator, and therefore, its noise can be combined with the DAC current noise. This is because both current noise sources are integrated and combined by the first integrator.

The signal transfer function (i.e., STF in Fig. 13) of the CTΣΔ modulator is represented as $H_{\mathrm{STF}}(\omega)$, while the quantizer noise transfer function is shown as $H_{\mathrm{NTF}}(z)$. Although there are several noise sources in the PLL, only reference feedthrough (i.e., S_{Spur}), CP noise (i.e., S_{ICP}), DAC current noise (i.e., S_{IDAC}), and quantization noise along with comparator thermal noise (i.e., S_q) come from the TDC. The thermal noise of CTΣΔ modulator loop filter opamp is made insignificant by design and, therefore, excluded from this analysis. From Fig. 13, the effect of the TDC noise sources on the PLL phase noise (i.e., S_{OUT}) is

$$\begin{aligned} &S_{\mathrm{OUT}}(\omega) \\ &= \left|\frac{N}{K_{\mathrm{PFD}}} * G(\omega)\right|^2 * S_{\mathrm{Spur}}(\omega) \\ &\quad + \left|\frac{N}{K_{\mathrm{PFD}} * I_{\mathrm{CP}}} * G(\omega)\right|^2 * \left(S_{I_{CP}}(\omega) + S_{I_{\mathrm{DAC}}}(\omega)\right) \\ &\quad + \frac{1}{T} * \left|\frac{N * T}{I_{\mathrm{CP}} * H_{\mathrm{STF}}(\omega) * K_{\mathrm{PFD}}} * G(\omega)\right|^2 \\ &\quad * |H_{\mathrm{NTF}}(e^{j\omega T})|^2 * S_q(\omega) \end{aligned} \tag{4}$$

where $G(\omega) = (\mathrm{PLL\_LoopGain})/(1 + \mathrm{PLL\_LoopGain})$, $H_{\mathrm{NTF}}(e^{j\omega T}) = (1 - e^{j\omega T})^L$, N is the division ratio, K_{PFD} is the PFD gain, I_{CP} is the CP gain, $H_{\mathrm{STF}}(\omega)$ is a signal

transfer function of the CT$\Sigma\Delta$ modulator, T is the sampling clock period, L is the loop filter order, S_{ICP} is the CP noise, S_{IDAC} is the DAC current noise, S_q is the combination of TDC quantization noise and the comparator thermal noise, and S_{OUT} is the PLL phase noise. At low frequencies, within the loop bandwidth of the PLL, PLL_LoopGain is much larger than 1, and therefore, the magnitude of $G(\omega)$ is equal to 1. Furthermore, for low frequencies where PLL in-band phase noise is considered, the magnitude of CT$\Sigma\Delta$ modulator STF at very low frequency [i.e., close to dc or $H_{\text{STF}}(\omega \approx 0)$] is set to $1/I_{\text{CP}}$ and the PLL phase noise at low frequencies due to TDC can be simplified as

$$S_{\text{OUT}}(\omega) = \left(\frac{N}{K_{\text{PFD}}}\right)^2 * \left[\left(\frac{S_{I_{\text{CP}}}(\omega) + S_{I_{\text{DAC}}}(\omega)}{I_{\text{CP}}^2} + S_{\text{Spur}}(\omega)\right) + |1 - e^{j\omega T}|^{2L} * T * S_q\right]. \quad (5)$$

We see that the effect of CP noise (i.e., S_{ICP}) and reference feedthrough (i.e., S_{Spur}) on the PLL phase noise are identical to that of an analog PLL.

Compared to an analog PLL, the additional noise sources within the PLL bandwidth are the DAC current noise (i.e., S_{IDAC}) and the TDC quantization error combined with the comparator thermal noise [i.e., $S_q(\omega)$]. However, S_q (ω) is modified by $(1-e^{j\omega T})^{2L}$, which has a high-pass characteristic, so that both quantization noise and comparator thermal noise are substantially suppressed at low frequencies. For instance, the prototype TDC has a 250-MHz reference sampling clock, a 1-MHz bandwidth, a third-order loop filter, and therefore, at 1 MHz, the spectral density of the quantization noise and the comparator thermal noise are attenuated by 200 dB. Fig. 14(a) shows the simulated TDC noise for three different conditions. The red line is quantization and comparator noise only. The orange line includes the DAC and opamp noise and finally blue line includes all noise sources including the CP noise, which dominates. The noise simulations of the TDC indicate an integrated noise of 141 fs within a 1-MHz bandwidth. This value includes the CP noise, PFD noise, DAC current noise, quantization noise and comparator thermal noise. On the other hand, thanks to the noise-shaping characteristics of the TDC and the 200-dB attenuation factor, the simulated integrated quantization noise including the comparator thermal noise is only 52 fs within the same bandwidth, even with a 1-bit quantizer. According to [11], the effective resolution of a TDC is the integrated rms noise within the bandwidth which in this case is 141 fs.[3] According to [32], the equivalent number of bits (ENOB) of a TDC is $\text{ENOB} = (20 * \log_{10}(\text{Range}_{2\pi}/\text{int}_{\text{noise}}) - 1.76)/6.02$, where $\text{Range}_{2\pi}$ is half of the reference period and $\text{int}_{\text{noise}}$ is the integrated rms noise within the bandwidth. Therefore, based on the simulation results, the ENOB of our third-order TDC is 13.5 bits. The effect of TDC noise on the PLL in-band phase noise can be calculated from $S_{\text{OUT}}(f) = ((2\pi)^2/12) * |(\Delta T/T_0|^2 * (1/F_{\text{REF}})$ [10], where $\Delta T = \sqrt{12 * \text{OSR}} * \text{int}_{\text{noise}}$ [32], T_0 is the VCO oscillation period and F_{REF} is the reference frequency. Therefore, the contribution of our noise-shaping TDC to the in-band phase noise of a 30-GHz PLL with a 250-MHz reference frequency is estimated as -91.5 dBc/Hz. Fig. 14(b) shows phase noise simulations of the 30-GHz PLL considering three different noise sources: TDC quantization noise and VCO noise only, TDC thermal noise only, and including all noise sources. According to these simulations, the in-band phase noise of the PLL is limited by the TDC thermal noise and not by quantization noise. Just as in an analog PLL, the dominant thermal noise source is the CP. Therefore, this approach can achieve an in-band noise performance comparable to that of an analog PLL.

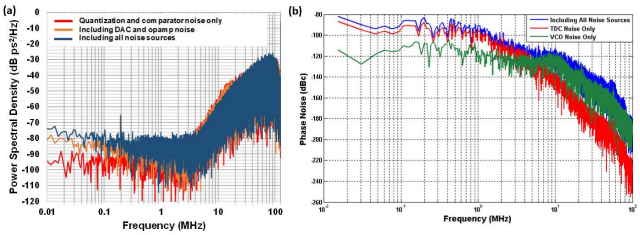

Fig. 14. (a) Simulated TDC noise for three different noise conditions when a single 600-fs_{pp} 200-kHz tone is given as the input: quantization and comparator noise only (red line), including DAC and opamp thermal noise (orange line), including all noise sources (blue line). (b) 30-GHz PLL phase noise simulation with Cppsim including three different noise sources. Green line: VCO noise and TDC quantization noise only. Red line: TDC thermal noise only. Blue line: including all noise sources.

VI. Ramp Generator Block

The ramp generation block (Fig. 15) controls the output frequency of the PLL to create the 25-step, linear segment, frequency sweep for the radar, by producing the necessary division ratio values for the divider and by controlling the coarse tuning of the VCO. The ramp generator block is based on a custom-designed synchronous logic circuit to reduce the required number of memory units. The prototype PLL uses one-point modulation, and therefore, we tune the output frequency by changing the division ratio of the divider and by selecting the correct number of switched capacitors in the VCO. Although it is possible to do this by storing each required division ratio along with the corresponding switched capacitor setting, such an approach consumes a lot of die area. Instead, we minimize the required number of memory elements by only storing the division ratio value for the start of each of the 25 segments and not for the entire ramp. The slope of the ramp is controlled by a digital word called the *division ratio step*. In this way, the division ratio lookup table needs only 25 registers. Similarly, the coarse switched capacitor lookup table also has 25 registers and stores only one-switched capacitor value for each segment. Since, the VCO has a large enough frequency tuning range for each ramp segment, we do not need to alter the switched capacitor configuration within each segment.

[3]Wu *et al*. [32] compare noise shaping TDC resolution with an oversampled Nyquist TDC with perfect matching using $\Delta T = \sqrt{(12 * \text{OSR})} * \text{int}_{\text{noise}}$, where OSR is the oversampling ratio and $\text{int}_{\text{noise}}$ is the TDC integrated rms noise within the bandwidth. To achieve the same noise performance as our noise shaping TDC, such an ideal oversampled Nyquist TDC operating with the same OSR would require a unit delay of 5.4 ps, which is half of the minimum propagation delay of 65-nm CMOS ($\sim$11 ps).

TABLE I

TDC PERFORMANCE SUMMARY AND COMPARISON WITH THE STATE-OF-THE-ART NOISE SHAPING TDCS

	This Work	Y. Wu [RFIC 2015]	A.Elshazly [ISSCC 2012]	Y. Cao [ISSCC 2011]	C. Hsu [ISSCC 2008]	B. Young [CICC 2010]
Technology [nm]	65	40	90	130	130	90
Supply [V]	1.2	1.1	1	1.2	1.5	1.2
Power [mW]	8.4	1.32	2	1.7	21	2.1
Bandwidth [MHz]	1	1.25	1	0.1	1	1
Type	CTΣΔ	Flash-ΣΔ	SRO	MASH	GRO	ΣΔ
Area [mm^2]	0.055	0.08	0.02	0.11	0.04	0.12
Fs [MHz]	250	50	500	50	50	156
Integrated$_{RMS}$ Noise [fs]	182	103	315	5600	80	2400
Range$_{2\pi}$ [ns]	2	0.32	5	10	0.564	3.2
DR[(a)] (dB)	80.8	70	84	65	77	62.5
ENOB[(b)] [bits]	13.13	11.3	13.7	10.5	12.5	10.1
FoM$_{2\pi}$[(c)] [pJ/step]	0.47	0.2	0.08	5.8	1.8	0.96

(a) DR=20*log$_{10}$(Range2π/Integrated$_{RMS}$ Noise)

(b) ENOB=(DR-1.76)/6.02

(c) FoM$_{2\pi}$=Power/(2*BW*2^{ENOB})

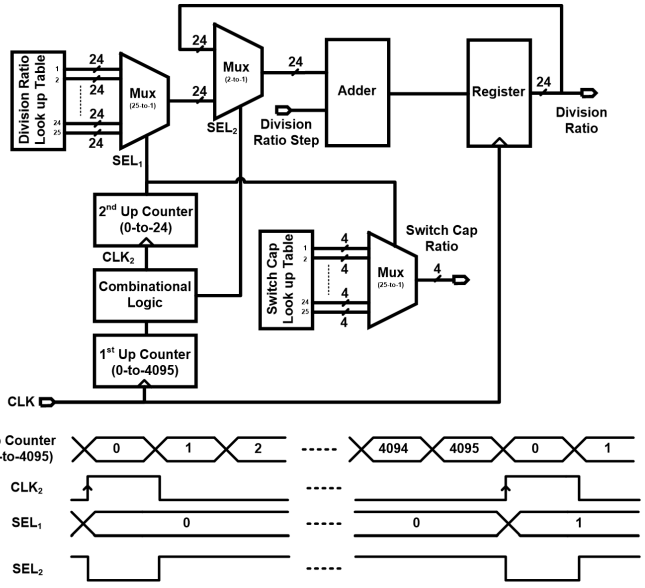

Fig. 15. Block diagram and timing diagram of the ramp generator.

The ramp generator block has two up-counters: the step counter and the segment counter. The step counter increments from 0 to 4095 to generate 4096 small steps for each segment and the segment counter increments from 0 to 24 to indicate the starting points of each segment, which is where each frequency jump occurs. The synchronous logic adds the division ratio step to the previous value of the division ratio each time the step counter increments. When the step counter completes all the 4096 cycles, the segment counter increments by one and selects the next starting division ratio for the next segment and the switched capacitor value for the VCO coarse tuning.

VII. MEASUREMENT RESULTS

We implemented two prototype high-frequency digital PLLs in a 65-nm CMOS. The first prototype is a 34.2–39-GHz fractional-*N* PLL incorporating a digital ramp generator, while the second is a 28.5–33.5-GHz fractional-*N* PLL. For both PLLs, the TDC sampling frequency is the 250-MHz PLL reference frequency (i.e., F_{REF}). The devices are packaged in QFN packages. To fully quantify the performance of the fabricated prototypes, we measure both TDC and PLL characteristics.

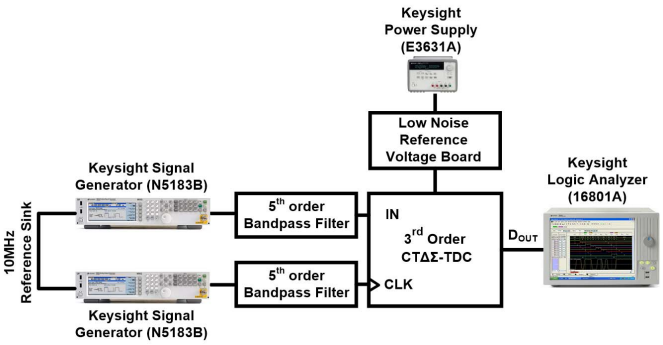

Fig. 16. TDC integrated noise test measurement setup.

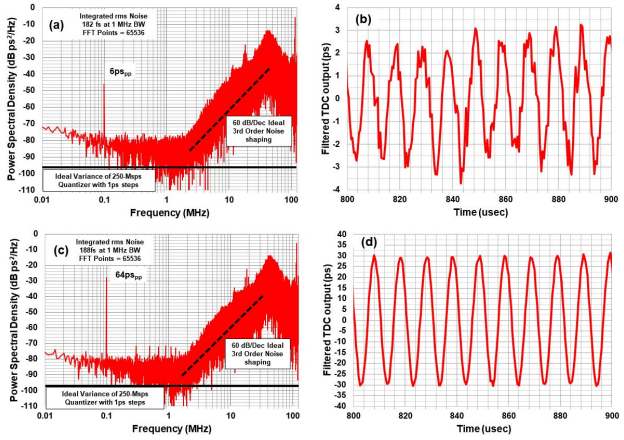

Fig. 17. (a) Measured output spectrum of the TDC (10 KHz–125 MHz) (6-ps$_{PP}$ 100-kHz sinusoidal input signal). (b) Measured TDC output filtered by a 1-MHz digital LPF and decimated by 125. (c) Measured output spectrum of the TDC (10 kHz–125 MHz) (64-pspp 100-kHz input). (d) Measured TDC output filtered by a 1-MHz digital LPF and decimated by 125.

A. Time-to-Digital Converter Measurements

We performed stand-alone TDC measurements to characterize the performance of the TDC. To minimize jitter mea-

TABLE II
PLL (OVER 10 GHz) PERFORMANCE SUMMARY AND COMPARISON

	This Work [30GHz PLL]	This Work [40GHz PLL]	V. Szortkya [ISSCC 2014]	X.Yi [ISSCC 2013]	W. Wu [JSSC 2014]	M. Ferris [VLSI 2013]	M. Ferris [ISSCC 2015]	A. Hussein [ISSCC 2017]	C. Li [VLSI 2016]
Technology [nm]	65	65	40	65	65	32 [SOI]	32 [SOI]	65	10 [Finfet]
Type	DigFrac-N	DigFrac-N	AnalogInt-N	AnalogInt-N	DigFrac-N	Hybrid Int-N	Hybrid Frac-N	DigFrac-N	DigFrac-N
Tuning Range [GHz]	28.5 – 33.5	34.2 - 39	53.8 - 63.3	57.9 - 68.3	56.4 - 63.4	23.8 – 30.2	13.1 – 28	50-66	10.8-19.3
Ref. Freq [MHz]	250	250	40	135	100	200	100	100	150
Freq. Resolution [MHz]	0.004	0.004	40	135	10 – 100	NA	NA	0.04	NA
Bandwidth [MHz]	1	1	NA	NA	0.5	1	1	NA	1
Phase Noise @ 100kHz [dBc/Hz]	-87	NA	-87	-85.5	-72	-84	-80	-85	-87
Area [mm^2]	0.18	0.217	0.16	0.19	0.48	0.03	0.24	0.45	0.034
Power [mW]	34.8	40	42	24.6	48	32	31	46	11.9
Supply [V]	1.2	1.2	0.9/1	1.2	1.2	1	1	1	0.8
Norm. Phase Noise @100kHz [dBc/Hz^2] [a]	-212.6	NA	-226.2	-220.2	-207.6	-209.9	-206.4	-220.2	-206.8
Jitter$_{RMS}$ [fs] [b]	545	NA	287	238	779	468	945	261	565
FoM$_{Jitter}$ [dB] [c]	-229.9	NA	-234.6	-238.6	-225.4	-231.5	-225.6	-235.0	-234.2

[a] Norm Phase Noise = Phase Noise – 20log(Division Ratio) – 10log(Reference Frequency)
[b] Jitter$_{RMS}$ is calculated from phase noise plots from 10kHz-to-1MHz for all PLLs
[c] FoM$_{Jitter}$ = 10log[(Jitter$_{RMS}$/1s)^2*Power/1mW]

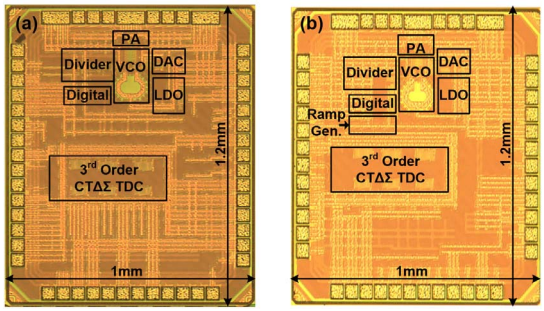

Fig. 18. (a) 30-GHz fractional-*N* PLL die micrograph. (b) 40-GHz fractional-*N* PLL die micrograph.

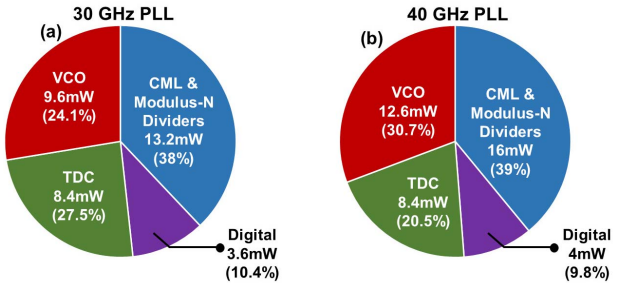

Fig. 19. Power consumption distribution of the prototypes. (a) 30-GHz PLL. (b) 40-GHz PLL.

surement errors (Fig. 16), we use two low-phase noise signal generators (Keysight 5183B), one to provide the reference clock and the other as the phase-modulated input source to the TDC. The two signal generators were locked to a low phase noise 10-MHz reference. The TDC reference clock frequency was set to constant 250 MHz, and a phase-modulated signal around 250 MHz was applied to the TDC input. The TDC was tested with 6 and 64 ps$_{pp}$ inputs.

Fig. 17(a) shows the frequency-domain TDC outputs when an input with 6-ps$_{pp}$ amplitude at 100 kHz was applied to the TDC input. The TDC output power spectral density shows third-order noise shaping with a 60-dB/decade slope. The integrated rms noise for a 1-MHz bandwidth is 182 fs. Fig. 17(b)

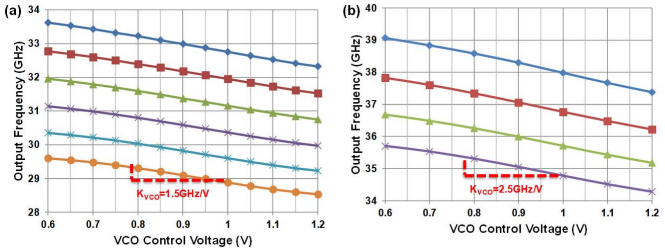

Fig. 20. (a) 30-GHz *LC*-VCO open-loop oscillation frequency versus control voltage. (b) 40-GHz *LC*-VCO open-loop oscillation frequency versus control voltage.

shows the time-domain digital output of the TDC after it is digitally filtered with a 1-MHz bandwidth and decimated by 125. Fig. 17(c) shows frequency-domain measurements of the TDC when the input amplitude is increased to 64 ps$_{pp}$. Again, the TDC output shows the third-order noise-shaping characteristics and the calculated integrated rms noise in a 1-MHz bandwidth is 188 fs (176 fs excluding harmonics). As mentioned in Section III-C, the simulated integrated rms TDC noise in a 1-MHz bandwidth is 141 fs, which is very consistent with this 182-fs measurement. Fig. 17(d) shows the time-domain digital output of the TDC of the 64-ps$_{pp}$ signal at 100 kHz after it digitally filtered with a 1-MHz bandwidth and decimated by 125. Based on these noise measurements, the dynamic range of the TDC is calculated as 81 dB, using the equation $\mathrm{DR} = 20 * \log(\mathrm{Range}_{2\pi}/\mathrm{integrated}_{\mathrm{noise}})$ [1], where $\mathrm{Range}_{2\pi}$ is 2 ns and integrated noise is 182 fs. Thus, the ENOB is 13.2 bits. The TDC consumes 8.4 mW from 1.2 V, and thus, the energy efficiency (FoM$_W$) of the TDC is calculated as 446 fJ/conv-step using $\mathrm{FoM}_W = \mathrm{Power}/(2*\mathrm{BW}*2^{\mathrm{ENOB}})$. Table I shows the measured performance of the TDC and compares it with the state-of-the-art noise-shaping TDCs. The prototype 65-nm CMOS TDC occupies 0.055 mm^2.

B. Phase-Locked Loop Measurements

Both PLLs are fabricated in TSMC 65 nm. The 28.5–33.5-GHz (i.e., 30 GHz) fractional-*N* PLL has an

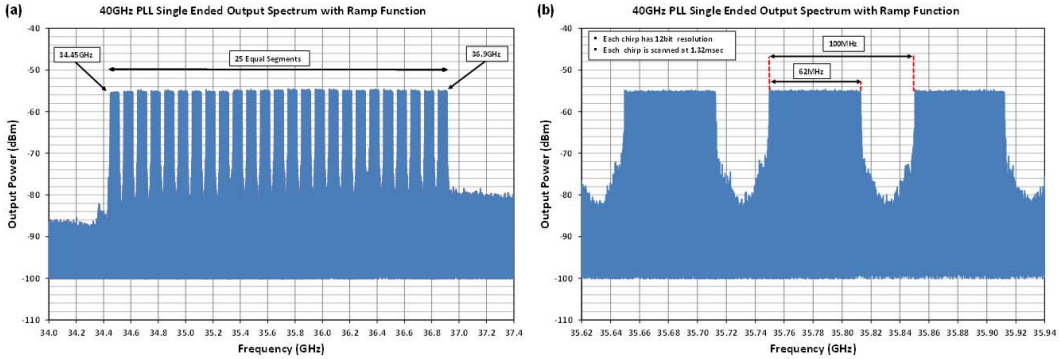

Fig. 21. Measured output spectrum of the 40-GHz PLL when the ramp generation function is enabled. (a) Full spectrum from 34.4 to 36.9 GHz. (b) Zoomed-in view of spectrum from 35.6 to 35.9 GHz to see three segments.

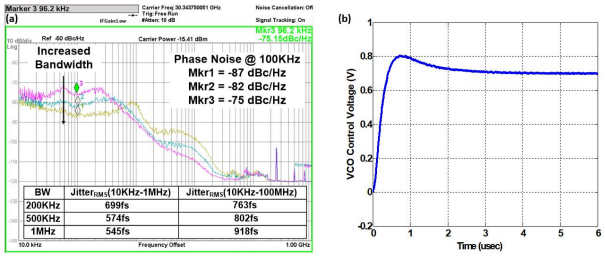

Fig. 22. (a) Phase noise measurements of single-ended output of the 30-GHz PLL for low (200 kHz), medium (500 kHz), and high (1 MHz) bandwidth settings at 30 GHz measured with a Keysight N9010A signal analyzer. (b) Simulated settling time of the PLL when its bandwidth is set to 1 MHz.

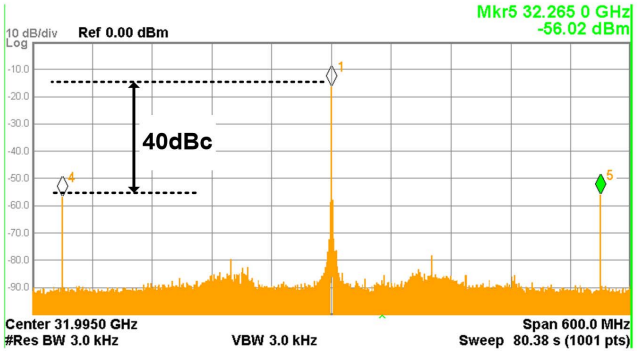

Fig. 23. Single-ended output spectrum of the 30-GHz PLL when it is locked to 32.2 GHz.

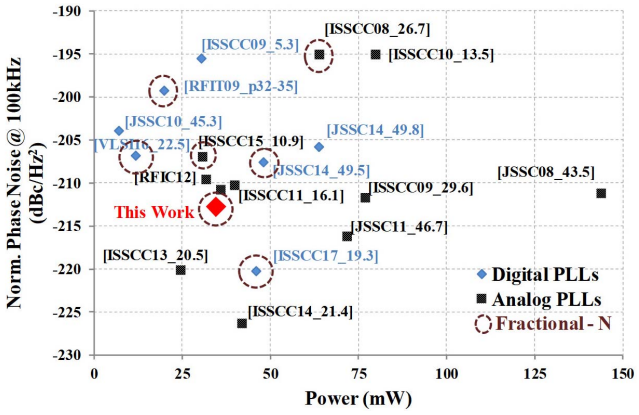

Fig. 24. 30-GHz PLL normalized phase noise at 100 kHz comparison with analog and digital PLLs faster than 10 GHz.

active area of 0.18 mm^2 [Fig. 18(a)], and the 34.2–39-GHz fractional-N PLL (i.e., 40 GHz) has an active area of 0.217 mm^2 [Fig. 18(b)]. The 30-GHz PLL consumes 34.8 mW, while the 40-GHz prototype uses 40 mW from a 1.2-V supply. Fig. 19 shows the power consumption distribution of both PLLs. Fig. 20 shows the measured VCO open-loop oscillation frequency for both PLLs. The ramp generation function of the 40-GHz PLL is recorded with a spectrum analyzer (Fig. 21). The output is composed of 25 segment chirp signal ranging from 34.45 to 36.9 GHz.

The effectiveness of the TDC for in-band phase noise reduction in the 28.5–33.5-GHz fractional-N PLL is measured for three different PLL bandwidth conditions (200 and 500 kHz and 1 MHz) [Fig. 22(a)] for a division ratio of 129.06. The measured in-band phase noise at a 100-kHz offset for 200- and 500-kHz loop bandwidths is −75 and −82 dBc/Hz, respectively. For the highest loop bandwidth case (1 MHz), the in-band phase noise is measured as −87 dBc/Hz at a 100-kHz offset. For a 1-MHz PLL bandwidth, Cppim estimates the settling time of the PLL as 4 μs [Fig. 22(b)]. This measured phase noise is very consistent with the −91.5-dBc/Hz in-band phase noise calculated in Section VII-A.[4] This measured phase noise corresponds to an integrated rms jitter from 10 kHz to 1 MHz of 545 fs, resulting in an FoM$_{\text{Jitter}}$ of −230 dB and the normalized in-band phase noise of −212.6 dBc/Hz^2. The reference spur is −40 dBc when the PLL is locked to 32.265 GHz with a 129.06 division ratio, as shown in Fig. 23.[5] Table II summarizes the performance of both 30- and 40-GHz prototype PLLs and compares with the state-of-the-art digital and analog PLLs faster than 10 GHz. Fig. 24 compares the

[4]As we increase the bandwidth of the TDC, we notice an increase at the phase noise of the PLL around 10 MHz, and we believe this related the second-order shaped noise of a modulo-N divider.

[5]We believe this reference frequency spur comes mainly from the delta sigma DAC that drives the VCO. To satisfy the FMCW radar requirements, the 30-GHz and 40-GHz PLLs have 1.5 and 2.5 GHz/V VCO gains, respectively. Even though we use a 6-bit DAC for the conversion, the reference spur level can still be relatively high depending on the switching of the DAC due to high VCO gain.

normalized phase noise of the 30-GHz PLL with the state-of-the-art digital and analog PLLs over 10 GHz.

VIII. Conclusion

FMCW radar requires low in-band phase noise, fast settling high-frequency PLLs. However, fast settling demands a wide loop bandwidth that conflicts with the requirements for low in-band phase noise, because a wide loop bandwidth passes more of the TDC noise. To solve this problem, a new third-order continuous-time TDC shapes quantization noise so that the TDC quantization noise no longer determines PLL in-band phase noise. This allows a digital PLL to have an in-band phase noise performance similar to that of an analog PLL. The prototype TDC is fabricated in 65-nm CMOS and has a measured integrated rms noise of 182 fs in a 1-MHz bandwidth, 81-dB dynamic range, and 13.2 bit of ENOB. To prove the effectiveness of the TDC, we fabricate a 30-GHz fractional-*N* digital PLL in 65-nm CMOS. The prototype has a measured phase noise of -87 dBc/Hz at 100-kHz offset and a normalized phase noise of -213 dBc/Hz^2.

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