A Mismatch-Immune 12-bit SAR ADC With Completely Reconfigurable Capacitor DAC

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***Abstract*—We overcome mismatch constraints of capacitor DAC design in SAR ADCs using a completely reconfigurable DAC with content addressable memory beneath groupings of unit capacitors. We demonstrate a linearity optimization technique in simulation and measurement. We achieve a nearly 2-bit repeatable ENOB improvement with a peak of 11.3 bits.**

I. Introduction

SAR ADCs have enjoyed increasing prominence due to their inherently scaling-friendly architecture. Several recent SAR ADC innovations [1], [2], focus on decreasing power consumption, mitigating thermal noise, and improving bandwidth, however most of those using non-hybrid architectures are limited to moderate (i.e. 8-10 bit) resolution. Assuming a nearly rail-to-rail dynamic range, comparator noise and DAC element mismatch constraints are critical but not insurmountable at 10 bits or less in sub-100nm processes. On the other hand, analysis from [3] in Fig. 1 shows that for medium-resolution ADCs (11-15 bits, depending on dynamic range), the mismatch sizing constraint still dominates unit capacitor sizing over the kT/C sampling noise constraint, and can only be mitigated by drawing increasingly larger capacitors.

The focus of this work is to extend the scaling benefits of the SAR architecture to medium and higher ADC resolutions through mitigating and ultimately harnessing DAC element mismatch. We do so via a novel, completely reconfigurable capacitor DAC that allows the rearranging of capacitors such that mismatch between capacitor groupings can be canceled. In section II we discuss mismatch in traditional DACs and propose DAC element reconfigurability as a solution. We describe details of the DAC in section III. In section IV we describe an intuitive approach to reconfiguration. We implement the DAC in an asynchronous SAR ADC described in section V. In section VI we present the performance measurements of the ADC and confirm our linearity optimization technique with a nearly 2-bit increase in measured ENOB.

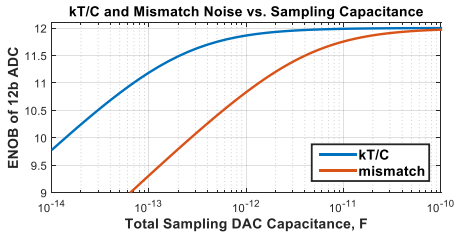

Fig. 1. ENOB comparison of otherwise ideal 12b ADC from kT/C sampling noise and noise from unit element mismatch. A 2V differential full-scale input is used in calculations.

II. Mismatch and Reconfigurability

In traditional capacitor DACs, the assignment of individual capacitors to SAR trial groupings is made during layout. The unit capacitors are hard-wired into groups whose relative sizes determine the radix of the SAR algorithm. Thus in traditional DACs, linearity is solely determined by the mismatch characteristics of the fabrication process, requiring calibration at medium or higher resolutions. Recent work [4], [5], [6], mitigates mismatch effects by adjusting a *specific* capacitor or groups of capacitors, while other methods [7] use tuneable sub-DACs or capacitors beneath a unit capacitor.

In our new approach to DAC design, we describe our DAC as "*completely* reconfigurable" because *any* capacitor can be assigned to any trial grouping in the SAR cycle, post-fabrication, independent of layout. We first discuss how mismatch constrains traditional DACs, then how our DAC overcomes this via reconfigurability.

A. Mismatch in Traditional DACs

For an N-bit capacitor DAC arranged in N binary-weighted switching groups, the DNL of all 2^N codes can be determined with just N unique DNL measurements of the major code transitions, e.g. 0100 $\rightarrow$ 1000 [3]. The linearity of these binary-weighted code transitions is determined by each group's fractional mismatch, γ_i, which is defined in (1) as the ratio of the mismatch of the i^{th} group to its ideal size:

$$\gamma_i = \frac{\Delta C_i}{C_{i,nominal}} \ (i^{th} \text{ group fractional mismatch})$$

where:

$$C_{i,nominal} = \sum_{1}^{2^i} C_{UNIT} \text{ ideal size of } i^{th} \text{ group}$$

$$\Delta C_i = \sum_{1}^{2^i} \Delta C_{UNIT} \text{ total mismatch of } i^{th} \text{ group} \quad (1)$$

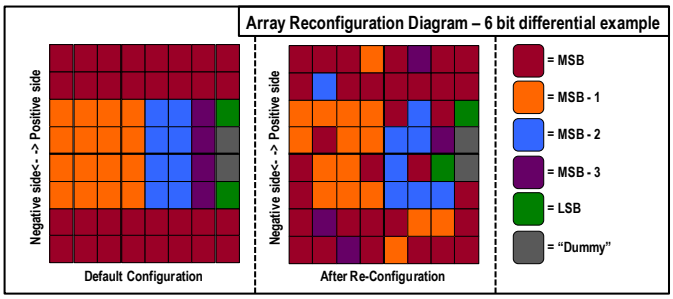

Fig. 2. Before-and-after example of arbitrary layout-independent DAC reconfiguration.

[3] ultimately derives the ENOB of a differential DAC as a function of these fractional mismatch parameters as (2):

$$ENOB = N - \log_4[1 + 3\gamma_0^2 + 3\sum_{i=1}^{N-1}(2^{i-1}\gamma_i)^2] \quad (2)$$

Because ΔC_{UNIT} is a function of a fabrication process's area proportionality constant from [8], the only way to reduce ΔC_{UNIT} and thus γ_i is by drawing larger capacitors. This is the mismatch constraint of traditional, hard-wired DACs.

B. Overcoming Mismatch via Reconfigurability

This work severs the previously described relationship between ENOB and unit element mismatch by removing the hard-wired constraint. In our new approach to DAC design, we describe our DAC as completely reconfigurable because any capacitor can be assigned to any trial grouping in the SAR cycle, after fabrication, independent of layout. A 6-bit differential DAC example of this layout-independent reconfiguration is shown in in Fig. 2. This novel reconfigurability provides the ability to *re*-group capacitors such that their mismatches cancel. For this DAC like any other there is a certain amount of C_{UNIT} mismatch from fabrication, however one is no longer forced to tolerate it, or over-size DAC elements to minimize it. Fig. 3 shows an example where a sea of 8 unit capacitor elements are laid out in a 2×4 array. In this example, a binary weighted group of $4 \times C_{UNIT}$ is desired. The initial (red) grouping exhibits detrimental mismatch where its four elements sum to $4 \times C_{UNIT}$. With the ability to create a different group after fabrication, one can now select the blue grouping in which the four elements sum to the intended $4 \times C_{UNIT}$.

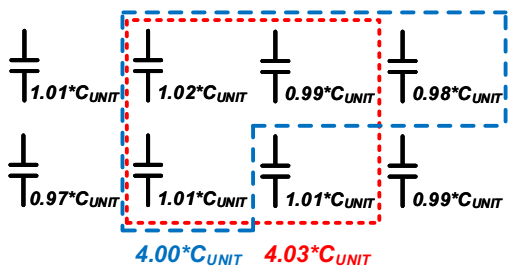

Fig. 3. Initial mismatched grouping (red) vs. reconfigured and corrected grouping (blue).

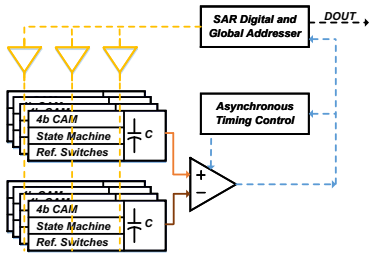

Fig. 4. Conceptual diagram of DAC and SAR ADC system.

III. Completely Reconfigurable Capacitor DAC

In a conventional SAR ADC, because the groupings of unit capacitors are predetermined during layout, the logic that decides whether to switch each trial grouping between voltage references can be very simple; a shift-register or counter-based approach is common. In this work where cells are not predetermined in layout, the traditional reference switching control logic must be distributed to each cell, while a central addressing system controls which cell groups are activated.

Fig. 4 shows a conceptual diagram of our 12-bit DAC and ADC system, which resembles a typical SAR loop where the DAC has been replaced with a grouping of capacitor cells containing unit elements. The capacitor cells in our DAC differ from typical DAC elements by their addition of 4 bits of Content Addressable Memory (CAM) and a state machine within each cell. The CAM provides the ability to selectively group cells post-fabrication while the state machine provides the reference switching control logic.

A more detailed representation of the reconfigurable DAC is shown in Fig. 5. The reconfigurable DAC is constructed with 16 rows and 17 columns of capacitor cells. The DAC is a symmetric, differential pairing of two arrays; rows 1-8 are the positive side of the DAC while rows 9-16 are the negative side. The cells in columns 1-16 on both sides of the array contain groupings of 4 unit capacitors ($4\times$ cells), while the cells in column 17 contain 1 unit capacitor ($1\times$ cells). This results in 521 unit capacitors on each side of the DAC,

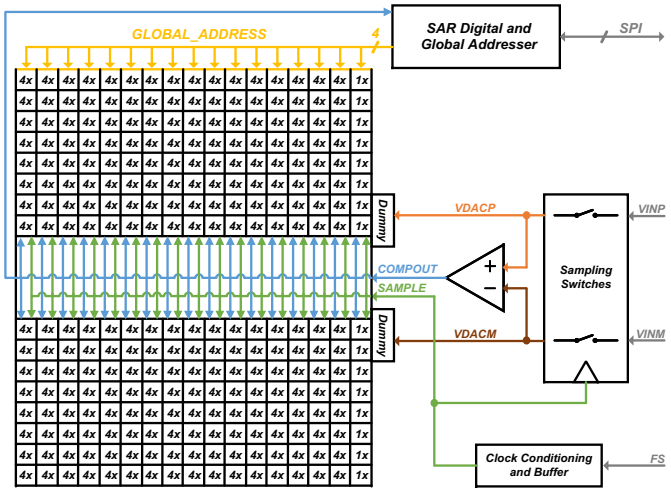

Fig. 5. Conceptual diagram of DAC and SAR ADC system.

TABLE I
DEFAULT BINARY-WEIGHTED ARRAY PROGRAMMING

SAR Trial Group	Num. of Cells $\times C_{UNIT}$	Reference During Sampling	Binary 4-bit Address
1*	32×4	V_{REFP}	0010
	32×4	V_{REFM}	0011
2*	16×4	V_{REFP}	0110
	16×4	V_{REFM}	0111
3*	8×4	V_{REFP}	1110
	8×4	V_{REFM}	1111
4*	4×4	V_{REFP}	1010
	4×4	V_{REFM}	1011
5	4×4	V_{REFP}	1000
6	2×4	V_{REFP}	1100
7	1×4	V_{REFP}	0100
8	2×1	V_{REFP}	0101
9	1×1	V_{REFP}	1101
10	1/2	V_{REFP}	$UNIT_1$*
11	1/4	V_{REFP}	$UNIT_2$*
12	N/A**	V_{REFP}	$SAMPLE**$

* Groups with same decision are switched differentially
$UNIT_X$* Done by 2-bit sub-DAC beneath C_{DUMMY}
$SAMPLE**$ After final decision initiate sampling

corresponding to a 9-bit array with 9 additional unit capacitors. A 2-bit resistor ladder sub-DAC is connected to the dummy capacitor on each side. The sub-DAC is used for the final two SAR trials, yielding a total differential DAC resolution of 12 bits.

A. DAC Operation

Complete reconfigurability is achieved by activating programmable groups of capacitors during the steps of SAR operation via their CAM. SAR group activation is controlled by the global addresser which is shown in both Figs. 4 and 5. The global addresser is a 4-bit wide, 13-state long chain of flip-flops that cycles through the CAM memory addresses as shown in Table I. All cells in each SAR trial grouping share the same unique 4-bit memory programming, and thus each cell's CAM programming determines its bit in the SAR cycle. The global addresser sends the 4-bit words to every column of the DAC, where they are buffered for reliable operation and span both positive and negative arrays. The entire DAC receives the same address simultaneously, so that a cell's physical location does not restrict its assignment options. Four bits of CAM are needed because there are 13 unique capacitor groups. Table I shows the mapping of 4-bit memory addresses to SAR trial groups.

B. Cell Structure

A 3-D diagram of a DAC cell is shown in Fig. 6. Beneath the MoM capacitors in each cell are the 4 bits of CAM and the state machine that controls the reference switching for the cell's capacitors. The memory is fully re-programmable, so the DAC configuration can be changed at any time. As shown, this logic fits directly under the MoM capacitors in each cell structure so there is minimal area penalty. A simplified

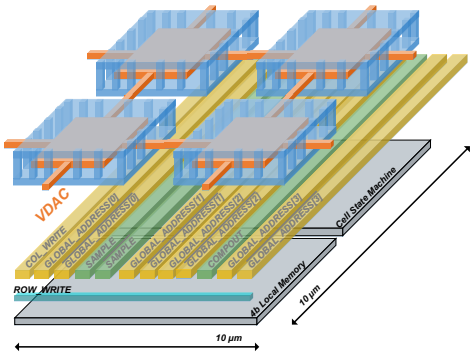

Fig. 6. 3-D diagram of 4x DAC cell.

schematic of a DAC cell is shown in Fig. 7. Every cell in the DAC contains a miniature state machine that controls the reference switching logic at the cell level. This state machine is activated when a cell's local CAM programming matches the 4-bit word being sent across the DAC by the global addresser. Once activated, the state machine monitors the current comparator decision being sent across the array, shown as $COMPOUT$ in Figs. 5 and 7. Depending on the polarity of $COMPOUT$ and the programmed state, the cell will switch the bottom plate of C_{UNIT} to V_{REFP} or V_{REFM} accordingly. This circuitry is identical for every cell in the array. The only difference between $4\times$ cells and $1\times$ cells is the number of bottom plates connected to the reference switches. The only difference between cells in the positive and negative sides of the array is the routing of $COMPOUT$ signals; $COMPOUT$ polarity is reversed for the negative side of the DAC.

IV. RECONFIGURATION TECHNIQUE

With this new reconfigurability in hand, the next objective is to determine how best to reassign the unit cells and redistribute their initial mismatch. The number of possible configurations of unit elements to assemble a 10-bit binary weighted DAC (2^{10}, or 1024 unit elements) is staggering. In the case of a differential 10-bit DAC where each side (positive and negative) has 512 (or 2^9) elements, simply choosing the $MSB1$ grouping of 256 capacitors follows the combinatorics

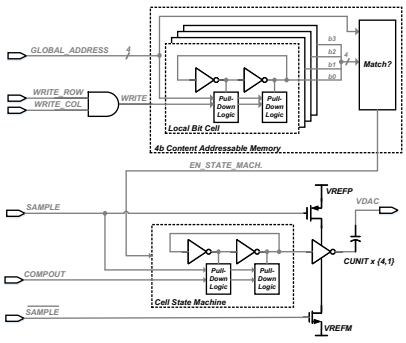

Fig. 7. Simplified schematic of a DAC cell.

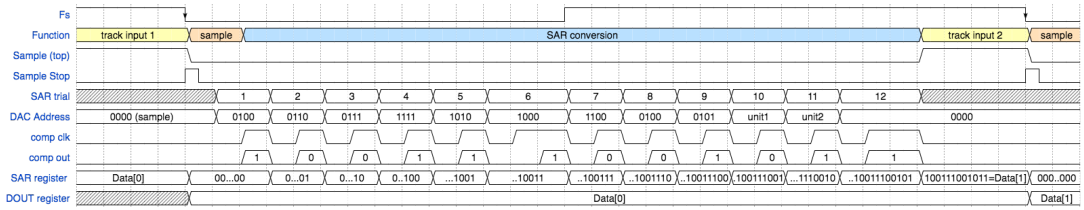

Fig. 8. Timing diagram of ADC.

formula:

$$\binom{512}{256} = \frac{512!}{256!(512-256)!} \simeq 4.725 \times 10^{152} \qquad (3)$$

This work being a proof-of-concept, we chose an intuitive approach to reconfiguration using simple randomization. The authors acknowledge reconfiguration of the DAC lends itself to many optimization algorithms which may be explored in future work. Our optimization algorithm proceeds through the DAC groupings in a random order. First, all cells in the DAC are de-programmed and made available for reconfiguration. Second, a SAR grouping is selected to reconfigure at random. Third, the capacitors for the presently selected SAR group are chosen at random from the cells that have not already been reconfigured. These three steps repeat until the entire DAC has been reconfigured. After all capacitor groups have been reassigned, the ADC ENOB is measured via FFT and stored for comparison, and one random reconfiguration has then been performed. This reconfiguration process repeats a user-defined number of times.

Fig. 9 shows a histogram comparison of 1,000 optimization runs on a single DAC with 2% element mismatch using 25, 50, and 100 reconfigurations per run. As shown, even with as few as 50 reconfigurations the DAC's ENOB improved all of the 1,000 times. Increasing the number of reconfigurations to 100 results in a higher average post-optimization ENOB and tightens the distribution across runs. All following simulation and measured results shown use 100 reconfigurations per optimization run.

Fig. 10 shows a simulated comparison of our algorithm for three different standard deviations of unit mismatch; $\Delta C_{UNIT}/C_{UNIT}$ of 0.1%, 1%, and 3%. The results show that every resulting ENOB is greater than the ENOB of the initial configuration, regardless of mismatch amount. All post-optimization measurements presented beyond this section are the result of this random reconfiguration algorithm.

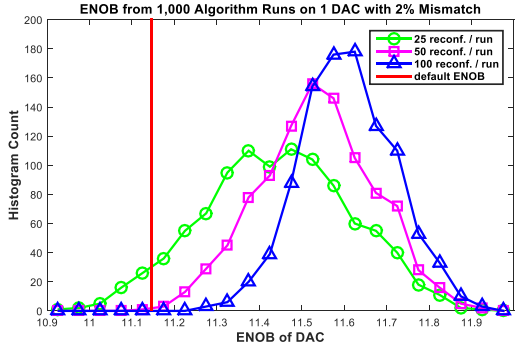

Fig. 9. Simulated ENOB of 1,000 random optimization runs on a single DAC with 2% element mismatch comparing 25, 50, and 100 reconfigurations per run. Using 25 results in $\mu = 11.44$, $\sigma = 0.17$ bits, 50 results in $\mu = 11.53$, $\sigma = 0.13$ bits, and 100 results in $\mu = 11.61$, $\sigma = 0.11$ bits. ENOB of every DAC is improved using 50 or more reconfigurations per run.

V. 12-BIT SAR ADC IMPLEMENTATION

The prototype ADC is fabricated in a 65nm 9-metal process, and a die photo is shown in Fig. 11. As shown in Fig. 6, the MoM unit capacitor structure is a sandwich type using only 3 standard-thickness metal layers. The DAC area is 228μm x 228μm, and the entire area of all circuits except for I/O routing and buffers but including reference decoupling is 0.112 mm^2. The entire die area including I/O pads is 1mm^2.

A timing diagram of ADC operation is shown in Fig. 8, and shows how the sequence of cell activation (DAC Address) and comparator timing for the 12-bit SAR algorithm. The ADC is asynchronous; after the sampling instance the comparator and DAC switching loop is self-timed with the aid of programmable delay cells (implied in Fig. 3) to ensure a minimum time for DAC settling.

The comparator is a slightly modified version of [9], sized up for 10.5-bit noise performance and with offset correction omitted. Better noise performance was desired, yet avoiding the linearity-degrading effects of nonlinear comparator input capacitance was the higher priority. This tradeoff is necessary due to our choice of a pseudo bottom-plate sampling method.

Our pseudo-bottom-plate sampling method disconnects the bottom plates within each cell so that charge injection is not input-dependent, however the input is still sampled onto the top plate of the DAC. This bottom-plate disconnection is performed by the NMOS and PMOS devices surrounding each cell's output inverter in Fig. 7. True bottom-plate sampling, where the input is sampled to the DAC bottom plate while the top plate and comparator inputs are connected to a fixed reference, would have allowed for a larger comparator size as its nonlinear input capacitance would not have affected the sampled charge in an input-dependent manner.

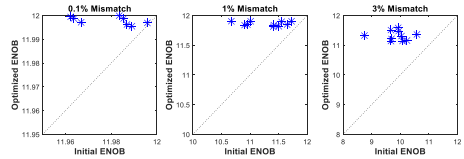

Fig. 10. Simulated results of random optimization: optimized vs. initial ENOB at 0.1%, 1%, and 3% std. dev. unit element mismatch. ENOB of every DAC is improved regardless of mismatch amount.

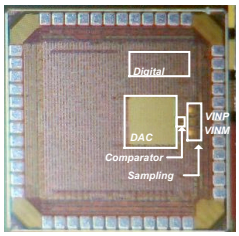

Fig. 11. Die photo of fabricated ADC with critical blocks outlined.

VI. Measurements

All ADC control is via SPI, which along with the number of DFT points determines the time consumed by DAC reconfiguration. Programming every CAM cell individually with a SPI data clock of 2 MHz takes 6.53 ms. The peak ENOB data below and its optimization process used DFTs with 2^{16} points. At the sampling rate of 20 MS/s each DFT took 3.28 ms. The DAC programming and DFT acquisition combine to 9.81 ms per iteration. The total 100-iteration optimization time is just under 1s. As shown in Fig. 9 improvement is also achieved with fewer runs. SPI data rate, sampling rate, and number of DFT points can be optimized for shorter optimization time.

During test we noise-average the ADC output to ensure our linearity measurements were unimpeded by the deliberately under-specified comparator noise. We are careful to keep only the original 12 binary bits of precision, so the effective ADC resolution remains only 12 bits. Fig. 12 is the noise-averaged output spectrum of the ADC with its peak ENOB of 11.3 bits using the reconfiguration algorithm discussed in Section IV. Fig. 13 shows the noise-averaged optimization results for several input and sampling frequency combinations. ADC performance is flat up to 35 MS/s, and a nearly 2-bit repeatable ENOB increase from optimization is demonstrated in all conditions.

ADC power consumption (including all supplies and references except for the CMOS I/O buffers on the digital outputs) is 1.457 mW at 10 MS/s and is dominated by the column buffers in the DAC. The peak ENOB *without* noise averaging is 10.4 bits (close to the expected 10.5), resulting in a Walden FoM of 109 fJ/C-s. Due to the undersized comparator, this work is not optimized for FoM and thus a comparison table has been omitted.

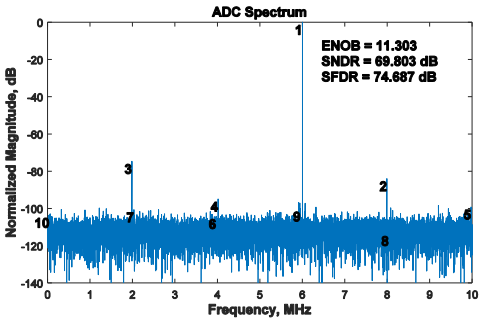

Fig. 12. Measured noise-averaged spectrum of ADC post-reconfiguration at Fs = 20MHz, Fin = 6 MHz.

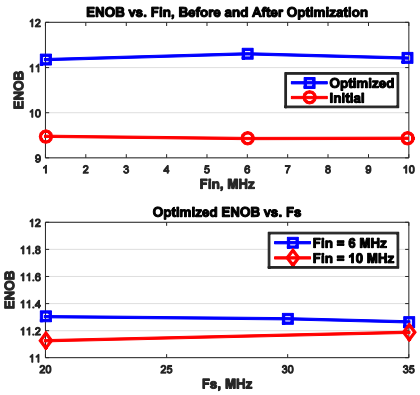

Fig. 13. Measured ENOB vs. Fin before and after optimization, and measured ENOB vs. Fs at two input frequencies.

VII. Conclusion

A novel, mismatch-immune, completely reconfigurable DAC has been realized. The goal of decoupling mismatch constraints from DAC linearity was successfully validated in a 65nm CMOS prototype. ADC performance is as intended and is consistent across both input and sampling frequency ranges. Every reconfiguration procedure resulted in improved linearity from the default fabricated configuration, regardless of test conditions.

Acknowledgments

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