A 48-MHz Differential Crystal Oscillator With 168-fs Jitter in 28-nm CMOS

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***Abstract*— A 168-fs rms jitter, 48-MHz differential crystal oscillator based on a new active inductor biasing circuit achieves differential operation with low noise, power, and area overhead. This architecture has two significant advantages compared to the single-ended crystal oscillators that are normally used: 1) this circuit rejects power supply noise and interference which leads to lower jitter and 2) the crystal oscillator-induced spurious tones are smaller and therefore less detrimental to sensitive blocks (e.g., LNA) in RF radios. This paper theoretically analyzes the differential crystal oscillator and provides detailed design considerations. A prototype requires half the power and 80% less area than previously reported differential crystal oscillators. Implemented in a 28-nm LP CMOS process, it draws 1.5 mA from a 1-V supply and occupies 0.013 mm^2.**

***Index Terms*— Crystal oscillators, frequency generation, jitter, phase noise.**

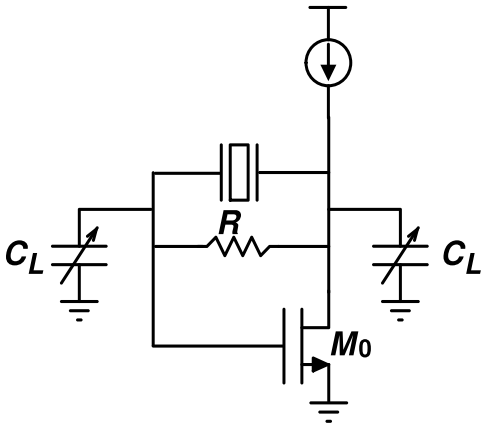

Fig. 1. Traditional Pierce crystal oscillator.

I. Introduction

CRYSTAL oscillators (XO) are essential components of wireless transceivers. A crystal oscillator provides a signal with a precise frequency (reference clock) to blocks such as frequency synthesizers and data converters [1]–[3]. Although the popular single-ended XOs provide acceptable phase noise, they suffer from spurious tones (spurs), due to unbalanced operation, and these spurs degrade both the sensitivity of RF receivers and the spectral emission of transmitters [4]. Low phase noise and accurate frequency are two of the most important requirements for the reference clock in RF systems. The XO must achieve low phase noise to meet the stringent requirements of the receiver SNR and transmitter EVM. In addition, the XO frequency must be accurate (e.g., 10 ppm for WLAN [5]) to accommodate receive and transmit synchronization.

Traditionally, a single-ended Pierce architecture is used to realize a crystal oscillator, as shown in Fig. 1 [6]. In a Pierce XO, the crystal (XTAL) is placed between the input and output of a self-biased amplifier. A properly designed Pierce XO achieves good phase noise and a precise oscillation frequency. Nevertheless, there are a number of significant drawbacks to this architecture. First, the Pierce XO is often a major generator of spurs due to the non-differential voltage swings at the crystal terminals. These XO spurs significantly degrade RF system performance because they degrade RX sensitivity and can cause TX spectral mask violations. Unfortunately, these XO spurs are costly to remove as they typically require off-chip filters. Second, the Pierce XO has poor power supply noise and interference rejection because of its single-ended operation. This power supply noise leads spurs and increased phase noise. Therefore, crystal oscillators that are fully differential are highly desirable to reduce spurs and improve the power supply rejection.

A challenge is that it is infeasible to construct a differential XO by simply placing a cross-coupled negative-g_m transistor pair across a crystal as is done with a differential *LC* oscillator—this is because such a circuit would latch. This approach forms a positive feedback and latches because a crystal resonator is high impedance at dc, unlike the case with an *LC* tank which is low impedance at dc. The differential XO in [7] solves this latching problem by ac coupling the cross-coupled transistors. However, noise and spurs can couple to the XO and degrade its phase noise because the cross-coupled pair is biased using a separate dc voltage. For ultralow jitter applications such as WLAN radios, this means that a large die area is required to filter the noise of this additional bias voltage. The differential XO architecture in [8] uses two current sources or degeneration resistors in series with two cross-coupled transistors. Even though this crystal oscillator is fully differential, this technique reduces voltage headroom which in turn degrades phase noise.

In this paper, we present a new [9], low phase noise crystal oscillator that uses an active inductor biasing circuit to achieve

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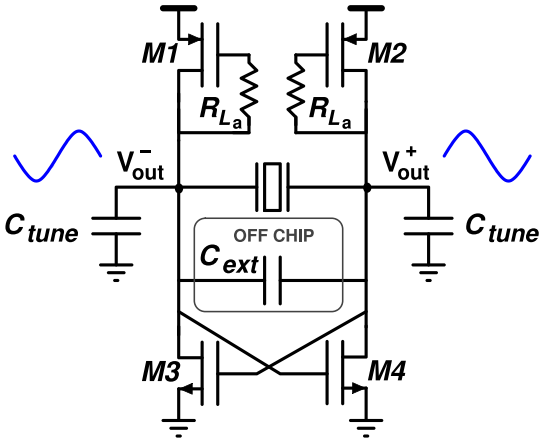

Fig. 2. Active inductor-based 48-MHz differential crystal oscillator.

a differential operation without need for an additional bias. This biasing scheme is low power, compact, and low noise. The prototype 48-MHz differential XO achieves a measured rms jitter of 168 fs with far less power consumption and area than prior art.

This paper is organized as follows. In Section II, we introduce the proposed differential XO and describe its operation. In Section III, we theoretically analyze the differential XO and outline detailed considerations for its design. This analysis is very helpful because a crystal is more complicated than a simple *LC* network and also because a fundamental understanding of our new differential XO structure is essential for effective design. This analysis leads to a set of design guidelines, and is verified against simulations and measurements. In Section IV, we present the experimental results and summary followed by the conclusions in Section V.

II. Architecture

Fig. 2 shows the new 48-MHz differential XO. Since the circuit is fully symmetric, the oscillation on nodes V_{out}^+ and V_{out}^- is differential. A low power, compact active inductor, formed by placing resistor R_{La} between the gate and drain of diode-connected transistors M1 and M2 biases the crystal. At dc, the active inductors are low impedance; therefore, the circuit does not latch since loop gain is less than one. Near the crystal oscillation frequency, the active inductor becomes high impedance to avoid loading the crystal and the cross-coupled NMOS pair (M3 and M4) that sustains the oscillation. For fine frequency tuning, C_{tune} (a programmable 6-bit binary capacitor bank with an LSB of 200 fF) is placed on both sides of the XO. C_{ext} is an off-chip capacitor for XO coarse frequency tuning. The resistor R_{La}, used in the active inductor, is a programmable 6-bit binary weighted resistor with an LSB of 0.5 kΩ.

Fig. 3 shows a small-signal model of the entire circuit. The crystal is modeled as a series *RLC* network with motion inductance L_1, motion capacitance C_1, and equivalent series resistance R_1, in parallel with shunt capacitance C_0. C_{par} represents all the parasitic capacitances seen between crystal terminals. $C_{\text{tune}}/2$ is the equivalent series combination of the on-chip fine-tuning capacitors.

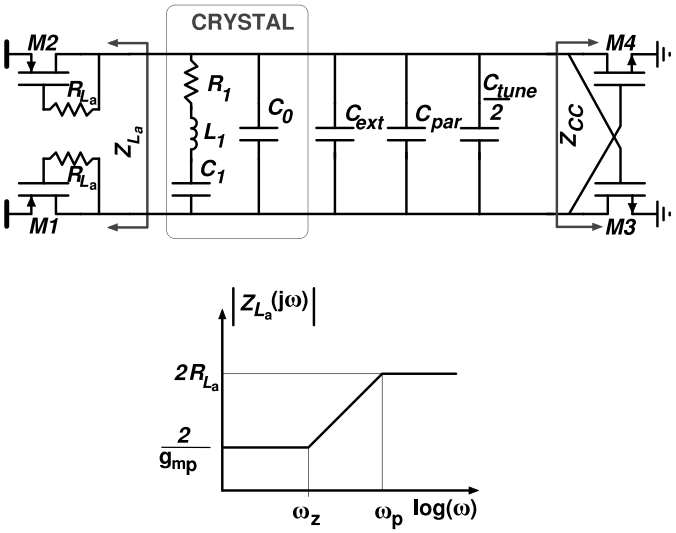

Fig. 3. Differential XO small-signal model (top) and magnitude of active inductor impedance (Z_{La}) (bottom).

The impedance of the cross-coupled pair Z_{CC} is $-2/g_{\text{mn}}$ at low frequency. The active inductor small-signal impedance Z_{La} has a zero at $\omega_z = 1/R_{\text{La}}C_{\text{gsp}}$ and a pole at $\omega_p = g_{\text{mp}}/C_{\text{gsp}}$.

As shown in the magnitude plot of Z_{La} versus frequency in Fig. 3, the low-frequency impedance of the active inductor is $2/g_{\text{mp}}$ while the high-frequency impedance rises to $2R_{\text{La}}$. M1 and M2 are sized large to achieve low impedance at dc to avoid latching (i.e., dc loop gain less than 1). The R_{La} value of the active inductor is judiciously chosen to: 1) avoid crystal loading at the desired oscillation frequency and 2) set ω_z to prevent oscillation at any frequency other than crystal's high Q, parallel-resonance frequency. This oscillation, which we term parasitic oscillation, is generally at a lower but unknown frequency. The parasitic oscillation is a relaxation oscillation with poor phase noise and should be avoided [8]. Appropriate setting of ω_z avoids a large loop gain at any frequency other than desired crystal oscillation frequency. We provide detailed analysis on how to select circuit parameters to avoid this parasitic oscillation in Section III.

III. Analysis

In this section, we analyze the new XO oscillator and provide a set of concise equations based on circuit parameters to properly design a differential XO with this new architecture. These design relationships must be satisfied to ensure proper XO startup, to avoid parasitic oscillation, and to tune the oscillation frequency. The aforementioned criteria are some of the most important design elements for this crystal oscillator. In Section III-A, we present a small-signal model for the differential XO circuit where different operating regions are identified. In Sections III-B and III-C, we analyze the XO in these different regions and use the small-signal models to derive the real and imaginary parts of the XO total admittance. The real and imaginary parts of the XO admittance are then used to derive design relationships based on circuit parameters. In Section III-D, we conclude the analysis section by providing

a design methodology based on circuit parameters that leverages the key equations derived in Sections III-A–III-C.

A. Crystal Oscillator Small-Signal Model

In this section, we present the crystal resonator small-signal model followed by the overall XO small-signal model. As shown in Fig. 3, the crystal resonator is modeled as a series *RLC* equivalent circuit (referred to as the motional arm) in parallel with the shunt capacitance C_0. The motional arm resistance, inductance, and capacitance are R_1, L_1, and C_1, respectively. The motional resistance R_1 models the loss in the crystal. The capacitor C_0 is the measured capacitance associated with the crystal, its electrodes, and the stray capacitance internal to the crystal enclosure. The equivalent circuit model is provided by the crystal manufacturer.

If we define $Z_0 = 1/j\omega C_0$, and the motional arm impedance $Z_1 = R_1 + j\omega L_1 + 1/j\omega C_1$, then the crystal impedance is obtained as

$$Z_{\text{xtal}} = \frac{Z_1 Z_0}{Z_1 + Z_0}. \tag{1}$$

At resonance, Z_{xtal} becomes resistive as $\text{Im}\{Z_{\text{xtal}}\}$ vanishes. $\text{Im}\{Z_{\text{xtal}}\} = 0$ yields two resonance frequencies designated as series ω_{rs} and parallel ω_{rp} resonance frequencies. These frequencies can be approximated by the following formulas:

$$\omega_{\text{rs}} \approx \frac{1}{\sqrt{L_1 C_1}}$$
$$\omega_{\text{rp}} \approx \frac{1}{\sqrt{L_1 C_1}} \left(1 + \frac{C_1}{2C_0}\right). \tag{2}$$

The crystal can be used in two different resonant modes. In a series resonant circuit, it appears as a pure resistor of value R_1 at a frequency ω_{rs}. In a parallel-mode oscillator, the crystal is used in the ω_{rs}–ω_{rp} frequency range called parallel-resonance region. In this region, the crystal acts as an inductor [10].

A "load capacitance" C_L, specified by the manufacturer, is added between the crystal terminals which together with C_0 resonate with L_1 at the ω_L frequency

$$\omega_L \approx \frac{1}{\sqrt{L_1 C_1}} \left(1 + \frac{C_1}{2(C_0 + C_L)}\right). \tag{3}$$

In this way, fine adjustment of oscillation frequency is achieved by fine-tuning C_L. It is important to note that C_L is different from the physical external capacitor C_{ext}, placed across the crystal (Fig. 2). Rather, C_L is C_{ext} plus the sum of all capacitances, including, the crystal buffer input capacitance and tunable capacitor C_{tune} across the crystal.

Using Fig. 3, the XO small-signal model is comprised of the parallel combination of crystal, the active inductor (Z_{La}), the cross-coupled NMOS pair (Z_{cc}), the external capacitor (C_{ext}), the parasitic capacitor (C_{par}), and the series combination of fine-tuning capacitors ($C_{\text{tune}}/2$).

In the following analysis, the NMOS and PMOS transistors are modeled by their small-signal parameters which are gate–source capacitance C_{gs} and transconductance g_m. The small-signal output resistance r_o is ignored because the transistors are always sized with a large enough r_o to avoid loading the crystal.

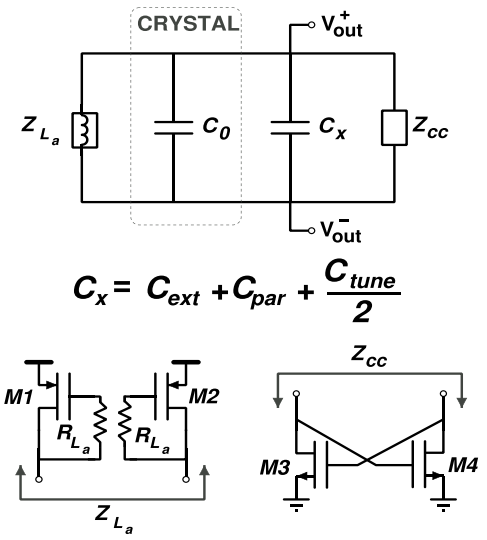

Fig. 4. Small-signal model of differential XO for frequencies $\omega < \omega_{\text{rs}}$ and $\omega > \omega_{\text{rp}}$.

The active inductor impedance (Z_{La} in Fig. 3) is

$$Z_{L_a}(\omega) = \frac{2}{g_{m_p}} \frac{1 + j\omega/\omega_z}{1 + j\omega/\omega_{T_p}} \tag{4}$$

where $\omega_z = 1/R_{\text{La}} C_{\text{gsp}}$ and $\omega_{\text{Tp}} = g_{\text{mp}}/C_{\text{gsp}}$. The pole frequency ω_{Tp} is equivalent to PMOS transit frequency. As mentioned earlier, the active inductor impedance at a low frequency is $2/g_{\text{mp}}$ and it increases with frequency to reach $2R_{\text{La}}$ beyond ω_{Tp}.

The impedance of the cross-coupled pair (Z_{cc} in Fig. 3) is given by

$$Z_{\text{cc}}(\omega) = \frac{-2}{g_{m_n}} \frac{1}{1 - j\omega/\omega_{T_n}} \tag{5}$$

where $\omega_{\text{Tn}} = g_{\text{mn}}/C_{\text{gsn}}$. The pole frequency ω_{Tn} is equivalent to NMOS transit frequency. As expected, the impedance of the cross-coupled pair is $-2/g_{\text{mn}}$ at low frequencies.

B. XO Small-Signal Analysis for $\omega < \omega_{rs}$ and $\omega > \omega_{rp}$

As mentioned in Section II, the differential XO, as shown in Fig. 2, can oscillate at an undesired frequency if the circuit parameters are incorrectly set. We refer to this as a "parasitic" oscillation. In this section, we analyze the XO at frequencies $\omega < \omega_{\text{rs}}$ and $\omega > \omega_{\text{rp}}$ and find the conditions that prevent parasitic oscillation.

We redraw the XO small-signal model in Fig. 4 for $\omega < \omega_{\text{rs}}$ and $\omega > \omega_{\text{rp}}$ where the crystal impedance can be approximated as capacitor C_0. This approximation is accurate because the impedance of the series *RLC* network consisting of R_1, C_1, and L_1 is larger than the impedance of C_0 in this region.

We define a parameter $C_x = C_{\text{ext}} + C_{\text{par}} + C_{\text{tune}}/2$ to make the calculations easier. As mentioned before, with an incorrect set of design parameters, it is possible for the active inductor in parallel with C_0 and C_x to form an *LC* tank. The combination of this *LC* tank and the negative resistance of the cross-coupled pair can result in an undesired parasitic oscillation.

A sufficient condition to avoid parasitic oscillation is to choose the design parameters such that $\text{Im}\{Y_t\} \neq 0$ for

$\omega < \omega_{\rm rs}$ and $\omega > \omega_{\rm rp}$, where Y_t is the total admittance seen between XO terminals and is calculated as the parallel combination of $Z_{\rm xtal}$, $Z_{\rm cc}$, $Z_{\rm La}$, and C_x. Nevertheless, even if $\mathrm{Im}\{Y_t\}$ is equal to zero at a certain frequency, parasitic oscillation is still avoided if we ensure that $\mathrm{Re}\{Y_t\} > 0$ for that frequency (i.e., avoid parasitic oscillation by depriving the circuit of the necessary loop gain[1]).

Using the small-signal model in Fig. 4, $\mathrm{Im}\{Y_t\}$ is obtained as

$$\mathrm{Im}\{Y_t\}(\omega)|_{\omega<\omega_{\rm rs},\omega>\omega_{\rm rp}} = \frac{\omega}{2\omega_{T_n}\omega_{T_p}(\omega^2+\omega_z^2)} \times\big[\omega^2(g_{m_n}\omega_{T_p}+2\omega_{T_p}\omega_{T_n}(C_x+C_0)) +g_{m_p}\omega_{T_n}\omega_z^2+g_{m_n}\omega_{T_p}\omega_z^2-g_{m_p}\omega_{T_p} \times\omega_{T_n}\omega_z+2\omega_{T_p}\omega_{T_n}\omega_z^2(C_x+C_0)\big] \quad (6)$$

and $\mathrm{Re}\{Y_t\}$ is obtained as

$$\mathrm{Re}\{Y_t\}(\omega)|_{\omega<\omega_{\rm rs},\omega>\omega_{\rm rp}} = \frac{1}{2\omega_{T_p}(\omega^2+\omega_z^2)}\big[(g_{m_p}\omega_z-g_{m_n}\omega_{T_p})\omega^2 +(g_{m_p}-g_{m_n})\omega_{T_p}\omega_z^2\big]. \quad (7)$$

It is important to note that the denominators in $\mathrm{Im}\{Y_t\}$ (6) and $\mathrm{Re}\{Y_t\}$ (7) are always positive. Therefore, they are neglected in this analysis as we are only concerned with the sign of $\mathrm{Im}\{Y_t\}$ and $\mathrm{Re}\{Y_t\}$ for this stability analysis.

If we let $\mathrm{Im}\{Y_t\}$ in (6) equal to zero, the equation can have up to three solutions for ω. $\omega = 0$ (dc) is always a solution to $\mathrm{Im}\{Y_t\} = 0$. Therefore, $\mathrm{Re}\{Y_t\}$ must be made positive at $\omega = 0$ (i.e., resistive to avoid loop gain) to prevent latching. Using (7) and simplifying

$$@\omega = 0, \text{for } \mathrm{Re}\{Y_t\} > 0, \quad g_{m_p} > g_{m_n}. \quad (8)$$

This makes intuitive sense as the positive conductance of the active inductor should dominate over the negative conductance of the cross-coupled pair to result in a low loop gain at dc and prevent latching. Solving for the other two solutions of ω in $\mathrm{Im}\{Y_t\} = 0$ we find

$$\omega^2 = \frac{-\omega_z/\omega_{T_p}}{g_{m_n}+2\omega_{T_n}(C_x+C_0)}[g_{m_p}\omega_{T_n}\omega_z - g_{m_p}\omega_{T_p}\omega_{T_n} +g_{m_n}\omega_{T_p}\omega_z+2\omega_{T_p}\omega_{T_n}\omega_z(C_x+C_0)]. \quad (9)$$

If we select design parameters such that the right-hand side of (9) is negative i.e., $\omega^2 < 0$ then there is no real frequency which can satisfy (9). Therefore, it is ensured that $\mathrm{Im}\{Y_t\}$ is always non-zero which in turn prevents a parasitic oscillation. For right-hand side of (9) to be negative it is sufficient that the expression in the brackets is positive. This yields the following inequality:

$$g_{m_p}\omega_{T_n}\omega_z - g_{m_p}\omega_{T_p}\omega_{T_n} + g_{m_n}\omega_{T_p}\omega_z + 2\omega_{T_p}\omega_{T_n}\omega_z(C_x+C_0) > 0. \quad (10)$$

Rearranging, we obtain

$$g_{m_p}\omega_{T_n}\omega_z + 2\omega_{T_p}\omega_{T_n}\omega_z(C_x+C_0) > g_{m_p}\omega_{T_p}\omega_{T_n} - g_{m_n}\omega_{T_p}\omega_z. \quad (11)$$

[1]This in essence is the small signal analysis for Barkhausen stability criterion.

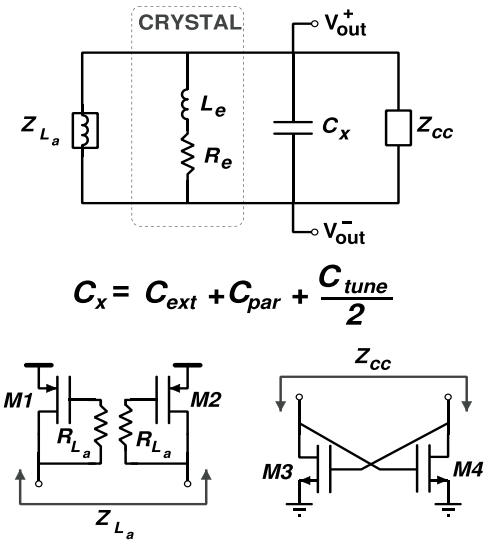

Fig. 5. Small-signal model of differential XO for the parallel-resonance region ($\omega_{\rm rs} < \omega < \omega_{\rm rp}$).

For $Z_{\rm La}$ to be inductive, $R_{\rm La}$ should be larger than $1/g_{\rm mp}$ [see Fig. 3 (bottom)]; therefore, we have $g_{\rm mp}R_{\rm La} \gg 1$. Considering this relationship, substituting $\omega_z = 1/R_{\rm La}C_{\rm gsp}$, $\omega_{\rm Tp}=g_{\rm mp}/C_{\rm gsp}$, and $\omega_{\rm Tn}=g_{\rm mn}/C_{\rm gsn}$, and factoring, we obtain

$$R_{L_a} < \frac{1}{g_{m_p}}\left(1+\frac{2(C_x+C_0)}{C_{gs_p}}\right). \quad (12)$$

Equation (12) sets an upper bound for the value of $R_{\rm La}$ as a sufficient condition to avoid parasitic oscillation in the differential XO. We must choose the active inductor PMOS transistor size ($g_{\rm mp}$ and $C_{\rm gsp}$) and the active inductor resistance $R_{\rm La}$ accordingly to avoid parasitic oscillation.

C. XO Small-Signal Analysis for $\omega_{rs} < \omega < \omega_{rp}$

The equivalent small-signal model for parallel-resonance region ($\omega_{\rm rs} < \omega < \omega_{\rm rp}$) is shown in Fig. 5. This is the region where the XO should oscillate. First, we obtain the real part of the crystal oscillator total admittance Y_t given by

$$\mathrm{Re}\{Y_t\}(\omega)|_{\omega_{\rm rs}<\omega<\omega_{\rm rp}} = \mathrm{Re}\{Y_{\rm xtal}\}|_{\omega_{\rm rs}<\omega<\omega_{\rm rp}} + \mathrm{Re}\{Y_{\rm cc}+Y_{L_a}\}. \quad (13)$$

In the parallel-resonance region, we need to ensure that $\mathrm{Re}\{Y_t\} \ll 0$ for oscillation startup. We now derive the conditions needed to fulfil this requirement. As mentioned in Section III-A, in the parallel-resonance region, the crystal can be modeled as an inductor L_e in series with a resistor R_e. Therefore, $Y_{\rm xtal}$ in the parallel-resonance region is given by

$$Y_{\rm xtal}(\omega)|_{\omega_{\rm rs}<\omega<\omega_{\rm rp}} = \frac{1}{R_e+j\omega L_e}. \quad (14)$$

To obtain $\mathrm{Re}\{Y_{\rm xtal}\}$, a series-to-parallel transformation is needed to calculate the crystal equivalent parallel

resistance R_p. The equivalent parallel resistance R_p can be approximated by [11]

$$R_p = Q^2 R_e = \frac{\omega^2 L_e^2}{R_e} \tag{15}$$

where $Q = \omega L_e / R_e$. Using the fact that $L_e = 1/(\omega^2 C_L)$ at parallel resonance including C_L

$$R_p = \frac{1}{\omega^2 R_e C_L^2}. \tag{16}$$

As shown in [10], R_e in this region is related to R_1 by

$$R_e = R_1 \left(1 + \frac{C_0}{C_L}\right)^2. \tag{17}$$

We therefore obtain

$$R_p = \frac{1}{\omega^2 R_1 (C_0 + C_L)^2}. \tag{18}$$

Therefore, the first term in (13) $\mathrm{Re}\{Y_{\mathrm{xtal}}\}$ (which is equal to $1/R_p$) is obtained as

$$\mathrm{Re}\{Y_{\mathrm{xtal}}\}(\omega)|_{\omega_{\mathrm{rs}} < \omega < \omega_{\mathrm{rp}}} = \omega^2 R_1 (C_0 + C_L)^2. \tag{19}$$

Substituting $Y_{\mathrm{La}} = 1/Z_{\mathrm{La}}$ from (4), $Y_{\mathrm{cc}} = 1/Z_{\mathrm{cc}}$ from (5), and simplifying we obtain the second remaining term in (13), that is

$$\mathrm{Re}\{Y_{\mathrm{cc}} + Y_{L_a}\}(\omega) \approx \frac{-g_{m_n}}{2} + \frac{g_{m_p}}{2} \frac{1}{\frac{\omega^2}{\omega_z^2} + 1}. \tag{20}$$

Equation (20) is accurate at frequencies where $\omega \ll \omega_{\mathrm{Tp}}$.

In the parallel-resonance region, we need to ensure that $\mathrm{Re}\{Y_t\} \ll 0$ for oscillation startup. At resonance (where $\omega = \omega_L$), we obtain

$$\mathrm{Re}\{Y_{\mathrm{cc}} + Y_{L_a}\}|_{\omega=\omega_L} \approx \frac{-g_{m_n}}{2} + \frac{g_{m_p}}{2} \frac{1}{\frac{\omega_L^2}{\omega_z^2} + 1}. \tag{21}$$

We have to choose the design parameters such that $\omega_L > \omega_z$. This is to avoid weakening of the negative transconductance of the cross-coupled pair by the active inductor as is clear from (21). Essentially, $\omega_L > \omega_z$ means that the active inductor impedance is relatively large at resonance.

We get a conservative upper bound on $\mathrm{Re}\{Y_{\mathrm{cc}} + Y_{\mathrm{La}}\}$ using $\omega_L > \omega_z$ and $g_{\mathrm{mp}} \sim g_{\mathrm{mn}}$

$$\mathrm{Re}\{Y_{\mathrm{cc}} + Y_{L_a}\}|_{\omega=\omega_L} < \frac{-g_{m_n}}{4}. \tag{22}$$

Using (13), (19), and (22), we obtain a startup condition ($\mathrm{Re}\{Y_t\} \ll 0$) at resonance which is

$$\frac{-g_{m_n}}{4} + \omega_L^2 R_1 (C_0 + C_L)^2 \ll 0 \tag{23}$$

where we have substituted $\mathrm{Re}\{Y_{\mathrm{cc}} + Y_{\mathrm{La}}\}$ with its upper bound value considering the direction of the inequalities.

This in turn simplifies to

$$g_{m_n} \cdot \frac{1}{4\omega_L^2 R_1 (C_0 + C_L)^2} \gg 1. \tag{24}$$

Now that the real part of the total admittance is obtained, we look at the imaginary part of Y_t. Our goal is to lay out the conditions that are required for the crystal to see C_L, the manufacturer recommended load capacitance, and oscillate at the desired frequency. Using Fig. 5

$$\mathrm{Im}\{Y_t\}|_{\omega_{\mathrm{rs}} < \omega < \omega_{\mathrm{rp}}} = \mathrm{Im}\{Y_{\mathrm{xtal}}\}|_{\omega_{r_s} < \omega < \omega_{r_p}} + \mathrm{Im}\{Y_{\mathrm{cc}} + Y_{L_a} + Y_{C_x}\}. \tag{25}$$

The imaginary part of crystal admittance is simply given by

$$\mathrm{Im}\{Y_{\mathrm{xtal}}\}|_{\omega_{\mathrm{rs}} < \omega < \omega_{\mathrm{rp}}} = \frac{1}{\omega L_e}. \tag{26}$$

The equivalent parallel capacitance (C_L) resonates with L_e at ω_L to yield the desired oscillation frequency in the parallel-resonance region; therefore, we only have to make sure that $\mathrm{Im}\{Y_{\mathrm{cc}} + Y_{\mathrm{La}} + Y_{\mathrm{Cx}}\} = \omega_L C_L$.

Similar to the approach for $\mathrm{Re}\{Y_t\}$, we obtain the imaginary part of the cross-coupled pair and active inductor admittances. Using the small-signal model of Fig. 5, we obtain

$$\mathrm{Im}\{Y_{\mathrm{cc}} + Y_{L_a} + Y_{C_x}\}(\omega) = \frac{g_{m_n}\omega}{2\omega_{T_n}} + \frac{g_{m_p}\omega}{2\omega_{T_p}\left(1 + \frac{\omega^2}{\omega_z^2}\right)} - \frac{g_{m_p}\omega}{2\omega_z\left(1 + \frac{\omega^2}{\omega_z^2}\right)} + \omega C_x. \tag{27}$$

Evaluating (27) at $\omega = \omega_L$ and equating with $\omega_L C_L$, we get

$$\frac{g_{m_p}}{2} \frac{\frac{1}{\omega_{T_p}} - \frac{1}{\omega_z}}{1 + \frac{\omega_L^2}{\omega_z^2}} + \frac{g_{m_n}}{2\omega_{T_n}} + C_x = C_L. \tag{28}$$

Substituting $\omega_z = 1/R_{\mathrm{La}} C_{\mathrm{gsp}}$, $\omega_{Tp} = g_{\mathrm{mp}}/C_{\mathrm{gsp}}$, and $\omega_{Tn} = g_{\mathrm{mn}}/C_{\mathrm{gsn}}$, we arrive at

$$\frac{C_{gs_p}}{2} \frac{1 - g_{m_p} R_{L_a}}{1 + \omega_L^2 R_{L_a}^2 C_{gs_p}^2} + \frac{C_{gs_n}}{2} + C_x = C_L. \tag{29}$$

TABLE I
KEY DESIGN EQUATIONS

Equation Number in Text	Equation	Description
8	$g_{m_p} > g_{m_n}$	Avoid latching at DC
12	$R_{L_a} < \frac{1}{g_{m_p}}(1 + \frac{2(C_x + C_0)}{C_{gs_p}})$	Avoid parasitic oscillation
18	$R_p = \frac{1}{\omega^2 R_1 (C_0 + C_L)^2}$	Crystal equivalent parallel resistance
24	$g_{m_n} \cdot \frac{1}{4\omega_L^2 R_1 (C_0 + C_L)^2} \gg 1$	Ensure startup
29	$\frac{C_{gs_p}}{2} \frac{1 - g_{m_p} R_{L_a}}{1 + \omega_L^2 R_{L_a}^2 C_{gs_p}^2} + \frac{C_{gs_n}}{2} + C_x = C_L$	Oscillate at target frequency

D. Design Methodology and Guidelines

In this section, we present guidelines for designing a differential XO circuit based on the architecture presented in this paper. The key equations derived in Sections III-A–III-C are summarized in Table I. Based on the criteria and these key equations, the design guidelines are as follows.

1) Calculate the crystal R_p from (18).
2) Pick NMOS and PMOS device lengths L such that their output resistance r_o is a few times larger than R_p to avoid loading the crystal resonator.

TABLE II
DESIGN EXAMPLE PARAMETERS

Design Parameters	Value	Crystal Parameters	Value
g_{mn}	4.3 mS	R_1	20 Ω
C_{gsn}	0.99 pF	C_1	3.15 fF
g_{mp}	4.9 mS	L_1	3.5 mH
C_{gsp}	2.66 pF	C_0	1.5 pF
R_{La}	2 kΩ	C_L	8 pF
C_x	10.5 pF		

3) Calculate the minimum g_{mn} from (24) using crystal parameters. Pick an actual g_{mn} which is an approximately two to three times bigger for faster startup.
4) Select g_{mp} to be bigger than g_{mn} to satisfy (8).
5) The device width W and total gate capacitance C_{gs} are calculated once L and g_m are known.

Start iteration:

6) Pick a starting value for C_x. C_L is a good starting point.
7) Choose the largest R_{La} that satisfies (12).
8) Calculate left-hand side of (29).
   a) If the result is smaller than C_L, increase C_x and go back to step 5.
   b) If the result is larger than C_L, decrease C_x and go back to step 5.
   c) If the result is close to C_L, design process is complete.

E. Simulation Results

Using the proposed methodology in Section III-D, we designed and fabricated a 48-MHz prototype of the new differential XO circuit in a 28-nm CMOS process. Table II lists the sample 48-MHz crystal specifications. Table II also includes the design parameters that follow from our theoretical analysis and design guidelines. Fig. 6 shows the simulated real and imaginary parts of Y_t (the total admittance seen between XO terminals) versus frequency. With our design parameters, $\mathrm{Im}\{Y_t\}$ never crosses zero except at the desired oscillation frequency. This means that a parasitic oscillation is safely avoided. Fig. 7 shows real and imaginary parts of Y_t in the vicinity of 48 MHz. Oscillation occurs at the frequency at which $\mathrm{Im}\{Y_t\}$ crosses zero and $\mathrm{Re}\{Y_t\} < 0$ (marked on Fig. 7). At this frequency, simulated $\mathrm{Re}\{Y_t\}$ is -1.2 mS which results in sufficient loop gain for oscillation. Fig. 8 shows the simulated differential waveforms at the crystal terminals. Fig. 9 shows the simulated phase noise profile of the differential XO (single-ended probing) which matches well with measurement results (Section IV).

To highlight the significance of our theoretical analysis, if for example, we increase the value of R_{La} to 2.5 kΩ (instead of 2 kΩ used in the design here) and violate the key design equation given in (12); there will be a potential parasitic oscillation at 11.2 MHz, as shown in Fig. 10. Fig. 11 shows

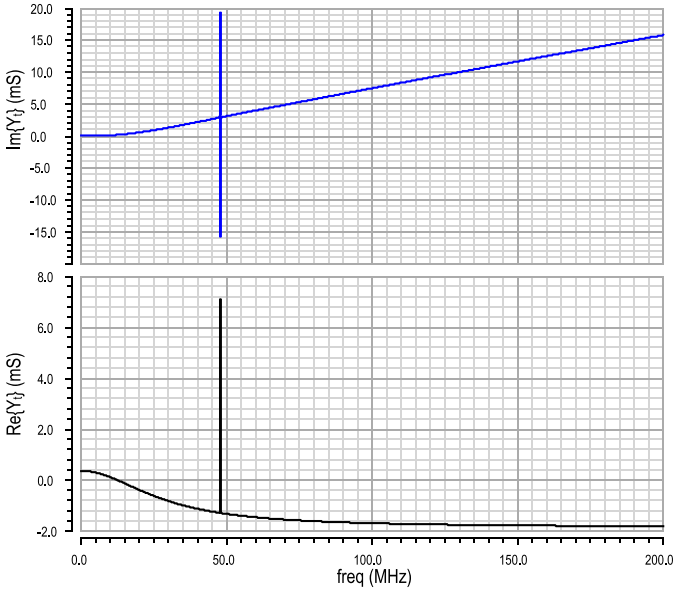

Fig. 6. Simulated real and imaginary parts of Y_t. (The total admittance seen between XO terminals.)

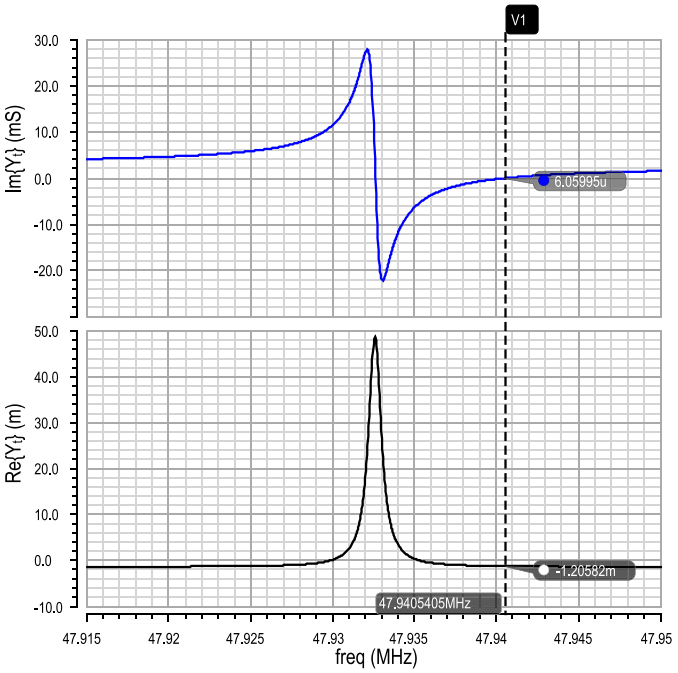

Fig. 7. Simulated real and imaginary parts of Y_t in the vicinity of 48 MHz.

the simulated real and imaginary parts of Y_t over process, supply voltage and temperature (PVT) using an R_{La} of 2 kΩ. Although for two of the corners $\mathrm{Im}\{Y_t\}$ crosses zero, $\mathrm{Re}\{Y_t\}$ remains positive; therefore, a parasitic oscillation is avoided. This result shows that the XO is immune to parasitic oscillation across PVT.

In addition, we simulated an efficient single-ended XO based on the Pierce topology (Fig. 1) to compare with our proposed differential XO. The supply current of the single-ended XO is simulated to be Idd (mA) $= 1.5 + 1.4\cos(\omega_L t + \varphi) + 0.7\cos(2\omega_L t + \theta)$. It is important to note that this current includes large undesired harmonics that will couple to

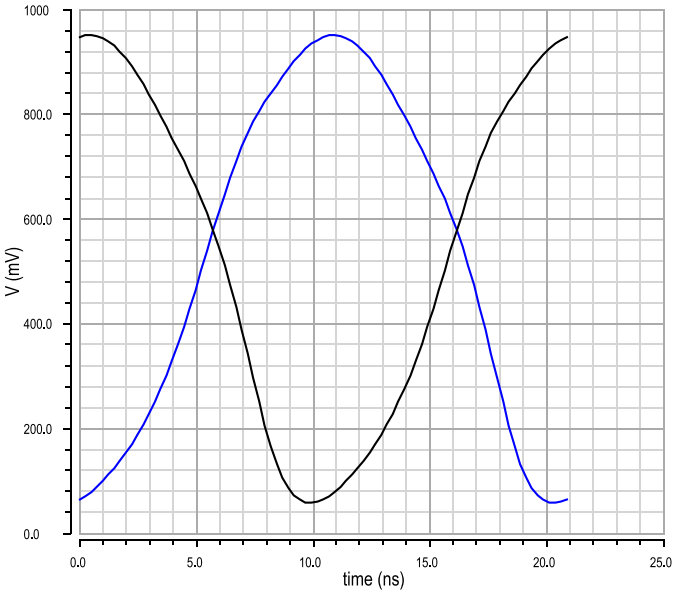

Fig. 8. Simulated 48-MHz differential XO waveform.

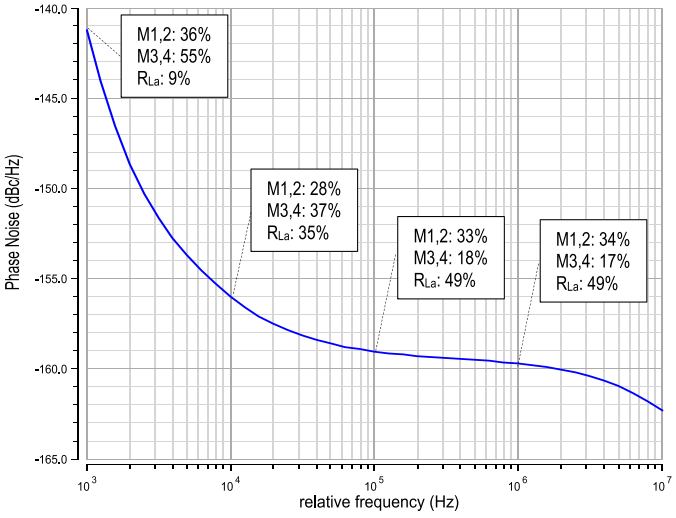

Fig. 9. Simulated phase noise of the 48-MHz differential XO (with single-ended probing) and noise contributors at 1 kHz, 10 kHz, 100 kHz, and 1 MHz offset frequencies.

sensitive blocks. The differential XO draws Idd (mA) $= 1.5 + 0.5\cos(2\omega_L t + \psi)$. In comparison to a single-ended XO, this current is free of large first harmonic. Instead, the strongest harmonic is at twice the oscillation frequency. Therefore, the differential crystal oscillator-induced spurious tones are smaller and farther apart and hence less detrimental to performance of sensitive blocks.

Another important criterion is XO power supply rejection. Supply disturbances couple to XO output which degrade the phase noise. We simulated power supply rejection of the differential XO and compared it with the single-ended Pierce XO. Table III lists power supply rejection ratios (PSRRs) at different offset frequencies for Pierce oscillator and differential XO. With single-ended probing, both circuits show similar PSRR. Nevertheless, with differential probing, as expected, the differential XO has far superior PSRR.

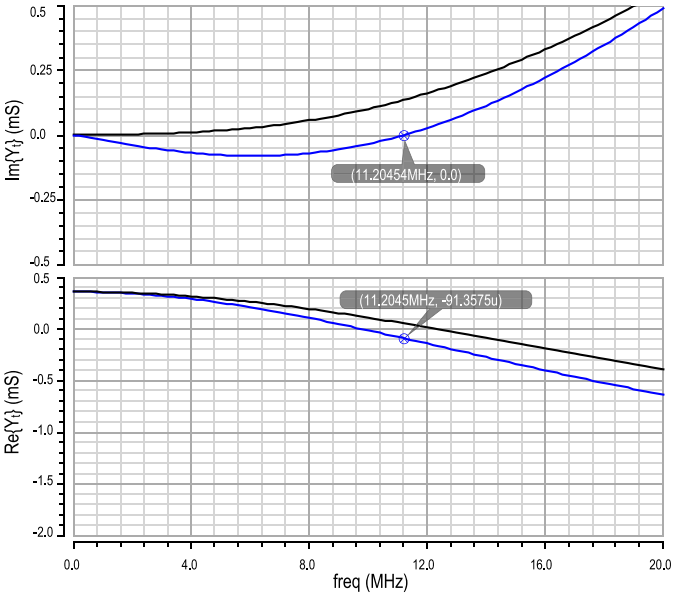

Fig. 10. Simulated real and imaginary parts of Y_t for $R_{\mathrm{La}} = 2$ kΩ (black) and $R_{\mathrm{La}} = 2.5$ kΩ (blue). Potential parasitic oscillation at 11.2 MHz with $R_{\mathrm{La}} = 2.5$ kΩ.

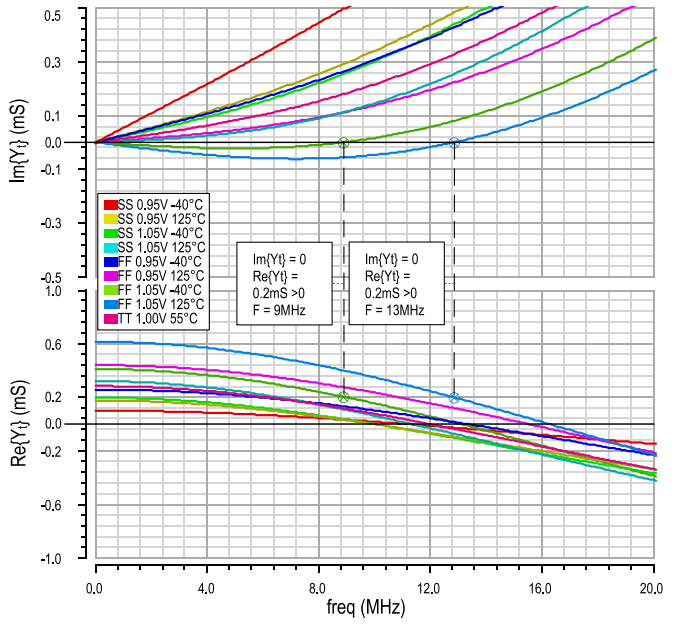

Fig. 11. Simulated real and imaginary parts of Y_t for $R_{\mathrm{La}} = 2$ kΩ over PVT.

With temperature from −40 °C to 125 °C, the XO oscillation frequency varies ±3 ppm (excludes intrinsic temperature variation of the crystal). Over the same range, phase noise performance is maintained (variation is less than 1 dB) across offset frequencies from 1 kHz to 10 MHz.

IV. Measurement Results

The circuit was fabricated in a 28-nm CMOS and occupies an active area of 0.013 mm^2 which includes the bias circuitry and the output buffers. A die photograph is shown in Fig. 12.

The measured phase noise of the 48-MHz differential XO signal using an Agilent 5052B signal analyzer is shown

TABLE III
SIMULATED PSRR (IN dB) AND COMPARISON

Offset Frequency	Pierce XO		Differential XO	
	Single-ended probing	Differential probing	Single-ended probing	Differential probing
1kHz	5.2	0.6	6.8	80
10kHz	6.1	4.8	6.8	88
100kHz	7.5	7.9	6.8	79
1MHz	7.7	8.4	7.4	79
10MHz	8.3	9.0	12.7	97

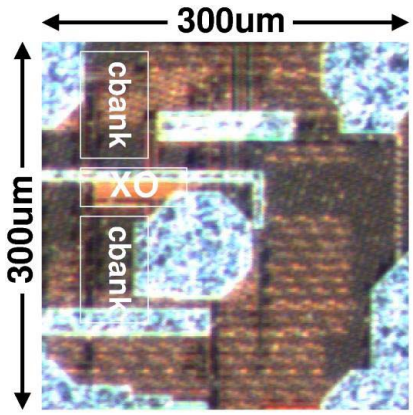

Fig. 12. Die photograph including 50-Ω output buffers, ESD circuitry, and bypass capacitors. The XO total active area is 0.013 mm^2.

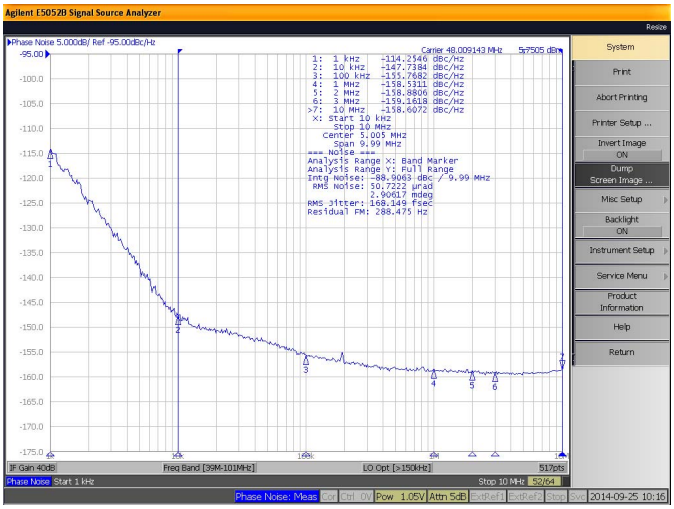

Fig. 13. Measured phase noise of the active inductor-based 48-MHz differential XO using the 5052B signal source analyzer.

in Fig. 13. The rms jitter, measured over an integration bandwidth from 10 kHz to 10 MHz, is only 168.1 fs. The measured phase noise is −147.7, −155.8, and −158.5 dBc/Hz at 10 kHz, 100 kHz, and 1 MHz offsets, respectively. At frequency offsets above 100 kHz, these numbers agree with simulation results as shown in Fig. 9. The difference between measurement and simulation results at lower frequency offsets

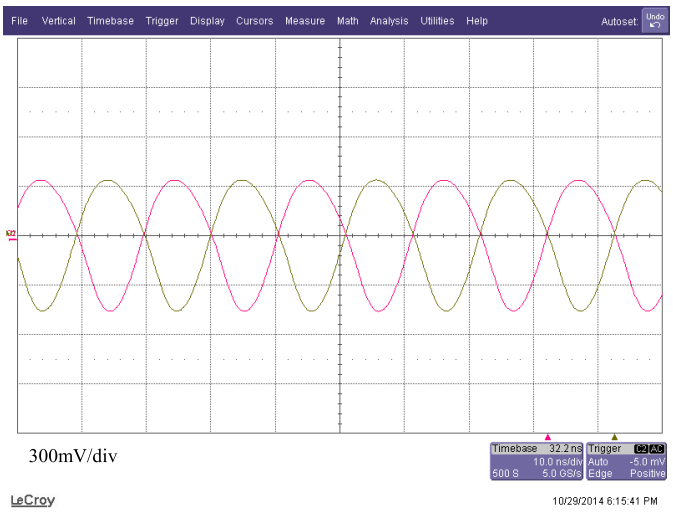

Fig. 14. Measured 48-MHz differential XO waveform probed at XO I/O pins.

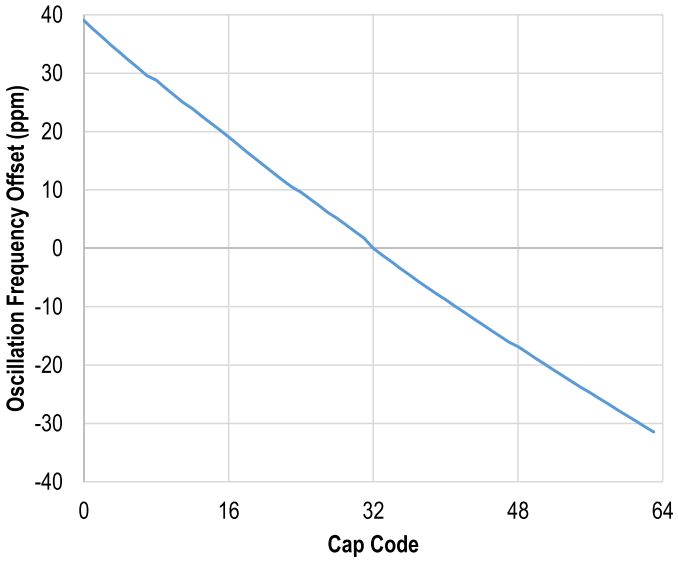

Fig. 15. Measured XO frequency tuning range.

is most likely attributed to supply noise. It is expected that the low-frequency offset phase noise will improve with an on-chip voltage regulator which is typically used in practice. The regulator filters the low-frequency noise content of the supply which can up-convert to the oscillation frequency and show up on the phase noise profile of the oscillator. In other words, the regulator shields the XO, to some extent, from outside noise and interference. However, such regulator is not effective in filtering the large current harmonics caused by the XO coupling to other sensitive blocks (e.g., LNAs). The current spikes are at much higher frequencies than the regulator bandwidth (e.g., harmonics of 48 MHz in our design) and, as a result, will appear on the main supply and ground connections and couple to other circuits.

Fig. 14 shows an oscilloscope plot which captures the differential waveforms at the crystal terminals. Fig. 15 shows the frequency tuning of the XO versus the 6-bit capacitor code. Fig. 16 shows the phase noise for different R_{La} values. As R_{La}

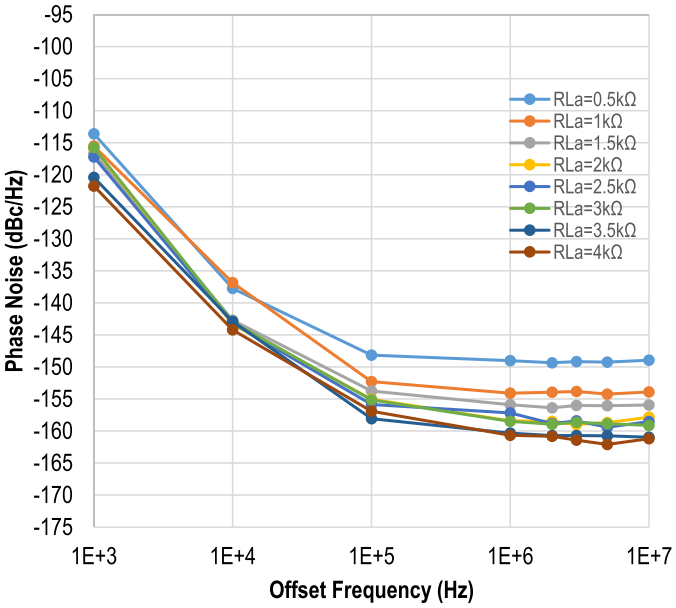

Fig. 16. Measured phase noise for different R_{La} values.

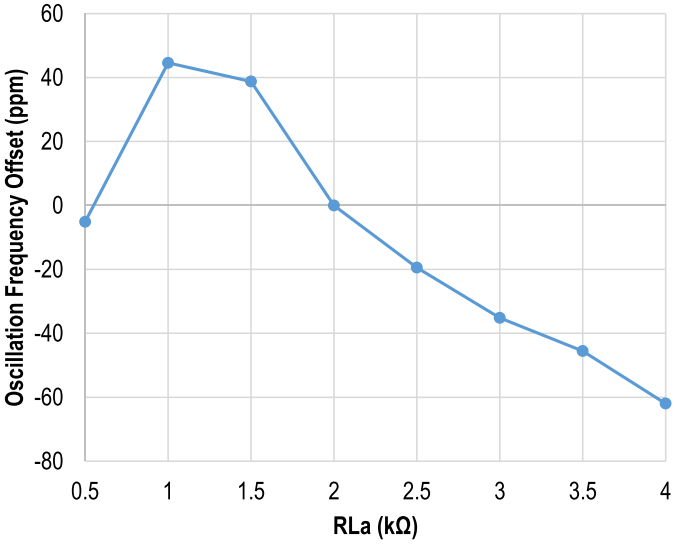

Fig. 17. Measured oscillation frequency variation for different R_{La} values.

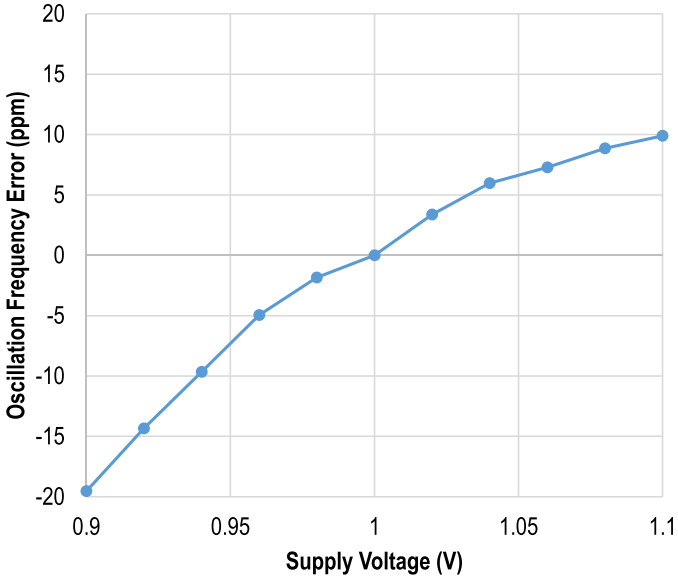

Fig. 18. Measured oscillation frequency variation with supply voltage.

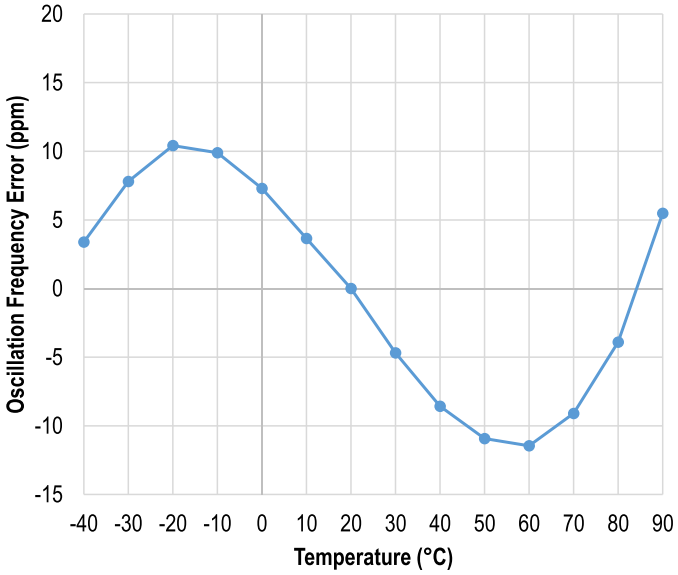

Fig. 19. Measured oscillation frequency variation across temperature.

is increased, phase noise of the XO improves. In order to avoid parasitic oscillation at startup, we should select R_{La} value to be below the limit set by (12) (here 2 kΩ). At R_{La} values above this limit, there exist two potential oscillation modes: desired at the Crystal frequency and parasitic at a lower frequency. The two modes will compete and one will dominate depending on conditions such as initial values, thermal noise profile, and relative loop gain of the two modes.

Fig. 17 shows oscillation frequency measurements for different R_{La} values. Oscillation frequency is stable within ±50 ppm with 8× variation in R_{La} value. During production, an XO is normally calibrated at room temperature using automated test equipment and the right capacitor code is chosen to cancel out the frequency error. In the proposed differential XO architecture, the same procedure can be done using both capacitor (C_{tune}) and resistor (R_{La}) codes to zero out the frequency error. As a result, the effect of process is calibrated. Moreover, since R_{La} is realized using poly resistors which have small temperature coefficients (e.g., <1% over −40 °C–120 °C range), such calibration holds over temperature.

Fig. 18 shows oscillation frequency measurements across various supply voltage levels. Supply pushing can be minimized by using a voltage regulator. The proposed XO topology is voltage biased; therefore, a stable supply voltage would also result in a stable bias point for the differential XO. Fig. 19 shows measured oscillation frequency variation over temperature. The XO frequency variation over the −40 °C–90 °C temperature range is approximately ±10 ppm.

Table IV summarizes the performance of the differential XO and compares with recent work.

TABLE IV
DIFFERENTIAL XO MEASUREMENT SUMMARY AND COMPARISON

Parameter	This Work	JSSC'12 [7]	RFIC'10 [12]	ISSCC'05 [13]	ISSCC'16 [14]
Differential	**Yes**	Yes	No	No	No
CMOS technology	**28nm**	65nm	65nm	90nm	65nm
Power (mW)	**1.5**	2.16	7	3	0.019
Supply voltage (V)	**1**	1.8	1.4	1.4	3.3
Active area (mm^2)	**0.0133**[1]	0.15	0.09	0.18	0.09
Crystal freq. (MHz)	**48**	26	38.4	26	39.25
Phase noise (dBc/Hz) 10kHz offset[2]	**-147.7**[3]	-143.8	-144	-147	-151.0[3]
Phase noise (dBc/Hz) 100kHz offset[2]	**-155.8**[3]	-148.1	-148	-150	-151.4[3]
Phase noise (dBc/Hz) 1MHz offset[2]	**-158.5**[3]	-148.7	-148	-150	-151.5[3]
RMS jitter (fs) 10kHz-10MHz BW	**168**[3]	420	587	660	380[3]
FOM[4] **(dB) 10kHz offset**	**250**	244	239	246	272
FOM[4] **(dB) 100kHz offset**	**258**	248	243	249	272
FOM[4] **(dB) 1MHz offset**	**260**	249	243	249	272
Tuning range (ppm)	**±35**	±104	280	70	
Average tuning step (ppm)	**1**	0.005	0.002	0.004	

[1] Would increase by ~15% if C_{ext} were to be realized on-chip.

[2] All phase noise numbers referenced to 48MHz for fair comparison.

[3] Reported phase noise and jitter numbers are without the use of an LDO.

[4] FOM = (Oscillation Frequency)^2 / (Power × Phase noise × (Offset frequency)^2).

V. CONCLUSION

We have presented a new low power, low jitter, compact 48-MHz differential crystal oscillator which uses an active inductor biasing scheme. This differential XO has several advantages compared to single-ended counterparts and prior art. This paper provides a detailed theoretical analysis which is crucial to the design of a differential XO using this topology. Based on the analysis, we provide detailed design guidelines for the new XO architecture. The new architecture and design guidelines are verified with simulations and measurements. This new topology is an ideal low jitter reference for a low phase noise phase-locked loop and requires considerably less power and area compared to previous methods.

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