A Calibration-free 2.3 mW 73.2 dB SNDR 15b 100 MS/s Four-Stage Fully Differential Ring Amplifier Based SAR-Assisted Pipeline ADC

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Abstract

A four-stage fully differential ring amplifier in 40 nm CMOS improves gain to over 90 dB without compromising speed. It is applied in a 15b, 100 MS/s calibration-free SAR-assisted pipeline ADC. In addition, a new auto-zero noise filtering method reduces noise without consuming additional power. The ADC achieves 73.2 dB SNDR (11.9b) and 90.4 dB SFDR with a 1.1 V supply. It consumes 2.3 mW resulting in a SNDR based Schreier FoM of 176.6 dB.

Introduction

Ring amplifiers [1,2] are a compelling energy-efficient alternative to OTAs in switched-capacitor (SC) circuits, and offer several benefits over OTAs including slew-based charging, near rail-to-rail output swing, and high gain from three stages. However, because of the low intrinsic gain in advanced CMOS [3], it is hard to get enough gain for high resolution applications, even with three stages. Although increasing the length of inverters or cascoding can increase ring amplifier gain, a drawback is that the increased output resistance reduces the speed of the ring amplifier, resulting in limited performance. We present the first four-stage fully differential ring amplifier, breaking the tradeoff between gain and speed. We also introduce auto-zero noise filtering to reduce noise without consuming extra power. We verify the new ring amplifier with a 15b 100 MS/s calibration-free SAR-assisted pipeline ADC.

Four-Stage Fully Differential Ring Amplifier

Unlike the case with three-stage ring amplifiers, making a dominate pole at the output of the final stage [1, 2] does not properly stabilize a four-stage ring amplifier. This is because in feedback, the common mode of a four-stage ring amplifier can latch. Latching is the result of the main signal feedback to the 1st-stage forming positive feedback for common mode. This is especially problematic during auto-zero as the feedback factor is high. In theory, a CMFB circuit could prevent common mode latching, however such a CMFB circuit would consume almost as much power as the ring amplifier itself. To solve this problem, we introduce an auto-zero method with passive only CMFB that reliably keeps the common mode at the desired common-mode metastable point.

Our four-stage ring amplifier (Fig. 1) avoids this common mode latching by auto-zeroing at the 2nd-stage. The four-stage ring amplifier consists of a 1st-stage differential pair, two 2nd-stage differential pairs in parallel, two 3rd-stage inverters with dynamic biasing resistors, R_B, and two last-stages inverters. We divide the 2nd-stage into two paths, one is the main signal amplifier, and the other is an auxiliary amplifier for auto-zero. The differential pairs reuse current in PMOS and NMOS input devices. This reuse maximizes transconductance for a given bias current and reduces thermal noise. NMOS triode-device CMFBs set the common mode of the differential pairs, which works as coarse CMFB for the entire ring amplifier. A separate SC CMFB controls the tail current biases in the 2nd- stage to set the ring amplifier output common mode to V_{CM} during the residue amplification period. Enable switches controlled by Φ_{EN} turn off the ring amplifier when it is not used to save power. The simulated small-signal gain of the ring amplifier is higher than 90 dB over an output swing from 0.1 V to 1.0 V with a 1.1 V supply.

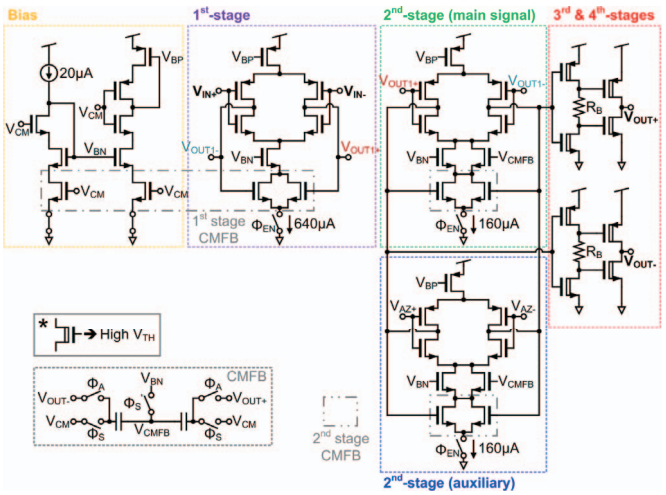

Fig. 1: Four-stage fully differential ring amplifier and biasing.

The key to preventing common-mode latching during auto-zero is a new auto-zero technique that uses the 2nd-stage auxiliary amplifier, as shown in Fig. 2. This modified auto-zero avoids common-mode latching because it operates through negative feedback. In the auto-zero phase (i.e. Φ_S is high), the input of the 1st-stage is connected to the common mode bias, V_{CM}. Next, the three-stage feedback through the auxiliary 2nd-stage amplifier samples the output offset of the 1st-stage and the input offsets of the 2nd-stages onto the auto-zero capacitor, C_{AZ}. In order to stabilize the feedback and reduce the noise folding of the auto-zero, relatively big C_{AZ} capacitors (4 pF) are used. However, the use of big C_{AZ} capacitors does not cause a significant area penalty. We can use high density MOS capacitors, stacked with MOM capacitors to minimize area since one node of C_{AZ} is always connected to ground. After auto-zero, the common mode of a SC amplifier using the four-stage ring amplifier does not latch because amplification always starts from the desired common mode.

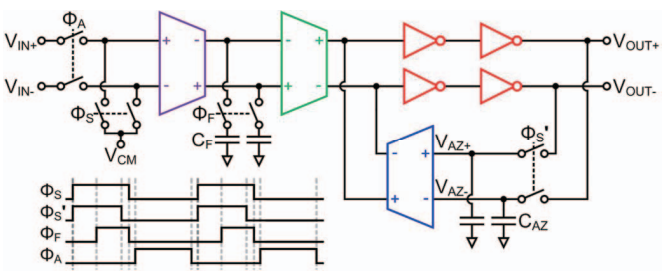

Fig. 2: Simplified four-stage ring amplifier in auto-zero configuration and timing diagram.

Auto-Zero Noise Filtering

Another benefit of this auto-zero configuration is that we further reduce auto-zero noise by filtering the 1st-stage noise,

which is the dominant noise source. We add additional 1st-stage loading capacitors, C_F in Fig. 2, to reduce the bandwidth of the 1st-stage during auto-zero, thus filtering the 1st-stage noise during the auto-zero phase. C_F is connected some delay after the beginning of the auto-zero phase (using Φ_F) to prevent slow initial settling of the 1st-stage. This insures that the output of the 1st-stage always settles to its output offset even with a low bandwidth. Transient noise simulations (Fig. 3) show that this 1st-stage noise filtering with an 8 pF C_F reduces RMS auto-zero noise by 89%. In contrast, increasing C_{AZ} by 8 pF reduces auto-zero noise folding by only 52%. This proves that the auto-zero noise filtering reduces noise more efficiently with the same additional capacitance when compared with conventional auto-zero noise folding reduction using a larger C_{AZ} [4].

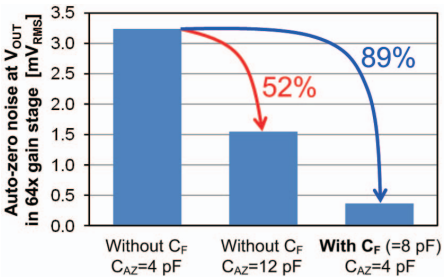

Fig. 3: Auto-zero noise filtering transient noise simulation.

ADC Implementation

The four-stage ring amplifier is used in a SAR-assisted pipeline ADC (Fig. 4) comprising of a 7b 1st-stage SAR ADC, a 64× residue gain stage, and a 9b 2nd-stage SAR ADC. With one bit of stage redundancy, the ADC resolves 15b after digital correction. The 1st-stage CDAC is divided into separate big and small CDACs [2, 5] to reduce switching energy and to improve linearity through floated-detect and skip (FDAS) switching [2]. The two CDACs sample the same input, then the small (128 fF) CDAC performs high-speed SAR conversion. The big (4 pF) CDAC, with FDAS encoding, generates a low noise residue voltage, applying the decision of the small CDAC SAR ADC. FDAS switching reduces the big CDAC mismatch by half avoiding need for calibration. The SAR CDACs are implemented with fully symmetric (including bottom plate routing) encapsulated MOM capacitors, laid out in common centroid to minimize systematic mismatch. The SAR ADCs use merged capacitor switching (MCS) [6] and asynchronously generated clocks.

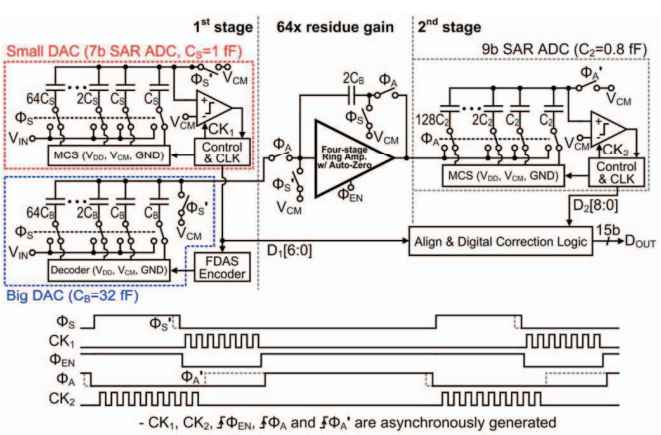

Fig. 4: Block diagram and timing of the ADC (Actual implementation is fully differential).

Measured Results

The ADC is implemented in 1P10M 40 nm CMOS and runs from a 1.1 V supply voltage. The ADC occupies 0.068 mm^2 (Fig. 5). Thanks to the wide output swing of the ring amplifier, the maximum input swing is a rail-to-rail 2.2 V_{pk-pk} even with the 64× full residue gain. Without calibration, the measured DNL and INL are -0.56/+0.67 LSB and -2.31/+2.19 LSB, respectively (Fig. 6), and the measured SNDR, SNR and SFDR are 73.2 dB (11.9b), 73.3 dB, and 90.4 dB, respectively at 100 MS/s (Fig.7). The auto-zero noise filtering improves SNDR by 1.2 dB (13% noise reduction) without extra power consumption. The measured power consumption is 2.3 mW at 100 MS/s which yields a state-of-the-art SNDR based Schreier FoM of 176.6 dB. Table I summaries the ADC performance.

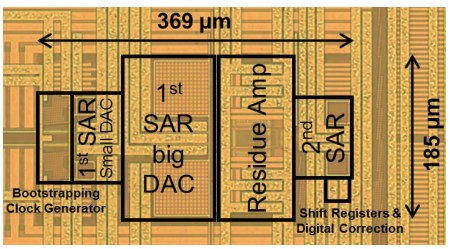

Fig. 5: Die microphotograph.

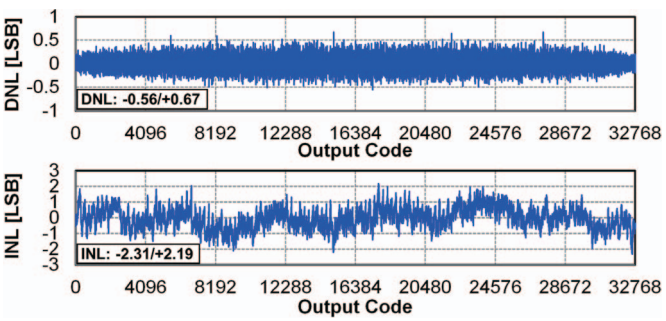

Fig. 6: Measured Linearity.

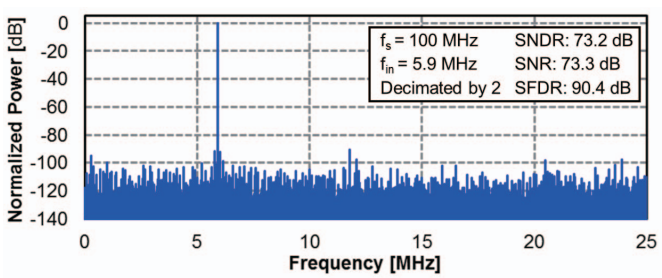

Fig. 7: Measured Spectrum (2^{20} point FFT).

TABLE I
Performance Summary

Resolution	15 bits	SNDR	73.2 dB
Supply Voltage	1.1 V	SNR	73.3 dB
Input Range	2.2 V_{pk-pk} diff.	SNDR	90.4 dB
Sampling Rate	100 MHz	ENoB	11.9 bits
Technology	40 nm CMOS	Total Power	2.3 mW
Active Area	0.068 mm^2	Schreier FoM	176.6 dB

References

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