A 5GS/s 156MHz BW 70dB DR Continuous-Time Sigma-Delta Modulator with Time-Interleaved Reference Data-Weighted Averaging

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Abstract

Conventional dynamic element matching limits the continuous time ΣΔ ADC architecture at high speeds. This work introduces a Time-Interleaved Reference Data-Weighted-Averaging (TI-RDWA) architecture that breaks the speed limitation of the traditional DEM decoder. Time-interleaving eliminates the reference voltage settling bottleneck, enabling DWA operation at 5GHz, while still achieving the benefits of first order shaping of feedback DAC mismatch. The prototype 5GS/s ADC has 70dB and 84dB measured dynamic range and SFDR, respectively, in a 156MHz bandwidth. TI-RDWA improves SFDR by 17dB. The 40nm CMOS prototype consumes 233mW.

Introduction

Emerging wireless standards, such as 5G, require wide bandwidth (>100MHz), high dynamic range (DR) (>70dB), high SFDR (>80dB) analog to digital converters (ADCs). Continuous time (CT) ΣΔ ADCs are promising for these applications because of simplified filtering and an easy to drive input. However, wide bandwidth and high DR necessitate a GHz+ sampling clock and multi-bit quantizers [1] which in turn lead to the significant challenge of DAC mismatch for linearity at high sampling speeds. Conventional dynamic element matching (DEM) methods to counter DAC mismatch, such as DWA, introduce too much delay in the feedback to be effective at high speeds. Currently, high-speed (GS/s) CTΣΔ modulators either use big DACs and burn extra power [1-2], employ calibration [3], inject dither and decrease their SNR [4], or limit their sampling speed due to reference switching delay [5]. We introduce a new DEM scheme that breaks the feedback DAC bottleneck and improves SFDR by 17dB.

We introduce a 5GS/s CTΣΔ ADC that uses a Time-Interleaved Reference Data Weighted Averaging (TI-RDWA) architecture (Fig. 1) to eliminate the DEM decoder delay in the feedback loop. We motivate this new architecture as follows: In a CTΣΔ ADC, each DAC unit element is physically connected to a corresponding comparator in the flash quantizer. Therefore, shuffling the reference voltage connections is equivalent to digitally shuffling the quantizer outputs in traditional DWA. This reference shuffling removes the digital delay of the decoder from the feedback loop, but the ADC speed is now limited by the reference voltage settling delay. In TI-RDWA, we introduce time interleaving, where we time interleave the quantizers to double the effective time for reference shuffling and overcome the reference voltage settling delay. In this way, the noise-shaping loop and the DAC mismatch-shaping loop are fully separated. Thus, the DWA decoder propagation delay does not affect the modulator loop delay, while it still first-order shapes the DAC mismatch effects for GS/s operating speeds.

The prototype 5GS/s CTΣΔ modulator has a 1.25x wider signal bandwidth than state-of-the-art ΣΔ modulators for the same power consumption [1]. It dissipates one third of the power for the same bandwidth as [2] without needing any DAC calibration [4]. The 40nm CMOS prototype achieves a 156MHz bandwidth, 66dB SNDR, 84dB SFDR, 70dB DR and a 158dB Schreier FoM while consuming 233mW. TI-RDWA improves SFDR by 17dB.

CTΣΔ TI-RDWA ADC Architecture

In TI-RDWA, we double the effective reference shuffling time by interleaving two quantization channels (i.e. CH_1 and CH_2). These channels operate at the half clock rate from complimentary clock signals (Fig. 1). While one channel quantizes the loop filter output, the other shuffles (i.e. rotates) its reference voltages based on the previous ADC output. Although TI-RDWA has two channels, only one channel consumes power at any given time, because we use fully dynamic comparators for our flash quantizers and each channel operates sequentially.

Reference DWA decoder, operating at full rate clock, applies the DWA algorithm to the feedback DACs by means of shuffling the quantizer reference voltages. It keeps track of the reference rotation and generates a new one-hot code (i.e. S[12:0]) every clock cycle depending on the previous ADC output (i.e. D_{OUT}[12:0]). This one-hot pointer (S[12:0]) alternately sets the reference connections for each of the quantizers. Therefore, as S[12:0] shuffles, the reference voltages shuffle.

Each interleaved channel (Fig. 2) latches S[12:0] using its own half-rate clock to generate an internal one-hot pointer (i.e. S_{CH1}[12:0] and S_{CH2}[12:0]). These internal pointers control the reference switch matrix in each channel. For the 13 possible rotations indicated by the one-hot code (i.e. S_{CH1} or S_{CH2}), one of 13 switches for each comparator connects the comparator reference input to the appropriate ladder tap.

The comparator sampling operation in each channel is controlled by the comparator clock (i.e. CLK_{comp}) which is an inverted version of the internal reference shuffling clock. In this way, we guarantee that the sampling happens well after the reference shuffling. Fig. 3 shows the timing diagram for reference shuffling and examples of how the reference connections for three of the 13 comparators in both channels change with time.

A third-order feed-forward loop filter architecture (Fig. 4) minimizes the amplifier output swing and the power consumption of the ADC for high speed operation. The time-interleaved multi-bit quantizer has 13 two-stage fully dynamic comparators per channel. The amplifiers are implemented with a multistage multipath feed-forward topology and the unit element of the multi-bit DACs is implemented as a fully complementary current-steering structure. The output impedance of the DAC current sources is increased with cascode transistors. 1.95V and -0.55V supply voltages are used for the current sources. Thanks to the use of TI-RDWA, the biasing current transistors are sized for only 9-bit linearity.

Measurement Results

The 40nm CMOS prototype occupies 0.45mm^2, not counting the on-chip decimator (Fig. 5(a)). The ADC consumes 233mW at 5GS/s. Fig. 5(b) shows the power consumption distribution of the prototype. While most of the power is consumed by the amplifiers (125mW), the reference DWA decoder only uses 6mW. The decimator power of 30mW is not included in the

total power consumption. For a 15MHz input, the measured SFDR (Fig. 5(c)) improves by 17dB when TI-RDWA is enabled, resulting in 66dB SNDR and 84dB SFDR. For a 100MHz input, the measured SNDR is 64dB (Fig. 6(a)). Table 1 compares the performance of the ADC with the state-of-the-art. The ADC achieves a measured dynamic range (DR) of 70dB in a 156MHz bandwidth for a 15MHz input.

Acknowledgements

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References

[1] M. Bolatkale, JSSC, 2011, pp.2857. [2] H. Shibata, JSSC, 2012, pp.2888. [3] S. Wu, ISSCC, 2016, pp.280. [4] Y. Dong, ISSCC, 2016, pp.278. [5] W. Yang, ISSCC, 2008, pp.498.

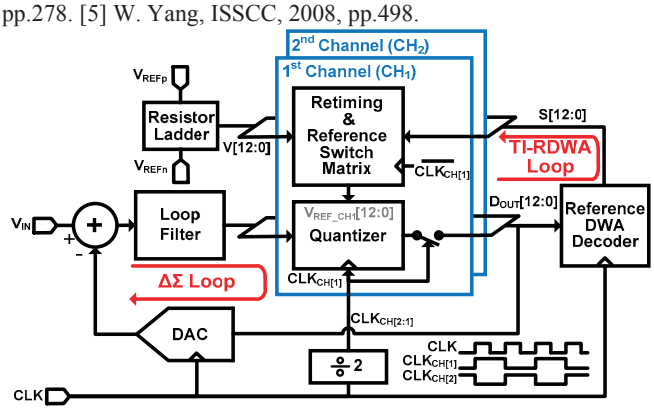

Fig. 1: Block diagram of the high speed CTΣΔ modulator with the proposed Time-Interleaved Reference DWA architecture.

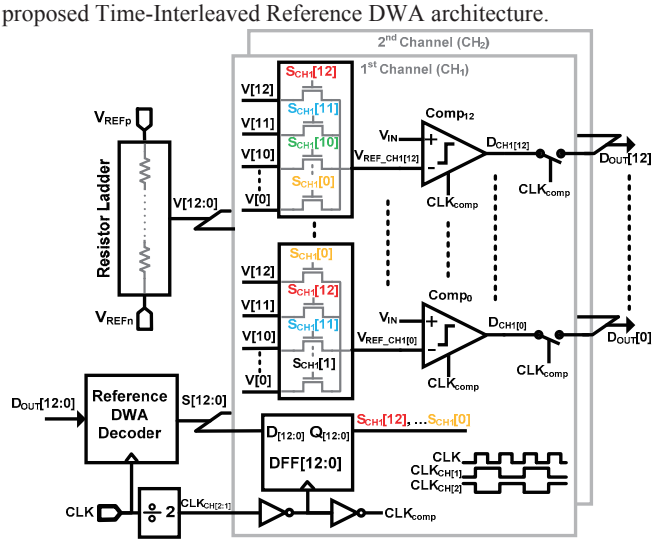

Fig. 2: Single-ended block diagram of TI-RDWA loop.

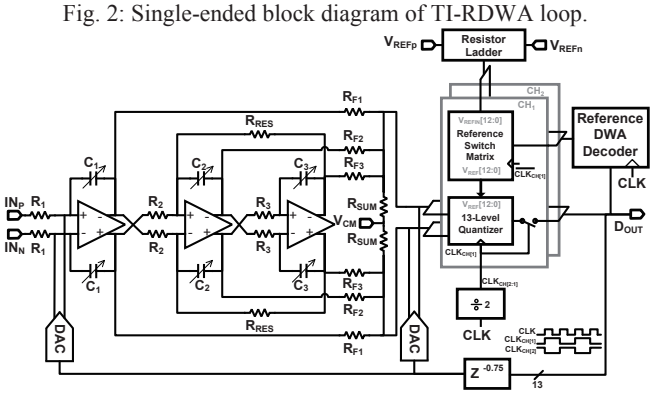

Fig. 4: Architecture of the CTΣΔ modulator with TI-RDWA.

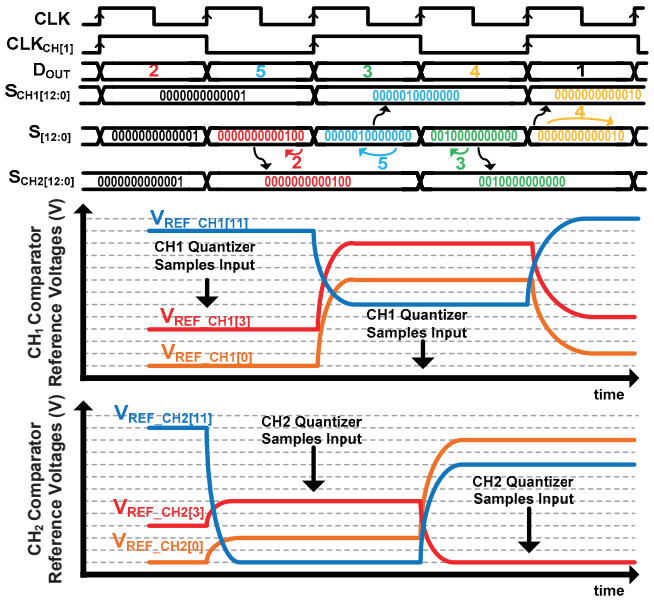

Fig. 3: Reference voltage rotation for three comparators (0,3 and 11) in channels 1 (CH_1) and channel 2 (CH_2).

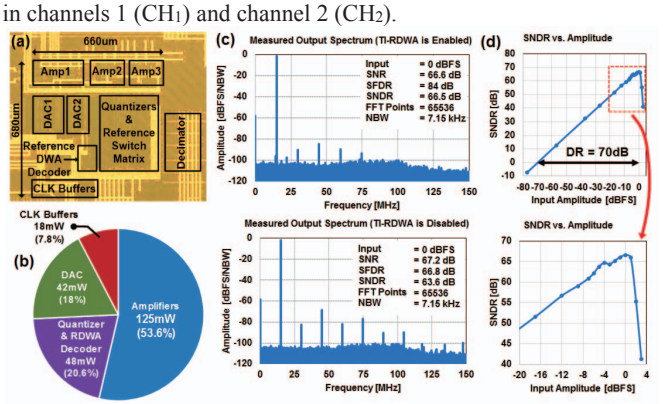

Fig. 5: (a) Die photograph, (b) Power consumption, (c) Output spectrum with 15MHz input after on-chip decimator (TI-RDWA is enabled and disabled), (d) SNDR vs. input power with a 15MHz input.

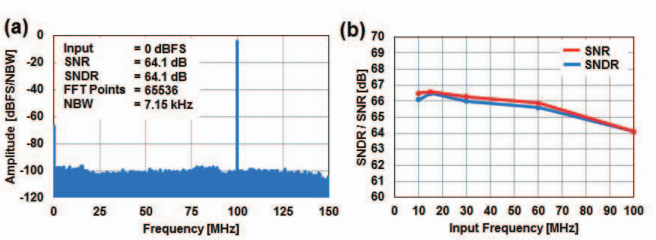

Fig. 6: (a) ADC spectrum with 100MHz input after on-chip decimator (TI-RDWA enabled) (b) SNDR and SNR plot vs input frequency

TABLE. I Performance comparison with the state-of-the-art

	This Work	JSSC 2011 [1]	JSSC 2012 [2]	ISSCC2016 [3]	ISSCC 2016 [4]
Architecture	CTΣΔ	CTΣΔ	CTΣΔ	CTΣΔ	CTΣΔ
Technology (nm)	40	45	65	16	28
Sampling Frequency (GHz)	5	4	4	2.88	8
Bandwidth (MHz)	156	125	150	160	465
Supply Voltage (V)	1.1/1.95/-0.55	1.1 / 1.8	1/±2.5	1.4/1.5/0.8	1/1.8/-1
Power (mW)	233	256	750	40	890
Area (mm^2)	0.45	0.9[b]	5.5[b]	0.155	1.4
DAC Error Control Technique	First-order Shaping	Sizing of the DACs	Sizing of the DACs	Sizing of the DACs	Calibration & Dithering
Dynamic Range (dB)	70	70	73	72.1	69.3
SNR (dB)	66.6	65.5	71	68.13	68
SFDR (dB)	83.3	78.2	78[c]	75	NA
SNDR (dB)	66.5	65	71	65.33	67
ENOB (bits)	10.75	10.50	11.50	10.56	10.84
FOM_S (dB)	158.3	156.9	156.0	168.1	156.5
FOM_W (fj/conversion-step)	432.4	704.7	862.2	82.8	523.1

[a] Including the decimation filter and clock buffers, [b] Including the bandpass CTΣΔ modulators
[c] For the RC low-pass modulator