A 16-Element 4-Beam 1GHz-IF 100MHz-Bandwidth Interleaved Bit-Stream Digital Beamformer in 40nm CMOS

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***Abstract*— This paper introduces a 16 element, 1GHz IF input, digital beamformer (DBF) that generates 4 independent simultaneous beams, with 100MHz bandwidth. Although DBF has several advantages over analog beamforming, including higher accuracy and multiple beam generation, application of on-chip DBF has been limited due to high power consumption and large die area. The proposed architecture addresses these issues by combining efficient Continuous-Time Band-Pass Delta Sigma Modulators (CTBPDSMs) with Interleaved Bit-Stream Processing (IL-BSP). IL-BSP saves 80% power and 80% area compared to a conventional DSP approach. The overall 16 element array has a measured 58.5dB SNDR and a 59.6dB SNR over a 100MHz bandwidth (11.2dB array gain). Thanks to the IL-BSP approach, the measured beam patterns are near ideal.**

***Index Terms*—Phased arrays, linear antenna array, beam steering, delta sigma modulation.**

I. Introduction

Large scale beamforming is essential for emerging high-capacity mm-wave wireless communication schemes such as 5G. Mm-wave systems require 10s to 100s of antennas to make up for high path loss and other link impairments [1]. A larger number of elements creates a sharper beam. Multiple simultaneous beams support multiple simultaneous links. Digital BeamForming (DBF) has several advantages over analog/RF beamforming including higher accuracy, more flexibility, efficient adaptive beam processing (such as tapering), higher noise immunity, faster beam control, simplified array calibration and multiple simultaneous beams [2]. However, the high power consumption and large die area of both the ADCs and the digital beamforming circuitry hinder DBF for large numbers of antenna elements.

In [2], a bandpass digital beamformer supports 8 input elements and generates 2 beams, however it is limited to 20MHz of bandwidth and an input frequency of 260MHz. Paving the way for multi-link large scale DBF, we introduce a digital beamformer that produces 4 beams from 16 antenna elements, which is the most for any published single-chip digital beamformer. This is enabled through a new Interleaved Bit-Stream Processing (IL-BSP) scheme and a compact and efficient ADC architecture. The prototype operates with an input IF of 1GHz and has 100MHz of bandwidth making it ideal for mm-wave and 5G communication systems.

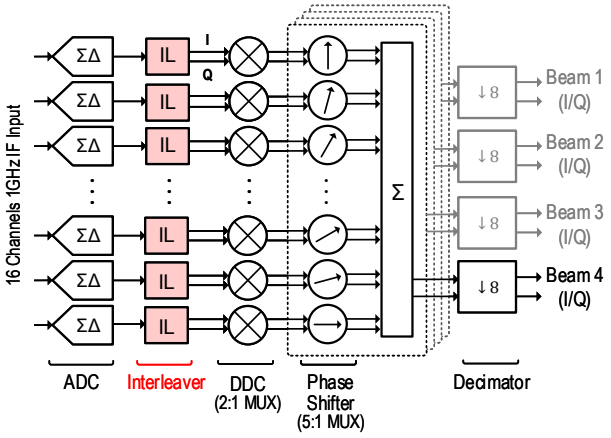

Fig. 1. Overview of the digital beamformer architecture.

II. System Architecture

As shown in Fig. 1, the 16 element 100MHz bandwidth prototype IC takes advantage of continuous-time bandpass delta-sigma modulators (CTBPDSMs) and IL-BSP to very efficiently form 4 simultaneous beams. 16 4GS/s 100MHz bandwidth CTBPDSMs digitize the 16 1GHz IF inputs. Interleavers separate the digitized bit-stream into quadrature signals. IL-BSP downconverts and phase-shifts the interleaved I/Q to form 4 beams simultaneously.

Direct digitization of the high frequency IF inputs is advantageous because it allows digital I/Q mixing to replace mismatch-prone analog I/Q mixing and halves the required number of ADCs. Continuous-time ADCs are tolerant of aliasing greatly relaxing filtering requirements. Furthermore, they present a resistive input (2kΩ in this work), simplifying the design of drivers. A quantizer resolution of 5 levels in the modulator leads to a good overall SNR and facilitates BSP. Direct BSP of the raw 5-level digital output of the modulators generates 4 independent, simultaneous beams in a fraction of the chip area compared to conventional systems.

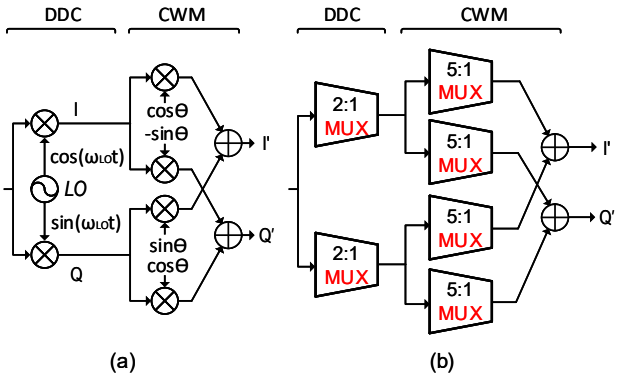

Fig. 2. (a) Operations for narrowband beamforming. (b) MUX based implementation.

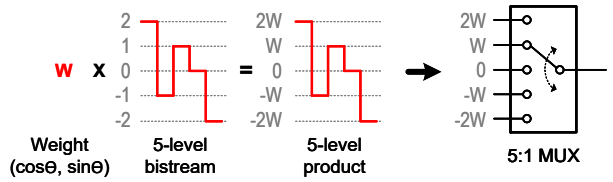

Fig. 3. BSP implementation of CWM.

III. Implementation

A. Bit-stream processing (BSP)

Our IL-BSP approach reduces die area and power consumption by 80% compared to conventional DSP. To begin with, BSP efficiently performs multiplication with multiplexers and reduces the number of decimators from the number of ADCs to the number of beams. We implement digital down-conversion (DDC) and complex weight multiplication (CWM) for phase shifting with BSP.

Fig. 2 shows digital down-conversion (DDC) and complex weight multiplication (CWM) for phase shifting with BSP [2]. For DDC, the use of a sampling frequency of four times the IF (i.e. 4GS/s) allows the sampled digital IQ mixing signals to be represented by +1, 0, -1, making down-mixing a simple MUXing operation. After down-mixing, the bitstream signal is still represented by 5-levels. 5-way MUX switching between -2W, -W, 0, W and 2W implements complex weight multiplication by W (Fig. 3). Each channel has 3-bit CWM resolution, resulting in a 0.02° beam direction resolution with 16 channels.

B. Interleaved Bit-Stream Processing(IL-BSP)

We introduce an Interleaved BSP architecture to reduce power consumption and area and to make 4GHz ADC operation practical. This is because 4GHz logic operation is challenging, especially for adders and decimators, and would necessitate extensive clock buffering and pipelining. Instead, IL-BSP takes advantage of the 0's in the sampled I/Q mixing signals to halve the digital clock rate without any loss in performance or accuracy.

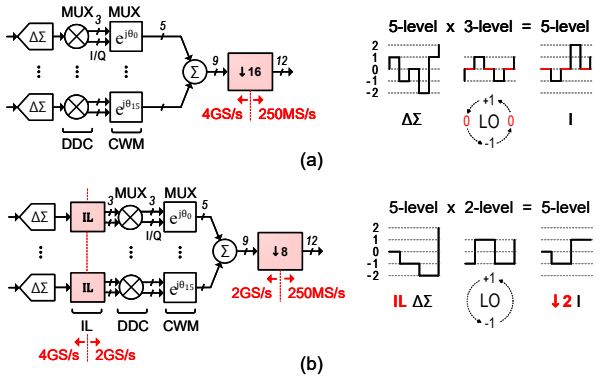

Fig. 4. Comparison between (a) BSP and (b) IL-BSP.

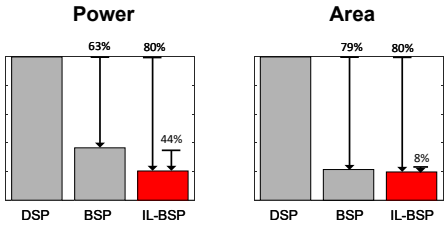

Fig. 5. Power/area comparison between DSP, BSP, and IL-BSP.

As shown in Fig. 4 (a), the sampled digital LO signals have only three values (+1, 0, -1). Since zeros do not play any role in multiplication and addition, half of the LO values can be eliminated. Therefore, as in Fig. 4 (b), an interleaver is introduced to pass two half-rate (i.e. 2GHz) data streams to the digital down mixers. The mixers and beamforming circuitry now operate at only 2GHz without losing any accuracy or performance.

Consequently, IL-BSP reduces power consumption by 44% and area by 8% compared to BSP alone. Compared to a conventional DSP implementation, both power and area are reduced by 80% (Fig. 5). The entire 16 element 4 simultaneous beam digital IL-BSP beamformer consumes only 68mW and occupies 0.0625mm^2.

C. Continuous-Time Band-Pass Delta Sigma Modulator

The ADC area and power consumption have a huge bearing on the die area and power consumption of the entire beamformer. We tackle these at the system and the circuit level. At the system level, we take advantage of the signal processing gain of the large ADC array to improve the SNR of the overall beamformer. Since noise and random mismatch errors are uncorrelated, we benefit from a near-ideal 11.2dB array SNR improvement. The fourth-order CTBPDSM in Fig. 6 (a) uses compact single op-amp RC resonators instead of bulky LC-tank resonators [3] to save power and area. The resonator center frequency is tuned with 3-bit trim capacitors (Fig. 6 (b)). To further reduce power and area, we use a passive summer instead of power hungry trans-impedance amplifier (TIA) in front of the

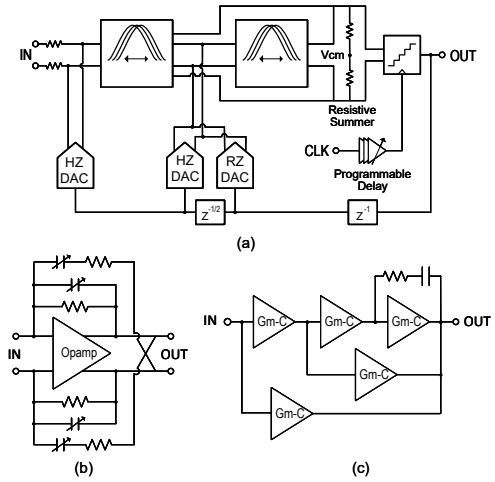

Fig. 6. Implementation of (a) 4th-order CTBPDSM (b) RC resonator and (c) 3-stage nested Gm-C op-amp.

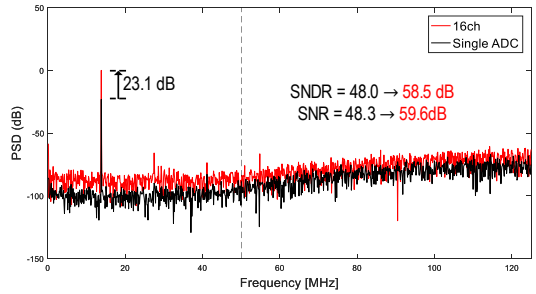

Fig. 7. Measured power spectral density of a single CTBPDSM and overall 16 element beamformer.

quantizer. Thanks to the passive summer, the ADC consumes 20% less power and occupies 10% less area. The 4GS/s 5-level quantizer is on-chip offset calibrated so it presents a very small capacitive load (0.2fF) to the summer. The quantizer sampling time is digitally adjusted by a 3b tunable delay to ensure loop stability. The op-amps use a 3-stage nested Gm-C structure which gives a good tradeoff between bandwidth and gain.

IV. Experimental Measurements

The prototype 16 element beamformer is implemented in 40nm CMOS (Fig. 12), packaged in an 88 lead QFN package and occupies a core area of 0.22mm^2 including 16 CTBPDSMs and DBF circuitry.

A. *ADC Performance and SNR Improvement*

The average measured single ADC ENOB, for 16 ADCs in a beamformer IC, is 7.7 bits over 100MHz bandwidth. The overall 16 element array achieves a measured ENOB of 9.4 bits. While the CTBPDSM achieves a comparable SNDR, it has a 5 times higher bandwidth (100MHz) and operates with a 4 times higher center frequency (1GHz)

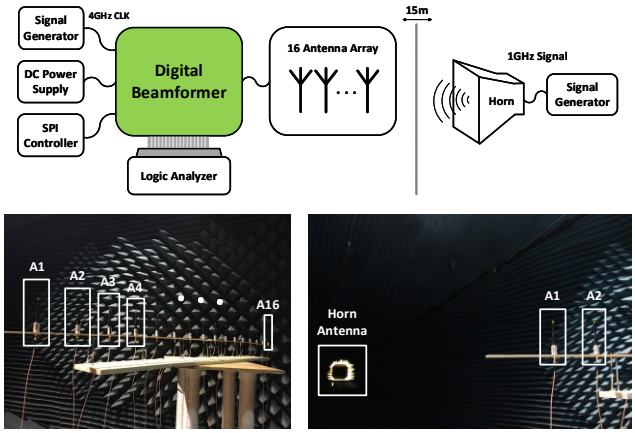

Fig. 8. Anechoic chamber testing setup. A1-16 are 1GHz antennas.

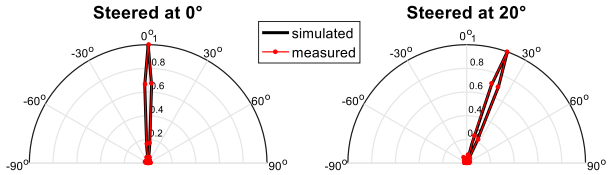

Fig. 9. Measured beam patterns in an anechoic chamber.

than the ADC in [2]. Even with this much higher performance, the ADC occupies just one third of the area (0.01mm^2) and consumes only 14% more power (15mW) than [2]. The digital beamformer benefits from a near-ideal SNR improvement of 11.2dB, which is slightly lower than theoretical value of 12dB, due to correlated errors (Fig. 7).

B. *Beam Patterns*

Beam patterns are measured in an anechoic chamber (Fig. 8) and with a benchtop setup. Benchtop measurements allow more accurate beam pattern measurement without imperfections due to long wires and echoes.

1) *Anechoic Chamber:* The prototype device is directly connected to a linear array of 16 quarter-wave whip antennas, spaced at λ/2 increments, without external LNAs (Fig. 8). A horn antenna at the end of the chamber transmits a 15dBm 1.006GHz continuous wave signal over 15m. The beam pattern is measured over incidence angles from -90° to 90° with a step size of 2.5° by rotating the antenna array. Fig. 9 shows measured beam patterns overlaid on ideal beam patterns. The measured beam pattern (red) is almost identical to the ideal one (black).

2) *Benchtop:* Similar beam patterns were measured with 16 994MHz inputs generated by direct digital synthesizers (DDS). Fig. 10 (a) shows the measured beam patterns for 4 simultaneous beams. As shown in Fig. 10 (b), the flexibility of DBF allows a beam pattern with two desired main lobes by averaging the CWM coefficients for two different single main lobes. Finally, Fig. 11 shows the variation of the beam pattern over the +/- 50MHz input bandwidth. The measured half-power beam width is 10°-15° for a +/- 60° angle range.

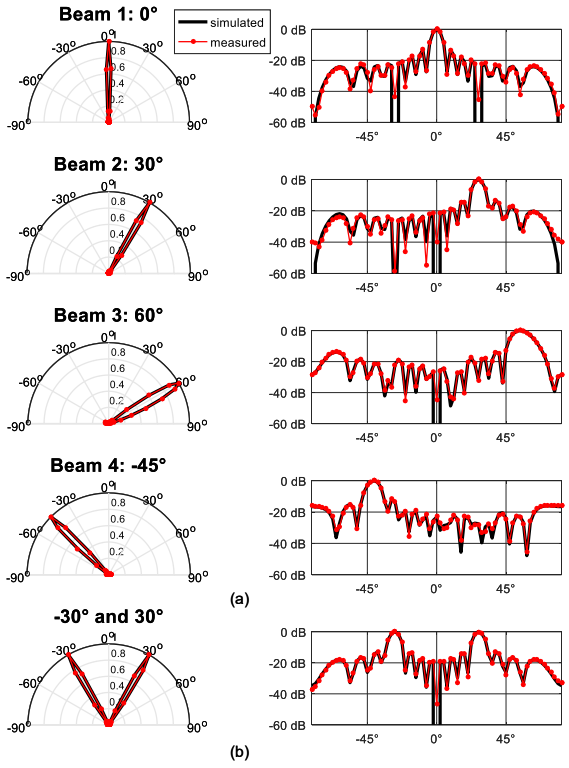

Fig. 10. (a) Measured 4 independent simultaneous beam patterns and (b) a two desired main lobes pattern with a benchtop setup.

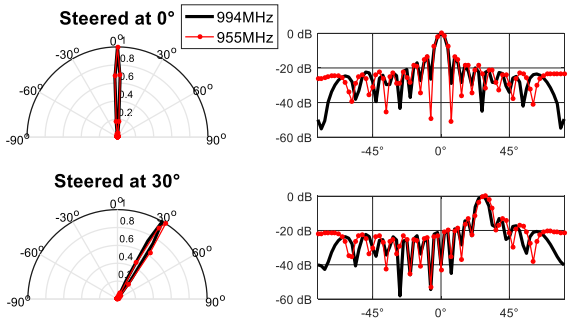

Fig. 11. Measured beam patterns over the +/-50MHz bandwidth.

C. *Comparison with state of the art*

Table I compares the prototype IC with other recent beamformer ICs. The 16 elements prototype has more elements and beams than any other published single-chip digital beamformer. The prototype consumes 312mW (16 CTBPDSMs: 244mW, DBF: 68mW). The prototype DBF has a low Power/(Beams*Elements*Bandwidth) of 0.05mW/MHz, comparable to the best analog beamformers and a record low Area/(Element*Beam) of 0.003mm^2.

ACKNOWLEDGMENTS

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TABLE I
PERFORMANCE SUMMARY AND COMPARISON

	This Work	Jeong [2]	Soer [4]	Ghaffari [5]
Domain	Digital	Digital	Analog	Analog
RF band [GHz]	1.0	0.26	1.0 – 2.5	0.6 – 4.5
# of Elements	16	8	4	4
# of Beams	4	2	1	1
Bandwidth [MHz]	100	20	30-300	3.3
Array SNDR [dB]	58.5	63.3	-	-
Array Gain [dB]	11.2	8.9[(a)]	6	4
Power [mW]	312	124	26 – 36	34 – 119
Active Area [mm^2]	0.22	0.28	0.2	0.65
Technology [nm]	40	65	65	28
Power FoM [mW/MHz] Power/(Beams *Elements*Bandwidth)	0.05[(b)]	0.39[(b)]	0.22-0.02[(c)]	3.41[(c)]
Area FoM [mm^2] Area/(Beams*Elements)	0.003	0.018	0.050	0.163

(a) SNDR improvement.
(b) ADC power included.
(c) Power estimated for 1GHz input with LNA included.

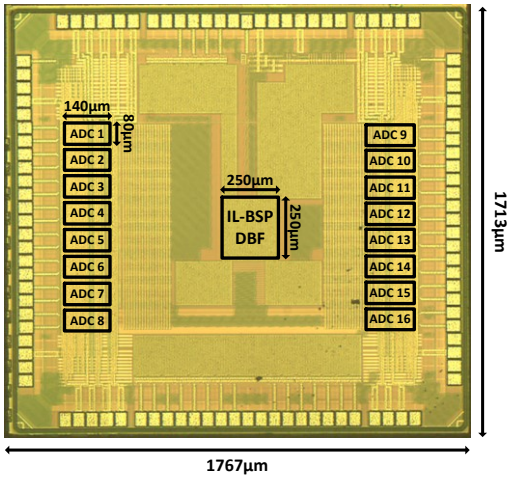

Fig. 12. Die micrograph.

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