Data Converter Reflections: 19 Papers from the Last Ten Years That Deserve a Second Look

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***Abstract*—The authors discuss several papers that have been presented over the last decade that are worth additional consideration by readers interested in data converter circuits. The papers have been selected for different reasons: some have become trend-setters, others present particularly interesting ideas that may yet set future trends.**

Keywords—data converters, interleaved converters, successive approximation converters

I. Introduction

This survey paper reflects upon influential "contemporary" data converter papers - those presented in the last 10 years. This time frame allows us the benefit of a couple of years of hindsight, but keeps us out of the "ancient history" domain. Nomination and selection is based on either impact (representing or even triggering an important trend) or interest (having the potential for future impact—perhaps something that has been overlooked to date.) The authors will make no claim that our list is definitive: these are certainly not the ONLY converter papers from the last decade worth a second read—but we will explain why we think these papers are worthy of re-examination.

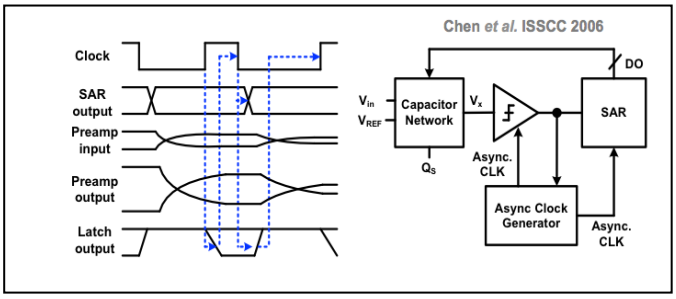
Note that in many cases, a great paper presented at a conference is invited for resubmission in greater detail in the Journal of Solid-State Circuits. In several cases, we use the journal article as our reference, though the debut was actually a conference paper. For the sake of simplicity, only the name of the first author is quoted here for multiple author papers.

II. A "Successive Approximation" Renaissance

Simplicity and elegance in design can sometimes be taken for granted, and must be periodically rediscovered. In many cases, a new set of design advantages may be exploited based on the characteristics of modern technology. The successive approximation structure (or SAR for short) has always represented a certain algorithmic optimum, but the structure provides some elegant answers to the challenges of deep micron CMOS, including its ability to be implemented without amplifiers.

For our first citation, we will violate our own criteria and point to a paper more than 10 years old, but still reasonably contemporary, and representing a leading edge of a new breed of SAR implementations. Draxelmayr's 2004 ISSCC paper [1] used a SAR structure as a building block for a high speed interleaved ADC. In contrast, previous implementations tended to interleave pipeline structures [12]. At only 6 bits of resolution, the emphasis was not on SNR, but on speed and low power, so a different set of design trade-offs were exercised. Within a few years, a number of interesting papers surfaced, exploring new dimensions in SAR design.

The Chen [2] circuit is still in the low resolution (6 bit)



high-speed performance region, but takes a very different approach to the conversion time of a SAR. Conventionally, SAR ADCs complete their n-bit conversions though equally spaced clock steps—with a clock period set by the worst-case settling/resolution time required. Chen created an asynchronous "self-timed" scheme that more efficiently allocated the nanoseconds across the decision series. Furthermore, the asynchronous operation avoided the necessity to generate and route the high speed SAR clock across the chip, offering additional power savings.

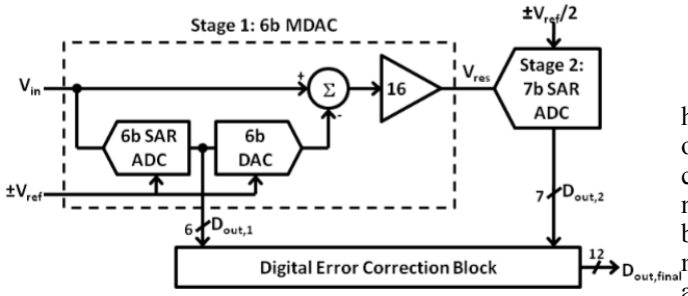
Ginsburg [3] was first to recognize that the switching power capacitor array DAC is a major component of the power consumption, and proposed a more energy efficient switching scheme. They realized that the energy consumption is much greater when the present bit decision is "0" (down transition) compared with "1" (up transition). This is because in a SAR ADC, each bit being tested is set to 1, thus the down transition requires setting the present bit back to "0', and the next bit to "1" to test the next bit. This requires 5 times greater charge (thus energy) drawn from the reference than the up transition, in which the present bit stays at "1" and only the next bit is switched to "1'. Their solution was to split each bit capacitor into two halves. This allowed the down transition to be made merely by setting one half of the present bit from "1" to "0"

without requiring any other switching. Their scheme resulted in a 37% saving in switching energy on average. This paper triggered a flurry of research in alternative switching methods, eventually rendering the capacitor array DAC switching power virtually insignificant. This work also featured careful design to really push energy efficiency: establishing the tradition of SARs running away with the converter figure-of-merit (FOM) titles. Since a SAR ADC has relatively little "active" circuitry, power optimization often involves careful analysis of the way the charge is moving on the capacitors, and how the reference and analog input are loaded.

For data converters, concepts that are workable at low resolution (6 bits or less) are not always amenable to higher resolutions where matching and SNR become important concerns. However, in this case, the deep sub-micron CMOS SAR revival has also been important in the mid resolution space that had come to be dominated by pipelined architectures. Craninckx [4] showed that an all-passive approach could be taken to higher resolutions—again with striking results on power efficiency.

At resolutions of 10 bits or more, power and performance trade-offs in SAR converters will often come down to the implementation of the comparator. Harpe [5] lowered the effective comparator noise by several dB's by allowing the comparator to retest the critical decision 5 times. Agnes used a different comparator topology that races two ramps to produce a "time domain comparator" that operates comfortably on a 1V supply [6]. Schinkel offered a different solution to the voltage headroom challenge by suggesting an entirely dynamic comparator topology (no tail current in the pre-amp) based on sense-amp structures.[7] these topologies can maintain good speed on low supply voltages across input common mode variation compared with stacked structures .

To complete the "SAR tour", we give you Kapusta [8], which took a relatively high speed SAR structure up to 14bits. One of the interesting aspects of Kapusta's implementation is the first conversion step is actually a 5 bit flash—which might lead purists to disqualify it as a "true SAR". The implementation does not require a residue amplifier, and realized a great power efficiency number for a 14 bit converter (where SNR certainly becomes a factor). The Kapusta paper is representative of a number of "hybrid SAR" approaches that have become common over the last decade: we have seen the appearance of "SAR-PIPEs", "SAR-FLASHES", and even "SAR-sigma-deltas".



12 bit SAR assisted pipeline ADC [20]

Other hybrid structures are explored by Hurrell [9] and Lee [10]. In both cases, residue amplification is employed to help realize higher resolution while maintaining speed. Merging SAR and pipeline in a SAR-assisted pipeline combines advantages of both architectures. The SAR sub-ADCs are very efficient compared to flash converters often used in pipelines. Furthermore, taking relatively high resolution (~6 bits) first stage and second stage sub-ADCs helps the pipeline. Compared to conventional pipelines, hybrid pipeline SARs only need a single inter-stage amplifier. Using a SAR for the first stage also eliminates timing mismatch between the first stage sub-ADC and MDAC sampling.

Chae combined a SAR first stage with a Delta-Sigma back end to realize a very high resolution ADC (20 bits) whose ultimate accuracy behaves like a Delta Sigma: the front end SAR converter allows the back end to quickly "zoom in" to the appropriate range.[11]. The authors have dubbed this a Zoom-ADC.

III. Interleaving For Speed

Just as SAR structures have been a key to breakthroughs in power efficiency, interleaving has been the key to pushing the frontiers of sampling rate. Of course, this technique was well established by Poulton [12] and others long before our "last 10 year" reference period. Part of what has been remarkable over the last 10 years is the pervasiveness of interleaving, and its applications across resolutions and speeds. In fact, it is worth noting that most of the papers we have already discussed ([1], [2], [3], [5]) also utilized a degree of interleaving, from simple 2-way (or ping-pong), to "lightly interleaved" (8 way or less) to highly interleaved (more than 8-way). We also see the pattern that interleaving SARs can provide an effective way of realizing a combination of speed and power efficiency that has challenged pipelined implementations in many situations.

For an indication of just what can be done with an interleaved SAR structure, we offer Kull [13], notable for pushing the interleaved SAR with mid-resolution (8 bit) up to 90 GS/s. One of the key issues for these very highly interleaved structures is how the analog input network is driven, where, when, and how the sampling is done, and how timing is aligned between the different paths. Many of the SAR techniques discussed so far are exploited in [13], including asynchronous clocking. This paper also features a dual-comparator implementation of their SAR sub-ADC: essentially another layer of interleaving within the SAR structure itself, used to boost speed.

IV. Mitigation of Dynamic Errors

Trim and calibration have been around for as long as we have been trying to implement converters with more than 8 bits of linearity. Over the last 20 years, we have been moving from correction of static errors to compensation of dynamic nonlinearities. Murmann [14] provided one of the important benchmarks here. Over the last 10 years there has been a great many papers featuring "digitally assisted analog" techniques, as well as numerous forums and sessions dedicated to this topic. With this in mind, we pick a few that offer a different twist.

Chai [15] proposed an intriguing modification to the typical pipeline architecture by splitting the amplifier into a coarse and fine path. This change extends the available settling time in each stage and may prove to be a valuable concept going forward. Essentially, this technique allows a pipeline stage to continue its settling beyond one clock cycle, much in the same way as this happens in a SAR ADC with redundancy, where the DAC also has time to settle over multiple clock cycles.

We need to have at least one DAC paper on this tour, and dynamic calibration is a good theme to highlight when looking at DACs—even for ADC fans. In many ways, DAC dynamics can be more demanding than ADC dynamics, since the ADC must be linear in the discrete time domain, whereas DACs must be linear continuously; the spectrum analyzer is always watching. (It is worth noting that the same demands apply for the feedback DAC in a continuous time sigma delta ADC.) Van de Vel [16] went beyond shuffling to do a careful re-mapping of the DAC elements to optimize both static and dynamic errors.

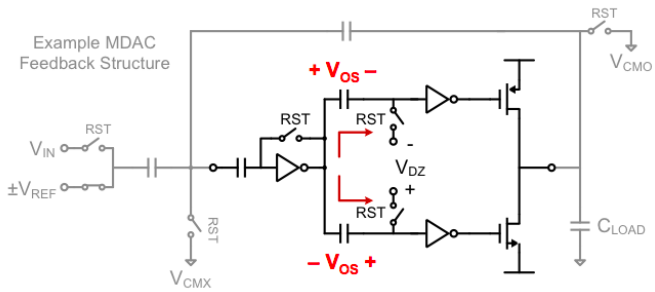
V. AMPLFICATION ON LOW SUPPLY VOLTAGE

One may chose a converter architecture that avoids amplifiers (like the SAR structures discussed previously, or the VCO based structures we will discuss next), but there are a great many very desirable converter structures—including pipelined ADCs and most sigma delta modulators-- that rely on amplifiers. Techniques that give us gain and speed in low headroom are still very attractive. However because some of the papers on this topic may not have the word "converter" in their titles, converter audiences may miss them.

Gregoire offered Correlated Level Shifting (CLS) in [17]. One can realize gain through cascading amplification stages, but that can offer stability challenges. CLS takes a different approach by estimating the final output voltage during a correlated sample phase and applying it in a second settling phase, significantly reducing the required signal swing of the amplifier. Signal charge isn't lost for the purpose of steering the op amp and is redistributed on the output capacitors as intended thereby significantly reducing radix errors in a pipelined converter. Since the amplifier is used twice (estimation and settling), the closed loop gain approaches that of a traditional stage with an amplifier with the square of the actual open loop gain. Another important advantage is that the kT/C issue in the traditional correlated double sampler (CDS) is gone, because the sampling onto that "error capacitor" happens at the output (instead of input as in CDS). But, one of the drawbacks is that unlike CDS, CLS does not cancel offset and 1/f noise. In either case, the gain is applied recursively, and we have the opportunity to optimize signal swing: a critical factor in low headroom environments.

Van de Goes [18] demonstrates the use of a dynamic integrator as a residue amplifier, where background calibration is used to realize the accuracy required in interstage gain for a pipeline ADC.

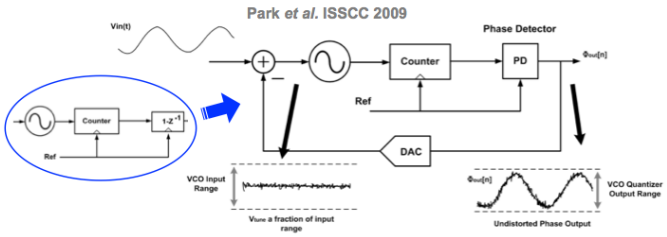
In a different approach, Hershberg [19] gave us the "ringamp". The amplifier is essentially a cascade of three inverters. However, in the middle an offset ("dead zone") is placed into the inverter such that the output stage (last inverter) is turned off for certain conditions. The control of this dead zone allows the cascade of inverters to behave like an amplifier. The ringamp can be thought of as a dynamic amplifier that self regulates/controls the behavior via the inherent feedback of the switched capacitor circuit. Lim's 2014 ISSCC paper [13] had a modified ringamp where dead zone is controlled by a resistor instead of a voltage across a capacitor, and there has been further work developing this amplifier structure. As supply voltages fall below 1V, diff pairs and tail currents become harder to squeeze in, and we are seeing more "inverter-as-an-analog-gain-block" approaches.



VI. SOMETHING DIFFERENT: VCO-BASED ADCS

The challenges of very deep submicron (low voltage compliance) and the advantages (very high speed) suggest that we consider completely different architectural approaches—including using time as part of the quantized quantity. The concept of VCO-based ADCs precedes our decade window, including work by Høvin [20], but in our time period the concept has been revived in a compelling way by Straayer [21]. The topology takes advantage of the fact that VCO-based quantizers can provide multi-bit quantization and integration without saturating—but it also deals with the nonlinear voltage-to-frequency characteristic by wrapping a conventional continuous time integrator loop around the quantizer—essentially making this a higher order modulator hybrid structure. This topology lends itself to higher SNDR applications than the previous work. This implementation also features a multi-phase VCO that is wired to the feedback DAC elements in a clever manner to provide 1st order shaping of DAC element mismatch.

As a follow up, Park [22] worked to address the remaining issue of VCO linearity by feeding back phase rather than frequency in the continuous time loop. While this approach forfeits the benefit of the inherent dynamic element matching noise shaping of the feedback DAC elements, it substantially reduces the effects of the VCO's Kv nonlinearity. (This is also a great example of where the Journal of Solid-State Circuits article represents a much more informative reference for study than the original conference paper.)



VII. Conclusion

As with any survey, these citations should be used as a starting point for the converter enthusiast. The references in each of these papers can be used to trace circuit genealogy backwards, and search for other papers by the same authors can also prove a rich vein of worthy work. The IEEE Xplore tool is recommended as an excellent resource (it also provides an indication of the number of times a given paper has been cited by other IEEE publications, and as you might guess, several of these papers have been substantially cited.)

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