27.3 Area-Efficient 1GS/s 6b SAR ADC with Charge-Injection-Cell-Based DAC

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To support growing data bandwidths, high-speed moderate-resolution ADCs have become vital for high-speed serial links. Interleaved SAR ADCs achieve high sampling speeds and good energy efficiency. However a challenge is that these ADCs are large and therefore suffer from interleaving artifacts related to size [1]. Compact, efficient SAR ADCs are needed to address this problem. As an alternative, multiple-bit-per-cycle SAR ADCs deliver high speed from a single SAR ADC, but at the cost of significant added complexity (i.e., extra quantizers and capacitor DACs) and die area [2,3]. This work addresses the need for a fast, compact SAR ADC, with a 1GS/s SAR ADC that has the best Walden FOM and the smallest area among 5-to-6.3b ADCs published in ISSCC (see Fig. 27.3.1).

We introduce a *charge-injection SAR* (or ciSAR), which is based on a charge-injection DAC structure. The ADC achieves GHz sampling speed from a single SAR ADC and reduces area by more than half by leveraging two unique features of ciSAR: (i) interrupted settling and (ii) reusability of charge-injection cells.

Thanks to interrupted settling, ciSAR is faster, simpler and more linear for high-speed applications. This is because ciSAR avoids the significant distortion suffered by conventional fast SAR ADCs due to insufficient DAC settling time. This distortion is caused by residual settling from earlier SAR conversion steps while the present DAC settling step is taking place. Figure 27.3.2 illustrates how residual settling compromises the linearity of the ADC. The residual settling from earlier steps continues into the present settling step, in this example, skewing trips points A and C upwards. Several techniques, mostly based on redundancy have previously been developed to lessen this problem, but these complicate back-end computation and require extra DAC steps. An *interrupted settling* scheme enabled by ciSAR solves the residual settling problem. With interrupted settling, DAC settling for a given SAR step stops *completely* (i.e., forced stop) at the end of that step – there is no residual settling in subsequent steps. As shown in Fig. 27.3.2, with interrupted settling, there is no longer any distortion of the trip points A, B, and C.

Interrupted settling in the ciSAR architecture is enabled by the charge-injection DAC, which consists of modular *charge-injection cells* (CICs), as shown in Fig. 27.3.3. The input signal is sampled onto two integration caps (C_{int}) on the DAC+ and DAC- nodes. During the binary search, the CICs contribute fixed quanta of charge to the integration caps. The binary search is similar to set-and-down method [4]. Thanks to their unique nature, the CICs are reused so that only 8 identical CICs are needed for a 6b ADC. The differential voltages on the integration caps are fed to a strong-arm type comparator and the comparator decision is fed back to the charge-injection DAC.

The charge-injection DAC employs a unique uni-directional transfer of charge as opposed to the bi-directional charge sharing in a conventional capacitor DAC. The CICs in the charge-injection DAC inject a fixed amount of charge to the integration caps when enabled. To achieve this, charge-transfer devices are used as unidirectional switches to isolate the charge source from the DAC outputs with high output impedance. In this way, a CIC will only ever transfer charge from its charge reservoir when enabled by the controller. The combination of high output impedance and controllability allows the CIC to transfer a fixed amount of charge to the C_{int} capacitors, independent of the sampled potential. With interrupted settling, CICs used as DAC elements eliminate residual settling to achieve better linearity even when DAC settling time is short, as shown in Fig. 27.3.2.

The CIC structure and its behavior are illustrated in Fig. 27.3.4. The differential CIC cell draws charge from the reservoir node and injects it into either the DAC+ or DAC- nodes, depending on the comparator decision, reducing its potential. The CIC cell consists of 4 NMOS transistors (M1~4) that source and transfer the charge and three logic gates (G1~3) that control these transistors. M1, M2 are charge transfer switches, M3 is a charge reservoir and M4 is a reset transistor. The CIC is normally in reset state with M4 on, pre-discharging the reservoir node to ground.

During each transfer cycle, when both Transfer and Enable are high, either M1 or M2 is turned on depending on Comp Out+ and Comp Out-. This initiates the transfer of charge out of reservoir node into DAC+ or DAC-. The charge reservoir is made up of the channel charge of the long-channel charge source transistor (M3), as well as parasitic capacitance. When the Transfer signal returns to zero, the charge-transfer process is interrupted and the CIC returns to the reset state to prepare for the next transfer cycle. The timing of the controls and the internal signals for a single transfer cycle are depicted in Fig. 27.3.4.

The charge-injection profile of the CIC is designed to facilitate interrupted settling. At the beginning of the charge-transfer cycle, the charge-transfer switch (M1 or M2) is strongly on; however, conduction weakens as the reservoir node rises and the V_{GS} of M1 (or M2) falls. The current dwindles until it reaches equilibrium with the small current supplied by M3. This gives the CIC the transfer current profile as shown in Fig. 27.3.4. Compared to a structure that has a flat current profile, one that tapers off is far less sensitive to jitter in the timing control signal. The tapered transfer current profile is further enhanced by channel charges injected by the charge source transistor (M3) and the reset transistor (M4) as they enter saturation and turn-off, respectively.

In addition to interrupted settling, another important advantage of ciSAR is that CIC cells can be reused multiple times in a SAR conversion. Since CICs are only active during a short time, they can utilize the rest of the time (i.e., waiting for a comparator decision) to get ready for another transfer. By reusing the CICs for the subsequent transfer cycles, the DAC area of ciSAR can be reduced at least by half or even more, since the charge-transfer process can be spread out over multiple transfer cycles to reach the desired level of transfers.

The prototype ciSAR performs 6b operation with only 8 CICs. To deliver 16 unit CIC transfers for the MSB decision, the 8 CICs are enabled twice (over two operation phases). This reuse method not only reduces DAC area by half but also halves the driver power for the control signals and the comparator's output stage, at the cost of slowing down the overall ADC by only 15%.

The ADC input range is $300mV_{pk\text{-}pk}$ ($600mV_{diffpk\text{-}pk}$). The common mode is set close to the V_{DD} so that the charge-transfer transistors in the CICs operate in saturation. This also allows the sampling switches to be implemented using only low-V_t PMOS transistors for further area reduction. A further advantage of ciSAR is that input signal does not modulate the power consumed by the CICs from the rails, since the CICs are always reset in the same pattern independent of the input signal. The integration caps are each 200fF. The integration capacitors are implemented as M1-M7 MOM capacitors and occupy only $66\mu m^2$. This compact layout scheme is possible since mismatch between the two capacitors only introduces a small offset.

The prototype, fabricated in 40nm CMOS, occupies $0.00058mm^2$ and consumes 1.26mW. The measured ENOB is above 5.46b across input frequencies spanning from 30 to 500MHz, sampled at 1GS/s (Fig. 27.3.5). The area is 52% of the closest competitor and the Walden FOM is measured at 28.7fJ/conv-step. Figure 27.3.6 compares the performance of the ciSAR prototype with state-of-the-art ADCs. A die micrograph is shown in Fig. 27.3.7.

References:

[1] Le Dortz, N. et al., "A 1.62GS/s Time-Interleaved SAR ADC with Digital Background Mismatch Calibration Achieving Interleaving Spurs Below 70dBFS," *ISSCC Dig. Tech. Papers*, pp. 386-387, Feb. 2014

[2] C-H. Chan et al., "A 5.5mW 6b 5GS/S 4×-interleaved 3b/cycle SAR ADC in 65nm CMOS," *ISSCC Dig. Tech. Papers*, pp. 466-467, Feb. 2015.

[3] H-K. Hong et al., "An 8.6 ENOB 900MS/s Time-Interleaved 2b/cycle SAR ADC with a 1b/cycle Reconfiguration for Resolution Enhancement," *ISSCC Dig. Tech. Papers*, pp. 470-471, Feb. 2013.

[4] C-C. Liu et al., "A 0.92mW 10-bit 50-MS/s SAR ADC in 0.13µm CMOS Process," *Symp. VLSI Circuits Dig. Tech. Papers*, pp. 236-237, June 2009.

[5] L. Kull et al., "A 3.1mW 8b 1.2GS/s Single-Channel Asynchronous SAR ADC with Alternate Comparators for Enhanced Speed in 32nm Digital SOI CMOS," *ISSCC Dig. Tech. Papers*, pp. 468-469, Feb. 2013.

[6] S. Le Tual et al., "A 20GHz-BW 6b 10GS/s 32mW Time-Interleaved SAR ADC with Master T&H in 28nm UTBB FDSOI Technology," *ISSCC Dig. Tech. Papers*, pp. 382-383, Feb. 2014.

[7] B. Murmann, "ADC Performance Survey 1997-2015," [Online]. Available: http://web.stanford.edu/~murmann/adcsurvey.html.

 978-1-4673-9467-3/16/$31.00

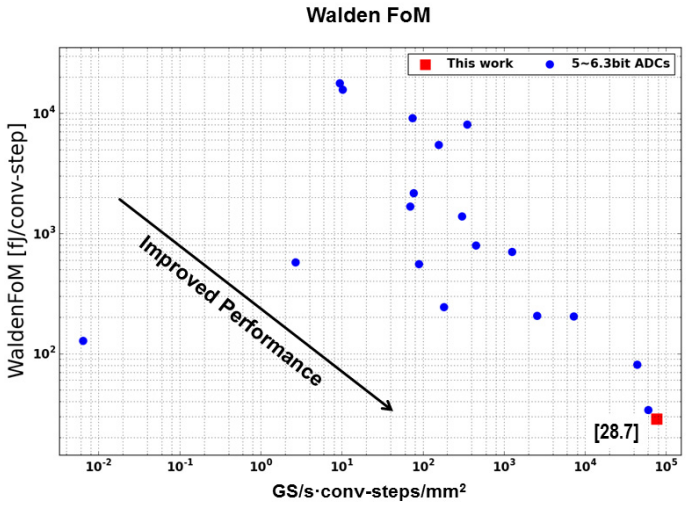

Figure 27.3.1: Survey of ADCs published in ISSCC on Walden FOM vs GS/s·conv-steps/mm².

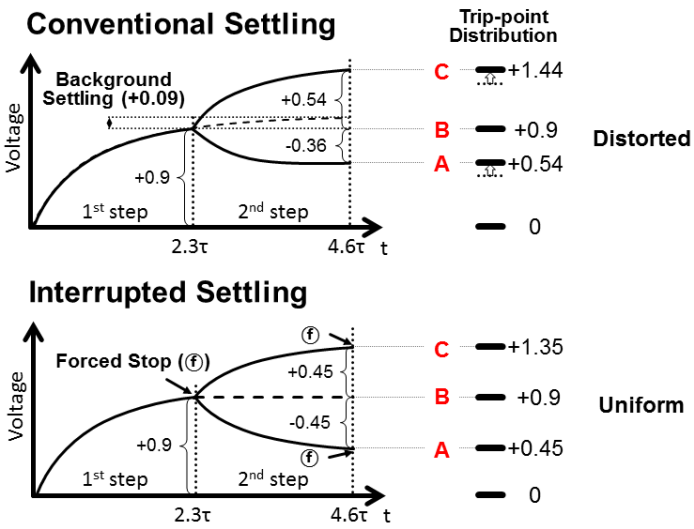

Figure 27.3.2: Comparison of conventional settling and interrupted settling methods in bandwidth-limited situation.

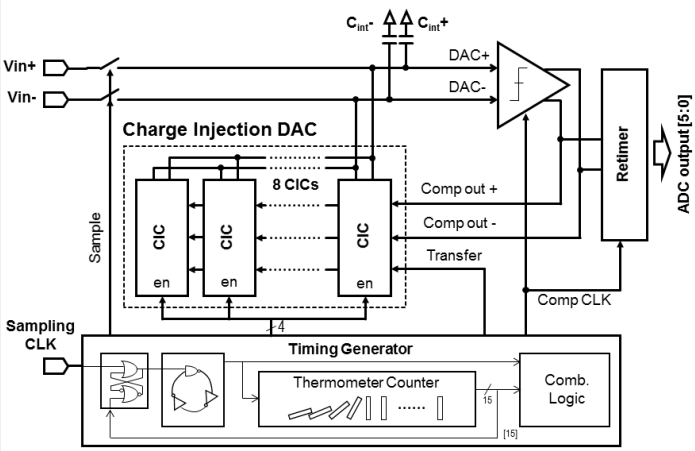

Figure 27.3.3: Overall ciSAR structure.

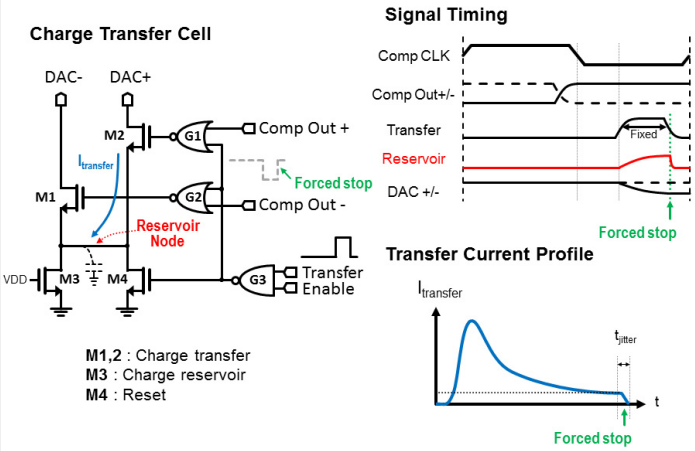

Figure 27.3.4: Charge-injection cell (CIC) with signal timing and transfer current profile.

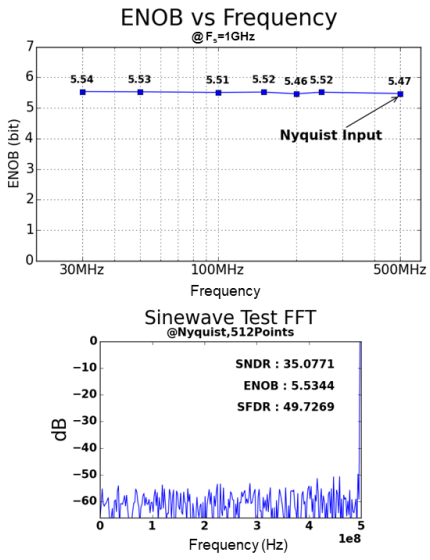

Figure 27.3.5: Measurement result.

		This Work	[2] ISSCC 2015	[3] ISSCC 2013	[5] ISSCC 2013	[6] ISSCC 2014
Technology		**40nm**	65nm	45nm	32nm SOI	28nm SOI
Type		**ciSAR**	TI SAR	TI SAR	SAR	TI SAR
Interleaving		**1**	4	2	1	8
Bits		**6**	6	9	8	6
Sample Rate (GS/s)		**1**	5	0.9	1.2	10
SNDR (@Nyquist) (dB)		**34.6**	30.8	51.2	39.3	33.8
ENOB (@HF)		**5.46**	4.8	8.2	6.2	5.3
Power (mW)		**1.26**	5.5	10.8	3.1	32
Per Channel	Sample Rate (GS/s)	**1**	1.25	0.45	1.2	1.25
	Power (mW)	**1.26**	1.375	5.4	3.1	4
	Area (mm2)	**0.00058**	0.0225	0.019	0.0015	0.001125
	Walden FoM (fJ/conv.step)	**28.7**	39.0	40.5	33.8	80.4

Figure 27.3.6: Comparison table.

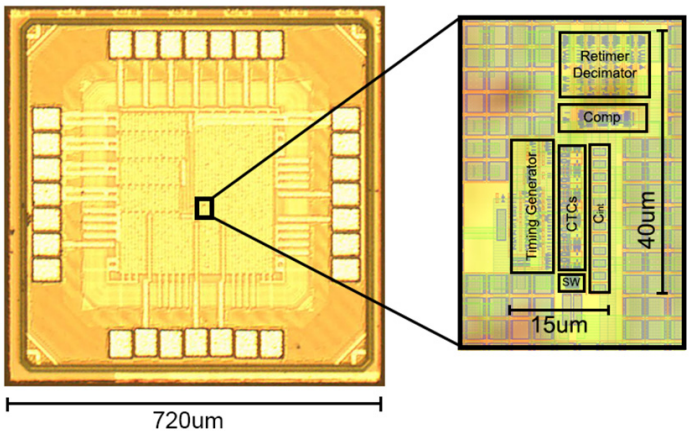

Figure 27.3.7: Die micrograph.

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