A 69 dB SNDR, 25 MHz BW, 800 MS/s Continuous-Time Bandpass $\Delta\Sigma$ Modulator Using a Duty-Cycle-Controlled DAC for Low Power and Reconfigurability

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***Abstract*—A center frequency reconfigurable continuous-time bandpass $\Delta\Sigma$ modulator is implemented in 65 nm CMOS. A new duty-cycle-controlled DAC scheme facilitates center frequency reconfiguration, and also reduces power consumption and die area by halving the total number of DACs in the modulator. A prototype sixth-order modulator, sampling at 800 MS/s, achieves a measured 69 dB SNDR over a 25 MHz bandwidth around a 200 MHz center frequency. The center frequency of the prototype bandpass $\Delta\Sigma$ modulator can be varied from 180 to 220 MHz. The total power consumption is 35 mW and the die area is 0.25 mm^2. This modulator scheme facilitates receivers that support multiple channels over a wide range of frequencies.**

***Index Terms*—ADC, bandpass, center frequency, continuous-time, delta-sigma, duty-cycle-control, low power, reconfiguration.**

I. Introduction

THE NUMBER of wireless standards supported by a single mobile device, such as a smart phone, is ever increasing. Furthermore, a single wireless standard requires several different channels to facilitate multiple users and channels can also be combined for wider bandwidth. Therefore, a wireless receiver for mobile devices should have wide tunability across different channels and different frequency bands. However, this tunability should not come at the cost of a large die size, and the tuning mechanism should be simple.

Software-defined radio (SDR) (Fig. 1) is more flexible than commonly used architectures such as the superheterodyne architecture. SDR also makes channel or band selection easier [1]–[3]. However, data conversion is a bottleneck in the implementation of SDR because of the needs for high-speed RF digitization and good power efficiency. Bandpass digitization with continuous-time bandpass $\Delta\Sigma$ modulators (CTBPDSMs) is very attractive for SDR [4] since this only digitizes around the band-of-interest and avoids side effects such as LO feedthrough that occur during down-conversion. Also, direct digitization and the inherent antialias filtering of a CTBPDSM can make the receiver chain simpler by eliminating (or relaxing the performance of) several blocks such as mixers and filters. Although CTBPDSMs remain less energy efficient than Nyquist or low-pass noise-shaping data converters, the energy efficiency of CTBPDSMs has greatly improved in recent years [5]–[7]. In addition to energy efficiency, this work also provides a bandpass signal transfer function (STF) and center frequency reconfiguration for band or channel selection, for a more practical implementation of SDRs.

The design of a CTBPDSM (i.e., feedback or feedforward) usually involves a tradeoff between power consumption and STF. A feedback-only modulator architecture has the advantage that it can provide bandpass filtering of the input signal which helps to suppress interferers and also provides more antialias filtering. On the other hand, feedforward architectures consume less power than feedback-only architectures but are prone to STF peaking [8], [9]. Inherent filtering in a CTBPDSM relaxes the requirements on the bandpass filter in front of a CTBPDSM in Fig. 1. Furthermore, it is very important to avoid STF peaking as this makes the modulator vulnerable to nearby interferers.

An SDR can be tuned between channels, by reconfiguring the center frequency of the CTBPDSM, without changing the sampling clock frequency, as shown in Fig. 2. A channel or a band at the CTBPDSM center frequency can be directly digitized. Alternatively, for a higher RF, a mixer with coarse frequency resolution in combination with a center frequency reconfigurable CTBPDSM enables channel or band tuning with a simple receiver chain. The image-rejection filtering requirement is somewhat relaxed with the help of bandpass filtering of the CTBPDSM STF.

Many reported CTBPDSMs use a sampling frequency F_s of four times the center frequency fixed. For these CTBPDSMs, F_s needs to be adjusted to select different channels or bands. However, this affects the digital output data rate and complicates the interface between the CTBPDSM and the digital processor. Another disadvantage is that changing bands or channels in this way also requires another clock synthesizer with fine resolution. On the other hand, a center frequency reconfigurable CTBPDSM has the advantage of a fixed digital output data rate regardless of the center frequency and only needs a single, fixed sampling clock frequency. Therefore, a center frequency reconfigurable CTBPDSM simplifies the receiver, providing that the modifications required for frequency tuning do not introduce

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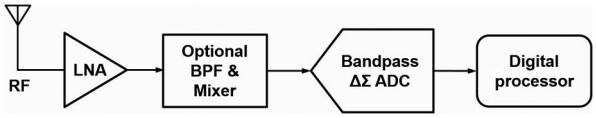

Fig. 1. Software-defined-radio architecture. A bandpass filter and a mixer may be necessary depending on the performance of a bandpass $\Delta\Sigma$ ADC.

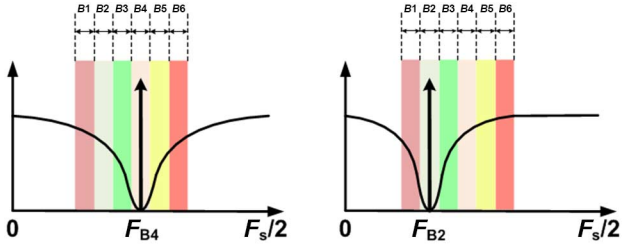

Fig. 2. CTBPDSM allows channel or band selection by the center frequency reconfiguration. This does not require the change in the sampling frequency of F_s.

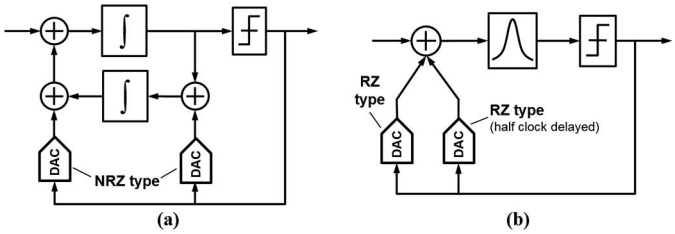

Fig. 3. CTBPDSM architectures (a) with NRZ DACs and bi-quad resonators and (b) with RZ DACs and resonators with one summing node.

additional overheads such as increased size, noise, or power consumption.

Center frequency reconfiguration of a CTBPDSM requires adjustment of the feedback and feedforward coefficients as well as adjustment of the resonant frequency of the resonators. A well-known method for the design of continuous-time modulators is discrete-time to continuous-time transformation [8]. Discrete-time to continuous-time transformation can be easily used for the CTBPDSM architecture in Fig. 3(a) which consists of a bi-quad resonator and two non-return-to-zero (NRZ) DACs. However, this architecture cannot be generally used since it needs two summing nodes and therefore is usually restricted to bi-quad resonators. On the other hand, resonators that only have a single summing node are often required. For example, LC-tank resonators have advantages for very high frequency applications, despite their larger silicon area and the poor quality factor of on-chip inductors [10]. Another method for the design of continuous-time modulators is *impulse-invariant transformation* [11], which is useful for the analysis of a CTBPDSM architecture that does not use NRZ DACs, such as in Fig. 3(b) [12]. Using impulse-invariant transformation, [12] proposes the architecture in Fig. 3(b) that utilizes return-to-zero (RZ) DACs in the feedback path and has only one virtual ground node for summing in the resonator. This architecture is more versatile because it requires only one summing node at the input of resonators and so is valid for many types of resonators [13]. Impulse-invariant transformation makes the loop impulse response of a CTBPDSM at

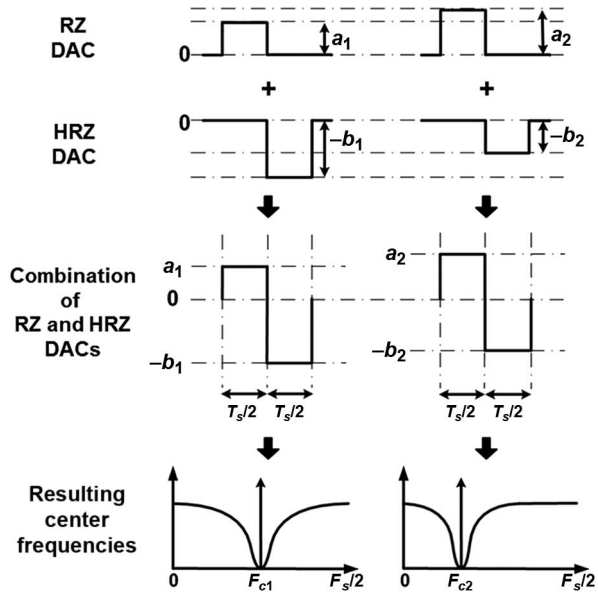

Fig. 4. Center frequency tuning for center frequencies F_{c1} and F_{c2}, with combination of RZ and HRZ DACs.

every multiple of T_s identical to the loop impulse response of a discrete-time bandpass $\Delta\Sigma$ modulator (DTBPDSM) [11].

Ref. [14] presents a center frequency reconfigurable CTBPDSM based on the architecture in Fig. 3(b). The amplitudes of the RZ and half-clock-delayed RZ (HRZ) DACs connected to each resonator are adjusted for center frequency reconfiguration as in Fig. 4. Different combinations of RZ and HRZ DAC amplitudes can provide the loop impulse response required for the different CTBPDSM center frequencies of F_{c1} and F_{c2}, assuming that the resonator is tuned appropriately. In this way, adjustment of the RZ and HRZ DAC amplitudes allows the reconfiguration of F_c However, a significant drawback of using two feedback DACs per resonator is that both DACs connected to the input resonator add noise to the modulator input. Also, the use of both RZ and HRZ DACs increases power consumption as well as silicon area. A single DAC that changes its amplitude for every half clock phase could in principle mimic the combination of RZ and HRZ DACs, but implementation is difficult in high-speed modulators. This is because changing the DAC amplitude at each clock phase can cause significant nonlinearity due to intersymbol interference related to DAC bias settling, e.g., in a current-steering DAC.

In this work, we introduce a simple, reconfigurable, sixth-order CTBPDSM architecture that uses a new duty-cycle-controlled feedback DAC. A single, duty-cycle-controlled DAC replaces the pair of RZ and HRZ DACs that are conventionally required [15] for each resonator. This new DAC scheme facilitates center frequency reconfiguration and results in a simple modulator architecture.

Section II introduces the new CTBPDSM architecture, and presents a new duty-cycle-control method, based on impulse-invariant transformation that can handle a variable center frequency. In Section III, the circuitry for each block, including the op-amp and a current-steering DAC, is explained. Section IV presents measurements of the CTBPDSM prototype.

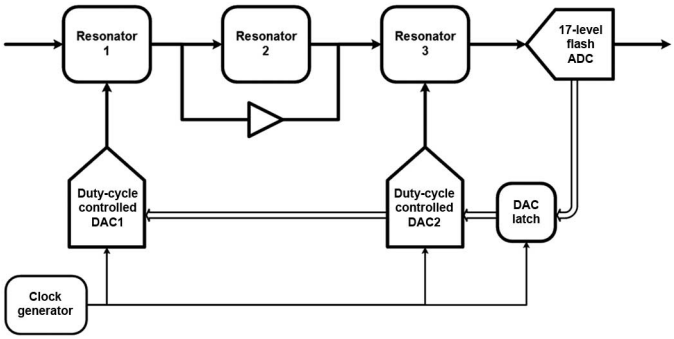

Fig. 5. System block diagram of the proposed sixth-order CTBPDSM.

II. System Architecture

A. Architecture Overview

The new sixth-order CTBPDSM, shown in Fig. 5, has three resonators and only two DACs, compared to six DACs in a conventional feedback-only, sixth-order CTBPDSM. Single-op-amp resonators [7] are used for simplicity of the modulator. As explained in Section II-B, the number of DACs is halved from six to three, thanks to DAC duty-cycle-control. (A feedforward path around the second resonator eliminates a further DAC). A single, duty-cycle-controlled DAC replaces the conventional combination of RZ and HRZ DACs that usually feed each resonator. This new duty-cycle-control scheme does not rely on feedforward paths to eliminate feedback DACs, and also enables the center frequency to be easily reconfigurable. The two DACs are connected to *Resonator1* and *Resonator3* as shown in Fig. 5.

Our new architecture has a single feedforward path from the output of *Resonator1* to the input of *Resonator3* in order to further reduce the power consumption of the modulator and to further reduce the number of DACs from three (i.e., with duty-cycle-control) to just two. We minimize peaking in STF with little SNDR penalty by reducing the gain of *Resonator2*. The lower gain of *Resonator2* makes the feedforward path dominant and leads to an SNDR between that of an ideal fourth-order and ideal sixth-order CTBPDSM. The quantizer is 4 bit flash ADC, and there is a one clock delay after the quantizer to relax the effect of excess loop delay. The sampling frequency of the modulator is 800 MS/s, and the nominal center frequency is 200 MHz. The bandwidth is 25 MHz, which results in an oversampling ratio of 16.

B. DAC Duty-Cycle-Control

To both achieve a reduction in the number of DACs and to facilitate center frequency reconfiguration, we propose a single, variable-duty-cycle NRZ DAC for use in CTBPDSMs. This single DAC replaces a pair of the RZ and HRZ DACs. Fig. 6 shows how adjustment of the duty-cycle allows a single DAC to replace the combination of RZ and HRZ DACs in a CTBPDSM. The key is that the combination of pulse width and pulse amplitude conveys the same overall information as the pulse amplitudes of the RZ and HRZ DACs. Fig. 6(a) shows the DAC waveform resulting from the combination of RZ and HRZ DACs with pulse amplitudes of a and b, respectively. The DAC waveform in Fig. 6(b) is from the new duty-cycle-controlled NRZ DAC with constant amplitude of c. Unlike conventional RZ or NRZ DACs, the duty-cycle is no longer fixed at 50%, and is varied depending on the center frequency. The variable duty-cycle of α provides additional information in addition to the amplitude c of the waveform, while the conventional combination of RZ and HRZ DACs carries information only in the form of amplitudes. Both DAC configurations have two variables; therefore, with properly chosen values of c and α, the duty-cycle-controlled DAC waveform in Fig. 6(b) can lead to the same overall sampled loop impulse response as with the combination of RZ and NRZ DACs in Fig. 6(a).

Our justification of the duty-cycle-controlled DAC begins with the simplest case, which is the second-order CTBPDSM shown in Fig. 3(b). Beginning with Z-domain analysis of a DTBPDSM, the general expression for the discrete-time frequency response of a second-order loop transfer function (i.e., resonator + DAC) is

$$\frac{-2\cos\theta z^{-1}+z^{-2}}{1-2\cos\theta z^{-1}+z^{-2}} \tag{1}$$

where θ is the center frequency with respect to the sampling frequency (i.e., $\theta=2\pi$ in the discrete-time domain). For example, when $\theta=\pi/2$, the center frequency is at the quarter of the sampling frequency and the loop transfer function becomes

$$\frac{z^{-2}}{1+z^{-2}} \tag{2}$$

as expected.

We design the CTBPDSM by making the loop impulse response, sampled at every T_s, the same as that of the DTBPDSM in (1), and in particular the same as (2) when $F_c=F_s/4$. Therefore, we configure the continuous-time blocks in a CTBPDSM to get the same sampled loop impulse response. The transfer function of a resonator in the continuous-time domain is expressed as

$$\frac{\omega_c s}{s^2+\omega_c^2} \tag{3}$$

$$\omega_c=2\pi f_c=2\pi/T_c. \tag{4}$$

The Laplace representation of a constant amplitude waveform that changes its polarity with a duty-cycle of α ($0<\alpha<1$) is

$$\frac{1-e^{-s\alpha T_s}}{s}-\frac{e^{-s\alpha T_s}\left(1-e^{-s(1-\alpha)T_s}\right)}{s}=\frac{1-2e^{-s\alpha T_s}+e^{-sTs}}{s}. \tag{5}$$

Next, the overall loop transfer function when combined with the resonator in the second-order CTBPDSM is

$$\frac{\omega_c\left(1-2e^{-s\alpha T_s}+e^{-sTs}\right)}{s^2+\omega_c^2}. \tag{6}$$

With sampling at the quantizer, and with the help of modified Z-transform [16], the Z-domain expression for the loop transfer function becomes

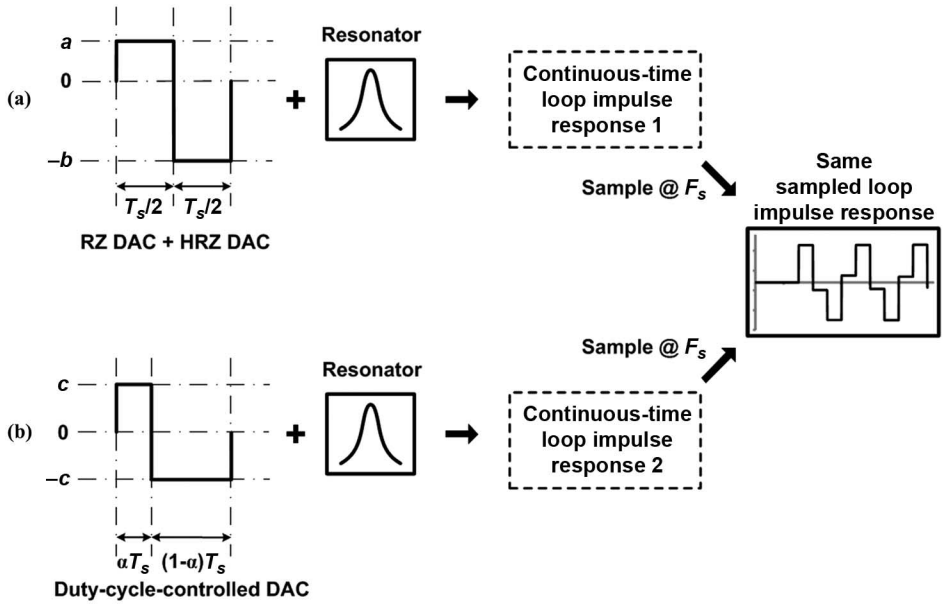

Fig. 6. Replacement of (a) combination of RZ and HRZ DACs with (b) a single duty-cycle-controlled DAC.

$$\frac{(\sin(\omega_c T_s)-2\sin(\omega_c(1-\alpha)T_s))z^{-1}+(\sin(\omega_c T_s)-2\sin(\omega_c \alpha T_s))z^{-2}}{1-2\cos(\omega_c T_s)z^{-1}+z^{-2}}. \tag{7}$$

The goal is to make (7) the same as (1) by matching the coefficients of z^{-1} and z^{-2} in the numerator. When the center frequency ω_c is given, the only variable is α and as the center frequency is varied, this equivalence is maintained by changing α.

For example, when the center frequency is $F_s/4$ and $\omega_c T_s = \pi/2$ making (1) become (2), then by setting the coefficient of the z^{-1} term in the numerator of (7) to 0, as in (2), we get

$$\sin(\omega_c T_s) - 2\sin(\omega_c(1-\alpha)T_s) = 0 \tag{8}$$

$$\sin(\pi/2) - 2\sin((1-\alpha)\pi/2) = 0. \tag{9}$$

From this, we easily get clock duty-cycle required by the second order modulatoras $\alpha = 2/3$ from (9). This same method can be used for any other center frequency. For a different center frequency $F_c(\theta = 2\pi \cdot F_c/F_s)$, α is calculated by comparing (1) and (7). The DAC duty-cycle control method is also valid when there is a single clock delay after the quantizer as long as center frequencies close to 0 or $F_s/2$ are avoided (see the Appendix).

Although the transfer function becomes more complicated, this method can also be applied for higher order CTBPDSMs. Every pair of RZ and HRZ DACs with amplitude a_k and b_k connected to each resonator is replaced with a duty-cycle-controlled DAC with amplitude c_k and duty-cycle α_k. In other words, for a $(2N)$th-order modulator, N duty-cycle-controlled DACs are necessary. Although N different duty-cycles $(\alpha_1, \ldots, \alpha_N)$ are in theory needed, considering that the coefficients of a $\Delta\Sigma$ modulator can tolerate some variation, the use of the same clock duty-cycle for all DACs in the modulator $(\alpha_1 = \alpha_k = \alpha_N)$ does not seriously deteriorate SNDR. In simulations, there is an SNDR degradation of only 1–2 dB for a sixth-order CTBPDSM when the center frequency is around $F_s/4$ and a single clock duty-cycle shared by DAC1 and DAC2 (i.e., Fig. 5) is well chosen. Furthermore, the SNDR can be kept close to the maximum value by optimizing the pulse amplitudes c_k. The sixth-order CTBPDSM architecture with one clock delay in the loop requires a 25% clock duty-cycle when the center frequency is at 200 MHz (i.e., $F_s/4$). Fig. 7 shows the duty-cycle versus center frequency derived from simulation for center frequencies between 100 and 300 MHz. The duty-cycle at each center frequency is chosen to provide the maximum SNDR as well as maximum modulator stability.

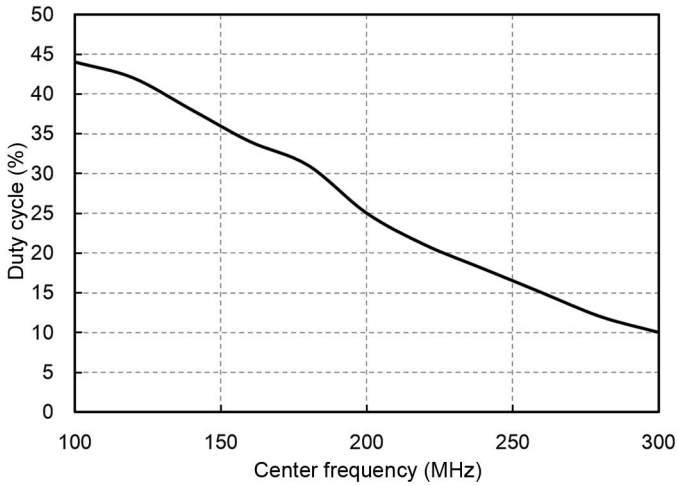

Fig. 7. Required clock duty-cycle for the modulator center frequency between 100 and 300 MHz. Nominal clock duty cycle, when $F_c = F_s/4$ is 25%.

This duty-cycle-control scheme is easily implemented in a differential modulator. The new differential DAC switches its differential outputs with a duty-cycle based on the values shown in Fig. 7. As shown by the simulated SNDR sensitivity to duty-cycle for a 200 MHz frequency in Fig. 8, the modulator is tolerant of duty-cycle variation. The modulator maintains a high

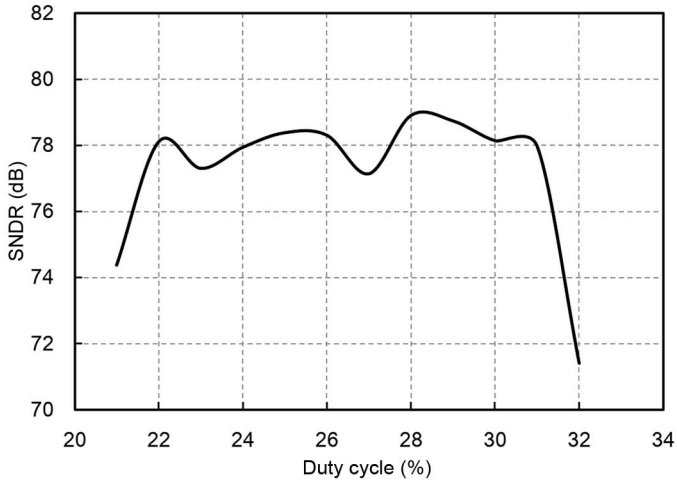

Fig. 8. MATLAB simulation of SNDR sensitivity to the clock duty-cycle variation in the nominal configuration. The modulator achieves a high SNDR for a duty-cycle range from 22% to 30%.

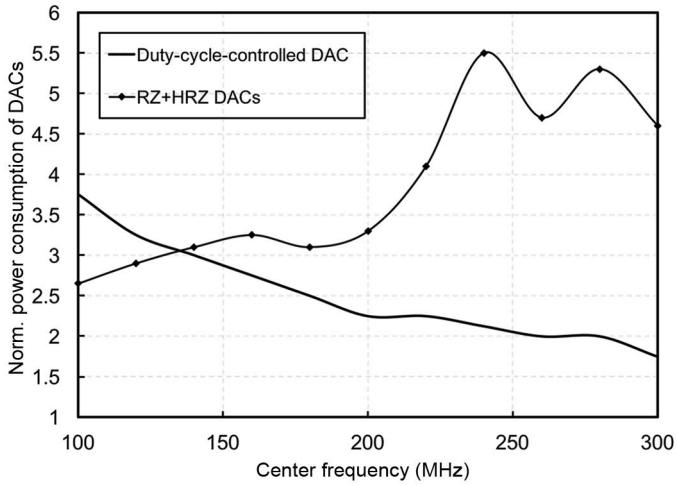

Fig. 9. Comparison of the normalized power consumption of a duty-cycle-controlled DAC with RZ and HRZ DACs for the center frequency change between 100 and 300 MHz. The power consumption only counts for the DAC bias current in a current-steering DAC which is the most dominant.

SNDR for a duty-cycle range from 22% to 30%. Beyond this, the modulator tends to become unstable and some peaking of the noise transfer function (NTF) becomes apparent, although SNDR is still high.

The DAC connected to the first resonator is most power hungry because it adds noise directly to the modulator input. A current-steering DAC is used to support a high DAC switching speed (i.e., 800 MHz). The DAC power consumption is dominated by the steered bias current flowing through DAC cells. The duty-cycle-controlled DAC scheme reduces power consumption by decreasing the total bias current for DACs. Fig. 9 compares the normalized power consumption for RZ and HRZ DAC bias currents at the modulator input in a conventional DAC scheme with that from a duty-cycle-controlled DAC which replaces the two DACs for the center frequency between 100 and 300 MHz. The duty-cycle-controlled DAC consumes less power for center frequencies above 140 MHz, and halves power consumption for a 240 MHz center frequency. Although this power saving only considers the steered DAC current, if peripheral circuits are considered, the result only changes slightly. The duty-cycle-controlled DAC requires a duty-cycle-controlled clock generator circuit. This clock generator circuitry (described in Section III-C) consumes less than 1 mW. Much of this additional power is offset by a reduction in the power consumption of the DAC drivers and the other digital circuits since the number of DACs is halved.

In addition to the substantial power reduction for center frequencies over 200 MHz, the new feedback DAC scheme generates less noise and takes less area. The steered bias current should always flow to avoid harmonics, and therefore in a differential system, RZ and HRZ DACs contribute noise to the modulator input regardless of the clock phase. Also, the DAC current sources are usually large and more DACs invariably mean more silicon area.

The clock jitter requirement for the new DAC scheme is the same as with conventional RZ/HZ DACs. The new scheme still has two edges per clock period so the clock jitter noise is same as that from a conventional RZ DAC. However, a conventional DAC scheme needs additional clock distribution circuitry (e.g., inverter chains) to support two DACs, and this generates more clock jitter noise feeding into the first resonator compared to the proposed single DAC. In comparison with an NRZ DAC, the duty-cycle-controlled DAC generates twice as much noise due to clock jitter. However, NRZ DACs can be used only for the architecture in Fig. 3(a), which supports only bi-quad resonators.

III. Block Implementation

Fig. 10 shows the top-level implementation of the modulator. Considering limitations such as thermal noise, the design targets 11 bit ENOB. Three resonators are connected in series through resistors and capacitors in order for the op-amp output to directly drive the following resonator [7]. A feedforward path through a capacitor and a resistor connects the op-amp output of the first resonator directly to the virtual ground node of the third resonator. This feedforward path helps to lower power consumption by reducing the signal swing through the resonators and also eliminates the DAC for the second resonator. The DACs are current-steering DACs and the duty-cycle for the DACs is controlled by a clock generator (described later) consisting of a clock receiver and a bias generator. The quantizer is a 17-level flash ADC with comparator-offset calibration.

A. Op-amp

The target resolution of this modulator is 11 bit, and this requires very low noise contributions from the passive components and the op-amp. The input resistors are set to 2KΩ. The op-amp is designed to have a thermal noise contribution of around half that of the input resistors. In addition to the tight noise requirement, the op-amp needs to have wide bandwidth in order to operate around the desired 200 MHz center frequency. Furthermore, the op-amp should have high linearity to achieve an SFDR of at least 10 dB higher than the target SNDR.

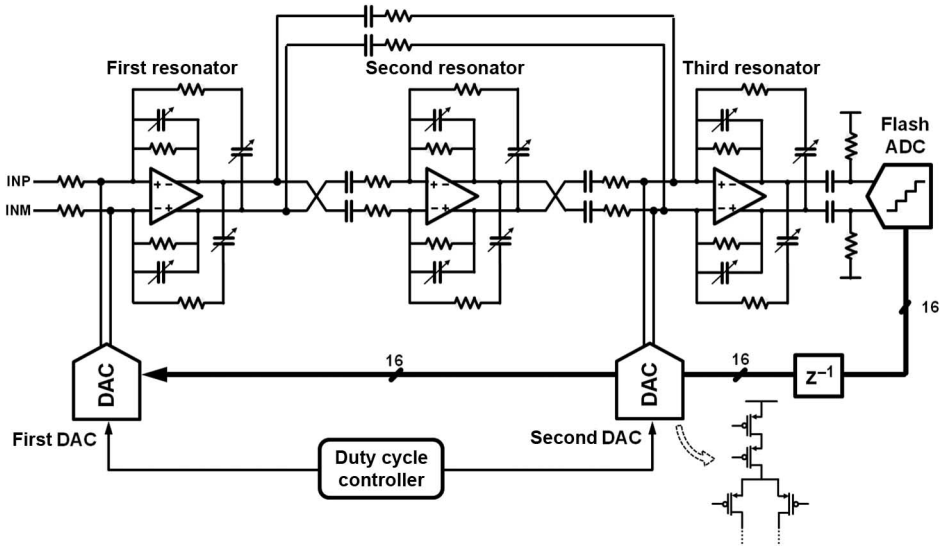

Fig. 10. Circuit-level implementation of the main blocks in the proposed sixth-order CTBPDSM.

A multistage op-amp is attractive because it delivers a large bandwidth and high gain with relatively low power consumption, and the structure in [17] is used in this work. The gain gradually decreases as the frequency increases due to internal capacitors loading each stage. A total of four paths are used to achieve more than 50 dB gain at 200 MHz and suppress in-band intermodulation. The op-amp for the first resonator, located at the modulator input, has a 450 MHz 3 dB bandwidth and 57 dB dc gain when loaded with the feedback network components. The phase margin is approximately 50°. A separate high supply voltage of 1.7 V and high voltage I/O devices are used for the last stage to achieve a large voltage swing and to get high linearity. The other stages run from a 1.2 V supply. The power consumption of the first resonator is 7.5 mW, while the other two resonators consume a total of 9 mW.

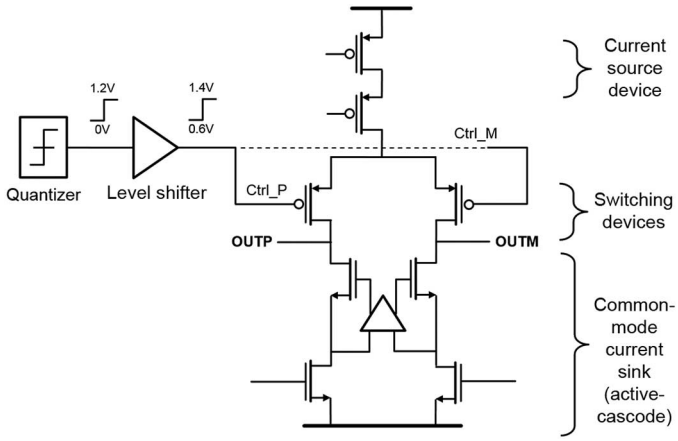

Fig. 11. Triple-cascode PMOS DAC (top) and NMOS common-mode current sink (bottom).

B. DAC

A current-steering DAC facilitates high-speed operation of the modulator. A large V_{GS} helps to lower the g_m and thus reduce the output current thermal noise. The regular 1.2 V supply voltage is not large enough to enable a sufficiently large V_{GS}, especially if a triple-cascode DAC structure is used for high output resistance. Therefore, a 2.5 V supply voltage and I/O devices are used to get a very large gate-source voltage for the current source devices. The virtual ground node voltage of the resonator is at 1 V, so PMOS stacks are used for the current-steering DAC unit cells, as shown in Fig. 11. With a 2.5 V supply and a 1 V output, the voltage headroom available for the triple-cascode structure is 1.5 V. 1 V of this 1.5 V is assigned to the PMOS current source devices to achieve a noise contribution equivalent to that of the first op-amp. The remainder of the headroom is assigned equally to the cascode devices and the switching devices.

The DAC is driven by a pair of level shifters since the full-swing digital output of the quantizer is inappropriate for the DAC switches. These level shifters should turn ON the switching device fast enough to suppress noise and nonlinearity caused by slow transitions. Also, the differential outputs of the level shifters should cross over at a low voltage to prevent both PMOS switches from both being OFF at any time [18]. The output common mode voltage of the DAC is 1 V, and the switching devices of DACs become saturated at a gate voltage of 0.6 V and turn OFF completely at 1.4 V. With the help of level shifters, the digital outputs from the DAC latch swing between 0.6 and 1.4 V.

The NMOS current source in the lower part in Fig. 11 is necessary to sink the common-mode current generated by the PMOS current source. The NMOS source is an active cascode structure. The active cascode keeps the output impedance high and also facilitates a large gate-source voltage for the NMOS current source to minimize thermal noise even with the low voltage of 1 V allotted for the NMOS current source.

C. Clock Generator

The default duty-cycle for the modulator is 25%, and as described in Section II-B, different duty-cycles are required

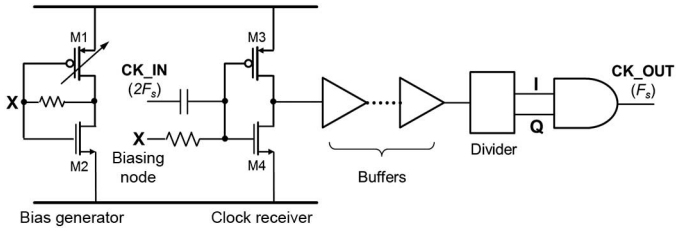

Fig. 12. Clock generator consisting of a $2F_s$ clock receiver, buffers, a divider, and an AND gate. A bias generator adjusts dc bias of node X, and changes the duty-cycle of the $2F_s$ clock.

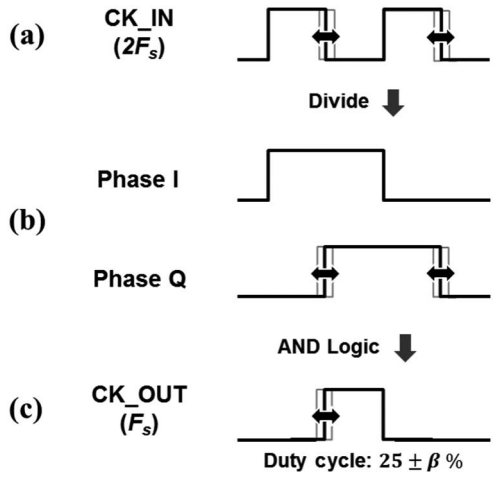

Fig. 13. Clock waveforms of (a) received $2F_s$ clock with variable duty-cycle; (b) divided I and Q clocks and; (c) ANDed variable duty-cycle F_s clock output.

for different center frequencies. The clock generator circuit is shown in Fig. 12 and the clock waveforms are shown in Fig. 13. A clock signal running at twice the sampling frequency (i.e., $2F_s$) feeds the clock generator, which makes a low jitter sampling clock at F_s with a variable duty-cycle around 25%. First, the $2F_s$ clock input is received by the clock receiver in Fig. 12, which changes the duty-cycle of the $2F_s$ clock with the help of a variable bias generator. The dc input bias voltage of the inverter in the clock receiver affects the duty-cycle, and therefore instead of using conventional resistive feedback to set the bias, a separate bias circuit sets the dc bias voltage. The voltage at node X in Fig. 12 is generated by the bias generator, which controls the bias voltage at node X by varying the size of $M1$. To do this, several PMOS transistors connected in parallel are turned ON or OFF depending on a digital control signal and thereby change the duty-cycle of the $2F_s$ clock as in Fig. 13(a). The bias generator barely contributes noise, and so uses minimum-sized transistors to reduce power consumption. The variable duty-cycle $2F_s$ clock signal goes through a divider to generate divided I and Q clocks, shown in Fig. 13(b). Following this, an AND gate combines the I and Q signals to generate the clock output with the required duty-cycle. The default duty-cycle is 25% and is varied by $\pm\beta\%$, as shown in Fig. 13(c).

Clock jitter is important since it fills the noise notch in the NTF in a manner similar to the thermal noise of the op-amps and DACs. Inverter chains with a large (W/L) ratio are used for the clock distribution to reduce the clock jitter. The clock jitter requirement for this modulator to achieve around 80 dB SNDR is estimated to be 500 fs, based on [19]. Inverters are sized to have the clock jitter of 250 fs, for margin.

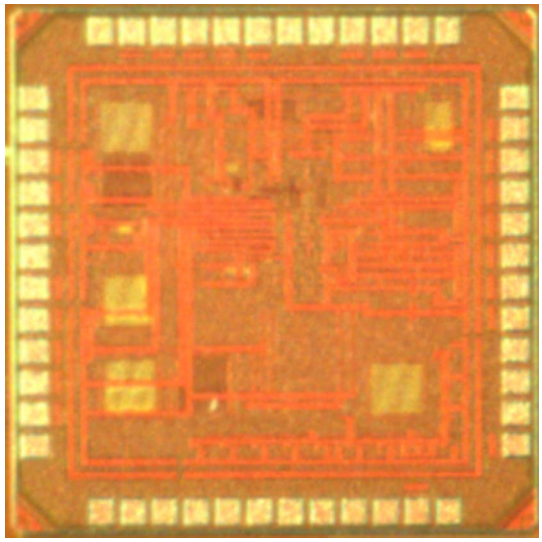

Fig. 14. Die photograph.

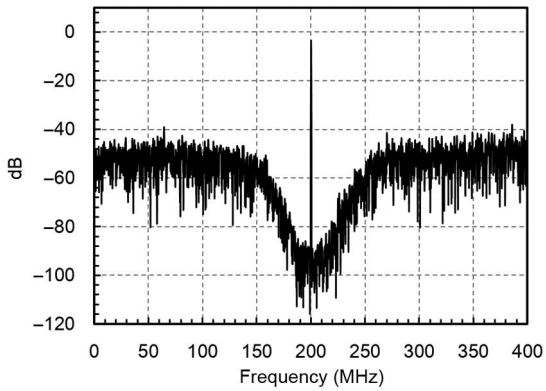

Fig. 15. Measured output power spectrum density shows 69 dB SNDR with a −3.5 dBFS 200 MHz center frequency and a 25 MHz bandwidth.

IV. Measurements

The prototype is fabricated in 65 nm CMOS [20]. Fig. 14 shows a die photo. The total active area is 0.25 mm^2. All biasing is done on-chip. Calibration of capacitors in the resonators is performed before evaluating the normal operation of the modulator. The quality factor is measured by directly feeding an off-chip sinusoidal input signal to each resonator while disabling the other circuits and observing the resonator output with a spectrum analyzer. This makes it easier to evaluate individual resonators independently and avoids signal saturation caused by the extremely high gain of all three resonators in series. All resonators are tuned to have quality factors above 20.

Fig. 15 shows the SNDR measurement when F_c is set to the nominal center frequency of 200 MHz (8192 points for FFT). The measured SNDR is 69 dB over a 25 MHz bandwidth with a 800 MHz sampling rate. Thanks to the use of the higher supply voltage at the output stage of op-amps, the third

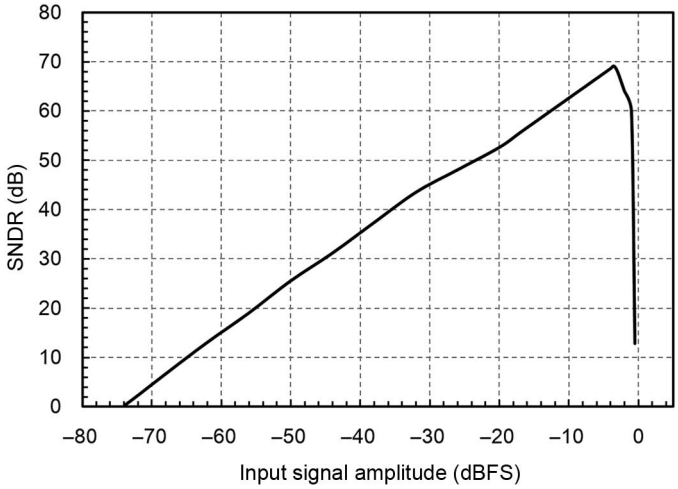

Fig. 16. SNDR versus modulator input amplitude. The measured dynamic range is 70 dB with a center frequency at 200 MHz.

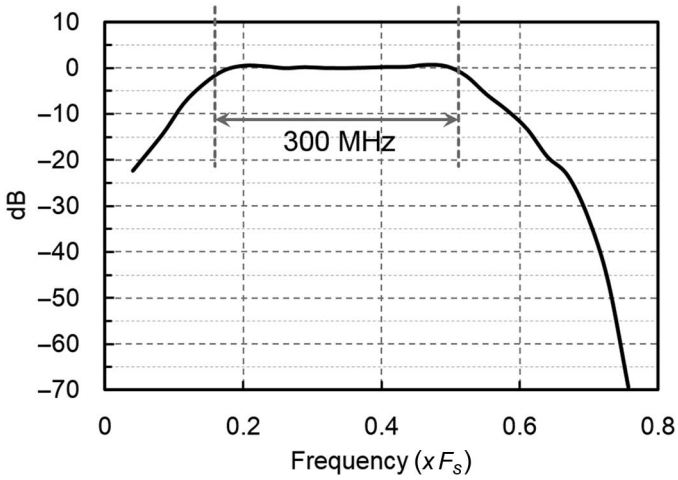

Fig. 17. Measured STF. The input signal bandwidth is 300 MHz.

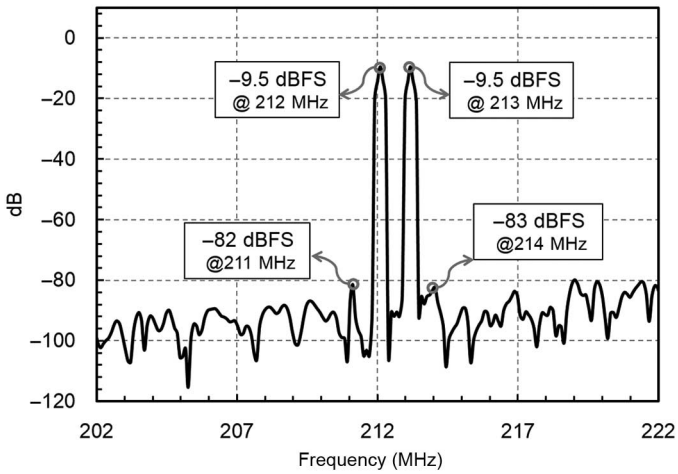

Fig. 18. Measured output power spectrum density with a -9.5 dBFS two-tone input around the band edge shows 73 dB IM3.

harmonic is suppressed enough to not affect the SNDR. The duty-cycle-controlled DAC shows the expected noise shaping in the measured output power spectrum density. There is no asymmetry or peaking in the NTF since the duty-cycle-controlled DAC does not cause any stability issue. The measured dynamic range at 200 MHz is 70 dB and SNDR versus input amplitude is shown in Fig. 16.

The STF is measured by simultaneously feeding two tones to the input of the modulator. One tone fixed at the center frequency and the other tone is varied between $0 < F_c < 0.75F_s$

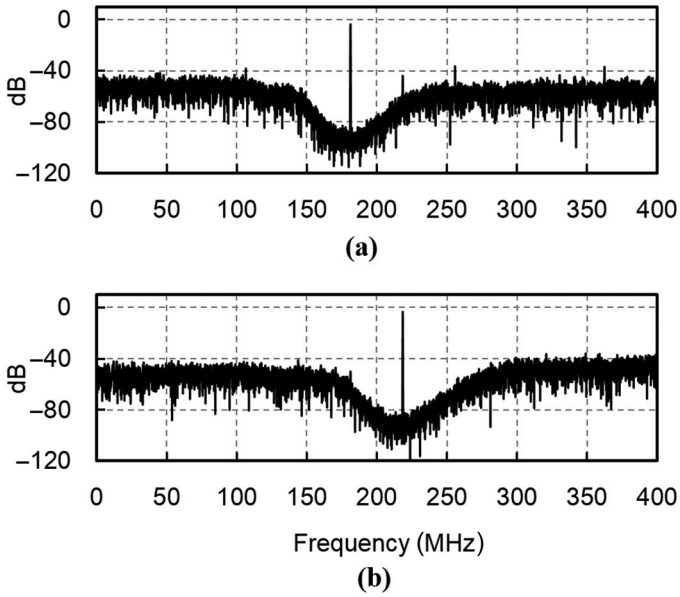

Fig. 19. Measured output power spectrum density with different center frequencies. (a) 180 MHz. (b) 220 MHz.

TABLE I
SUPPLY VOLTAGE AND POWER CONSUMPTION OF MAIN BLOCKS

Analog		
Resonators	1.2 V + 1.7 V	16.5 mW
DAC	2.5 V	4.3 mW
Bias	1.2 V	1 mW
Quantizer	1.2 V	6.6 mW
Clock gen	1.2 V	4.8 mW
DAC driver	0.6 V + 1.4 V	1.8 mW
Total		35 mW

TABLE II
PERFORMANCE SUMMARY

Center frequency	180 MHz, 200 MHz	220 MHz
Sampling rate	800 MHz	800 MHz
BW	25 MHz	25 MHz
Power	35 mW	36 mW
SNDR	69 dB	69 dB
DR	70 dB	70 dB
Area	0.25 mm^2	0.25 mm^2
FoM	320 fJ/conv.	330 fJ/conv.

TABLE III
STATE-OF-THE ART CTBPDSMs

	Lu 2010 [21]	Harrison 2012 [5]	Shibata 2012 [6]	Atac 2013 [22]	Chae 2014 [7]	This work
Order	Sixth	Sixth	Sixth	Third	Fourth	Sixth
DR (dB)	70		74	60	60	70
Fs (MHz)	800	3200	4000	32	800	800
Fc (MHz)	200	7–800	0–1000	1	200	180–220
BW (MHz)	10	20	150	1	24	25
SNDR (dB)	68.4	70		58.6	58	69
SNR (dB)			69			
Power (mW)	160	20	550	1.7	12	35–36
Area (mm^2)	2.5	0.4	5.5	0.62	0.2	0.25
Process	0.18 um CMOS	40 nm CMOS	65 nm CMOS	130 nm CMOS	65 nm CMOS	65 nm CMOS
[1]FoM (pJ/ Conv.)	3.72	0.19	0.8	1.2	0.38	0.32
[2]FoM (dB)	146	160	153	146	151	157

[1]$\text{FoM} = \text{Power}/(2^{\text{ENOB}} \times \text{BW})$.
[2]$\text{FoM} = (\text{DR})_{\text{dB}} + 10\log_{10}(\text{BW}/\text{Power})$.

while measuring the output power difference between the two tones. The measured STF is shown in Fig. 17. The 3 dB bandwidth of the modulator input is 300 MHz. The maximum peaking is less than 1 dB verifying that the modulator is robust to near-band interferers.

Fig. 18 shows the measured output power spectrum density with a two-tone input. The tones are 1 MHz apart, and are located around the edge of the bandwidth. The measured IM3 is 73 dB. Fig. 19 shows the operation of the prototype at other center frequencies. The center frequency of the prototype can be configured from 180 to 220 MHz, since the resonator has a $\pm 10\%$ tuning range. The duty-cycle is varied from 21% to 31% for this tuning range. Fig. 19(a) and (b) shows the measured power spectrum densities at 180 and 220 MHz. The measured SNDR is 66 and 67 dB, for 180 and 220 MHz center frequencies, respectively.

The total power consumption, including that of the clocking and bias generator, is 35 mW. This corresponds to a Walden figure-of-merit (FoM) of 317 fJ/conv and a Schreier FoM of 157 dB. Table I shows the power consumption and the supply voltage for each block. The resonators use dual supplies and the DACs run from a 2.5 V supply in order to get better noise and linearity performance. The digital blocks use the regular 1.2 V supply.

Table II summarizes the performance of this prototype. There is 1 mW increase in the power consumption due to the increased DAC bias when the center frequency is 220 MHz. Table III compares this work with state-of-the-art CTBPDSMs. To our knowledge, this work demonstrates the best energy efficiency for a CTBPDSM that uses active resonators. The design also enables reconfigurability of the modulator.

V. Conclusion

A duty-cycle-control method facilitates center frequency reconfiguration, and reduces the power consumption and area of a CTBPDSM. A single DAC with duty-cycle-control replaces the conventionally needed pair of RZ and HRZ DACs, and greatly reduces the total number of DACs in the modulator. A sixth-order architecture based on the new DAC scheme is presented, and an op-amp and a DAC to support high resolution are also introduced.

A prototype CTBPDSM, based on duty-cycle-control, achieves 11 bit ENOB for a 25 MHz bandwidth. With a power consumption of 35 mW, the CTBPDSM achieves a better energy efficiency than state-of-the-art designs that use active resonators. The design methods presented in this work make CTBPDSMs ideal for future receivers by improving energy efficiency and enabling RF flexibility to allow the elimination of several blocks in a receiver.

Appendix

The DAC duty-cycle-control method introduced in Section II-B is also valid when there is a single clock

delay after the quantizer. This is proved in different ways for $F_c = F_s/4$ and $F_c \neq F_s/4$. First, considering $F_c = F_s/4$, a single clock delay multiplies (7) by z^{-1}

$$\frac{(\sin(\omega_c T_s) - 2\sin(\omega_c(1-\alpha)T_s))z^{-2} + (\sin(\omega_c T_s) - 2\sin(\omega_c \alpha T_s))z^{-3}}{1 - 2\cos(\omega_c T_s)z^{-1} + z^{-2}} \tag{10}$$

and when the center frequency is $F_s/4$, by comparing (2) and (10) we get

$$\sin(\omega_c T_s) - 2\sin(\omega_c \alpha T_s) = 0. \tag{11}$$

The required clock duty-cycle changes to 1/3 from 2/3 due to the single clock delay. By removing the third-order term in the numerator of (10), the resulting loop impulse response is the same as that without clock delay.

For $F_c \neq F_s/4$, (10) cannot be made equivalent to (1) due to the first-order term in (1) and the third-order term in (10). However, (10) can still provide noise-shaping in the NTF by adjusting α. The prototype loop impulse response (1) generates a NTF of

$$\frac{z^2 - 2\cos\theta z + 1}{z^2} \tag{12}$$

since the NTF equals $1/\{1 - (\text{loop transfer function})\}$.

The additional z^{-1} in (10) due to a single clock delay leads to a NTF of

$$\frac{\left(z^2 - 2\cos\theta z + 1\right) z}{\left(z - c_0\right)^2 \left(z + c_0/2\right)}, \mathrm{c}_0 \langle 0, \text{and } \mathrm{c}_1 \rangle 0 \tag{13}$$

for a given value of α, and poles are located at c_0 and $-c_0/2$. Adjustment of α makes c_0 real and less than 1 in magnitude. Therefore, the single clock delay after the quantizer does not affect the stability of the whole loop. With these pole locations, noise shaping is not significantly affected as long as the center frequency is not very close to 0 or $F_s/2$. To summarize, the duty-cycle-controlled DAC can operate with one clock delay in the modulator feedback loop if center frequencies close to 0 or $F_s/2$ are avoided.

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