ADC Trends and Impact on SAR ADC Architecture and Analysis

(Invited Paper)

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***Abstract* — The performance of ADCs continues to improve with process scaling. For low to moderate resolutions, SAR ADCs deliver the best energy efficiency. Interleaved SAR converters have become popular for very high sampling speeds. The SAR assisted scheme has dramatically improved the energy efficiency of higher resolution pipeline ADCs. This paper reviews the fundamental limits of the energy efficiency of the SAR architecture, considering the energy consumption of the capacitor array and of the comparator. ADCs. ADC yield as a function of capacitor matching is also considered.**

***Index Terms* — SAC ADC, comparator, capacitor, FOM, pipeline, SAR assisted.**

I. Introduction

Defying some predictions, the performance and energy efficiency of analog-to-digital converters (ADCs) have improved steadily over the past two decades. No one ADC architecture dominates the entire application space and instead the choice of architecture depends on the required performance. Broadly, as shown in Fig. 1, there are four main types of ADC. Noise shaping ADCs satisfy high-resolution low-bandwidth applications. SAR ADCs are very effective for medium resolution and low-to-medium sampling speeds. Higher sampling speeds and higher resolution require pipelining. Very-high-speed, low-resolution ADCs can be implemented with the flash architecture.

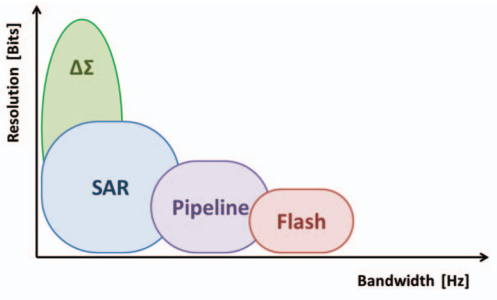

Figure 1: ADC architectures

The tradeoff between resolution and bandwidth is further quantified in Fig. 2, which surveys measured performance data from scholarly published ADCs based on [1]. As shown in Fig. 2, ADC resolution, expressed in signal-to-noise-and-distortion (SNDR), decreases at higher signal bandwidths. This is in part due to sampling jitter and Fig 2. also traces the maximum SNDR that can

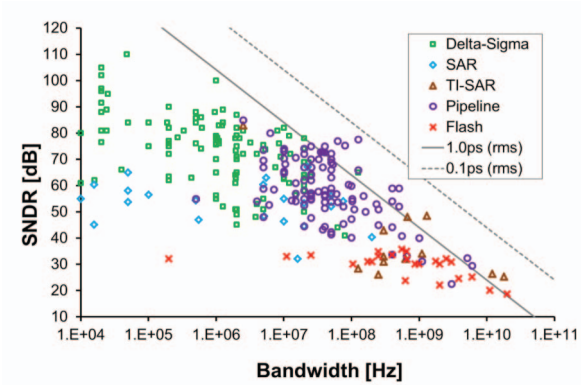

Figure 2: Survey of resolution versus bandwidth for various ADC architectures with data compiled from 2015 online survey [1]

be achieved for a sampling jitters of 1ps(rms) and 0.1ps(rms). As in the sketch of architectures provided in Fig 1, ΔΣ ADCs dominate high resolution applications, while flash ADCs dominate high bandwidth applications.

A closer look at the figure shows the extensive role played by SAR ADCs. These dominate for low to moderate resolutions and moderate bandwidths. Moderate-resolution moderate-speed SAR ADCs achieve remarkable energy efficiency (~5fJ/conversion.step) [2]-[4]. Recently, at the other end of the performance spectrum, interleaved SAR ADCs have become attractive for very-high-bandwidth moderate-resolution analog to digital conversion, displacing flash ADCs [5]-[6].

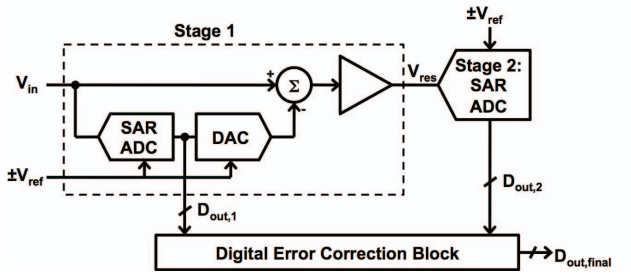

Figure 3: SAR assisted pipeline ADC

Although pipeline converters play a continued role for moderate to high resolution high-speed conversion, these too have been affected by the improvements in SAR ADC performance. In particular, the SAR assisted pipeline

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architecture [7]-[9] allows pipeline ADCs to achieve record efficiency. A SAR assisted pipeline ADC (Fig. 3) is a two-stage pipeline that uses the SAR architecture to implement the both the first and second stage sub-ADCs. Compared to a conventional pipeline ADC, this allows a higher first stage resolution, thereby improving linearity and reducing amplifier power consumption. Compared to high resolution SAR ADCs, the SAR assisted pipeline architecture has the advantages of higher throughput and relaxed comparator noise.

Although SAR based quantizers are rarely used in ΣΔ ADCs, a recent innovation is to use noise-shaping to improve the resolution of SAR ADCs. Noise shaping shapes both quantization noise and the input referred noise of the comparator so the SAR ADC comparator no longer needs to have the full accuracy of the overall ADC. Noise-shaping provides a means to enhance the resolution of a SAR ADC without significant modification to the basic SAR ADC structure [10].

The rest of the paper is divided as follows. Section II and Section III examine the energy efficiency of charge-redistribution SAR ADCs. Although an energy analysis of the digital SAR controller is omitted form the analysis, a detailed look at the energy consumption of the SAR capacitor DAC and comparator is presented in terms of the resolution and bandwidth constraints. Section IV, examines the effects of capacitor mismatch on ADC resolution and yield. The analysis on capacitor mismatch is quite intensive, but the analysis is the first to relate resolution, yield, and mismatch for SAR ADCs with a complete closed-form statistical model [11].

II. DAC Switching Energy

This section derives an expression for the DAC switching energy of a SAR ADC. The derivation begins by analyzing the energy consumption of a binary weighted capacitor array during a single switching event and continues by summing these energy contributions across complete conversion cycles for a uniformly distributed input. Fig. 4 presents the model used to calculate the DAC switching energy. In this model, the differential DAC consists of two single ended capacitors arrays each comprised of 2^{N-1} unit capacitors – where N is the differential DAC resolution in bits. Furthermore, each half of the array uses both positive and negative reference voltages to permit addition and subtraction of voltage at the DAC output during conversion. SAR ADCs using similar DACs are found in [12]-[13].

In terms of implementation, this dual reference switching scheme is more complex than single reference switching schemes [13], but from an energy perspective,

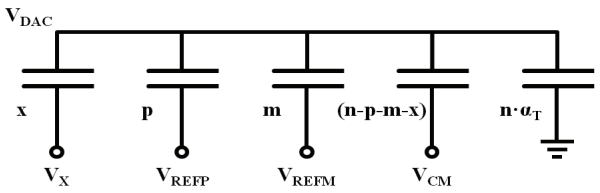

Figure 4: Single-ended circuit model used to calculate the DAC switching energy due to switching x capacitors from V_{CM} to either V_{REFP} or V_{REFM}. V_X describes final the switching reference voltage (either V_{REFP} or V_{REFM}), the quantities x, p, m, and (n-p-m-x) describe the number of unit capacitors at particular voltages, n is the total number of capacitors, and α_T describes the top plate parasitic capacitance normalized to the array capacitance

this switching operation is more efficient since each capacitor is charged by a reference voltage only once – whereas a DAC using a single reference voltage may need to switch a capacitor twice: once during a trial bit test and again when setting the final bit decision. Although recent literature shows a variety of other energy efficient DAC implementations, the energy efficiency of those implementations is comparable to this DAC [13].

We first calculate how the DAC output voltage responds to single switching events. As shown in Fig. 4, the change in the DAC output voltage due to switching x capacitors through a voltage difference of ΔV_X is calculated by applying conservation of charge at the top plate of the DAC. Equating the charge on the top plate before and after switching the reference voltage for the x capacitors to ΔV_X, we derive (1):

$$\Delta V_{DAC} = \frac{x}{n(1+\alpha_T)}\Delta V_X \quad (1)$$

Equation (1) describes the change in the DAC output voltage after a single switching event – where ΔV_{DAC} describes the change in the DAC voltage, n is the total number of unit capacitors, x is the number switched by a voltage difference of ΔV_X, and α_T is fractional top plate parasitic capacitance as normalized by the total array capacitance.

Next, we calculate the energy consumed by the reference voltages during switching events. During the switching of the x capacitors, transient currents flow from the reference voltages at each node and shuffle charge between the array capacitors in order to equalize the DAC top plate potential. The energy consumption of the DAC is calculated by integrating the power associated with each these currents over time. Fig. 5 presents an abstract model for calculating the switching energy contributed by each node in the array. Assuming the bottom plate of an isolated unit capacitor is connected to some arbitrary

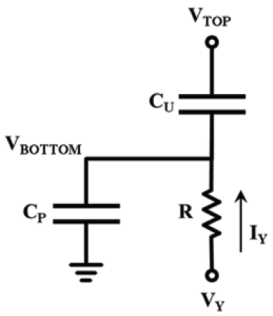

Figure 5: Circuit model used to calculate the switching energy of an arbitrary capacitor from the array. C_U is the unit capacitance, C_P is the bottom plate parasitic capacitance, R is the switch resistance, V_Y is the node reference voltage (either V_{CM}, V_{REFP}, or V_{REFM}), and I_Y is the current delivered by V_Y.

voltage V_Y through a switch resistance R, the calculation of the energy contribution from this node is shown in (2):

$$\Delta E_Y = V_Y \int_0^\infty I_Y(t)dt \qquad (2)$$

Since the time integral of current is charge, ΔE_Y is the product of V_Y and ΔQ_Y – where ΔQ_Y is the change in charge at the bottom plate node. Equation (3) describes the change in energy associated with switching the reference voltage to V_Y through a voltage difference of ΔV_Y. By convention, a positive ΔE_Y indicates energy consumption, and a negative ΔE_Y indicates energy recovery.

$$\Delta E_Y = \left[C_u\left(\Delta V_Y - \Delta V_{TOP}\right) + C_p \Delta V_Y\right] V_Y \qquad (3)$$

Next, we iterate the results from (3) across each of the DAC nodes and calculate the energy for the entire differential DAC. During the switching of *x* capacitors, as described in Fig. 4, the energy contributions at each node are calculated and summed. Assuming a differential array structure, which switches the references voltages oppositely, the energy contributions calculated from (3) are summed across every node for both halves of the differential array. The ΔV_{TOP} term in the resulting expression is simplified using (1) since ΔV_{TOP} is equal to ΔV_{DAC}.

The simplified result of this calculation is shown in (4), which describes the change in energy for the differential DAC during the switching of *x* capacitors in each array through a differential voltage of $\Delta V_{X,DIFF}$ – where $|\Delta V_{X,DIFF}| = \frac{1}{2}V_{FS}$, $V_{REFP} - V_{REFM} = \frac{1}{2}V_{FS}$, α_P is the bottom plate parasitic capacitance normalized to a unit capacitance, α_T is the top plate parasitic capacitance normalized to the array capacitance, *n* is total number of capacitors in each half of the array, and the quantities *p* and *m* represent the number of capacitors connected to the positive and negative reference voltages as shown in Fig. 4.

$$\Delta E = \Delta E_{Indpendent} + \Delta E_{Depdendent}$$

$$\Delta E_{Indpendent} = \tfrac{1}{8} C_u V_{FS}^2 \left[x\left(1+\alpha_p\right) - \frac{x^2}{n\left(1+\alpha_T\right)}\right] \qquad (4)$$

$$\Delta E_{Dependent} = \tfrac{1}{8} C_u V_{FS}^2 \left[\frac{x\left(m-p\right)}{n\left(1+\alpha_T\right)}\right] \mathrm{sign}\left(\Delta V_{X,DIFF}\right)$$

Equation (4) is decomposed into two parts: a state independent energy term and a state dependent energy term. Since the energy dissipated by the reference voltages during a single switching event depends on the state of the DAC switches, the power dissipation of the DAC during a complete conversion cycle varies as a function of the sampled input voltage. The independent term describes the constant amount of energy required to switch x capacitors – independent of the DAC switch arrangement. The dependent term describes the excess switching energy that is either expended or recovered during a switching event as a function of the DAC switch configuration.

Fig. 6 graphs the normalized energy contributions from the state independent and dependent terms summed throughout the switching events of a complete conversion cycle. As shown in the figure, the average state dependent energy contribution across the ADC codes is zero. Hence, the state dependent energy contribution for a uniformly distributed input signal is zero and can be neglected. Note that the average state dependent energy contribution for a sinusoidally distributed input signal is negative since its probability density is higher at the outer codes than the middle codes. Therefore, the assumption of a uniformly distributed inputs result in a slightly pessimistic energy approximation when considering sinusoidally distributed inputs.

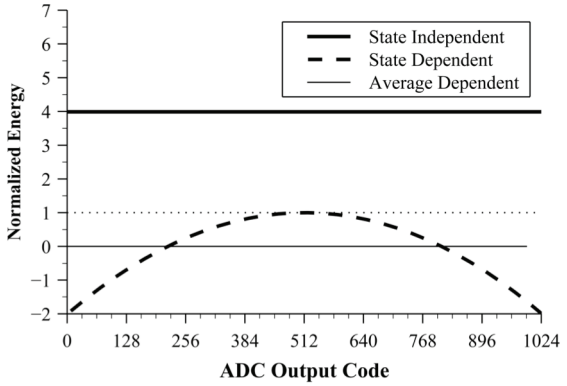

Figure 6: Normalized energy contributions versus 10 bit ADC output code for both the state dependent and state independent terms. For comparison purposes, both, α_T and α_P are set to zero.

Finally, we derive the average switching energy of the DAC. By summing each of the state independent switching energy contributions described by (4) throughout a complete conversion cycle, we calculate the average energy. Equation (5) describes the average energy consumption after completing the summation – where *N* is the number of bits. The parameter *x* from (4) is summed in a descending binary fashion from 2^{N-2} down to 2^0 in order to capture the binary weighting of the DAC capacitors. Note that the summation proceeds from 2^{N-2} since the MSB capacitor in each half of the differential array consists of 2^{N-2} unit capacitors and only *N-1* switching events are needed during a complete conversion cycle.

$$\Delta E_{DAC} = \tfrac{1}{8} C_u V_{FS}^2 \left[(1+\alpha_p)(2^{N-1}-1) - \frac{2^{N-1}-2^{1-N}}{3(1+\alpha_T)} \right] \quad (5)$$

In the limit of large N, we can approximate (5) as (6):

$$\Delta E_{DAC} \cong \tfrac{1}{16} 2^N C_u (1+\alpha_p) V_{FS}^2 \left[1 - \frac{1}{3(1+\alpha_T)(1+\alpha_p)} \right] \quad (6)$$

Equation (6) is further simplified by relating the DAC capacitance to the kT/C noise incurred during sampling. When a signal is sampled through bottom plate sampling, each unit capacitor acquires some noise voltage. The total sampling noise of the DAC is calculated by summing the noise power contributions from all the unit caps of the differential array, which yields (7) – where σ sampling is expressed as a fraction of an LSB. The noise power expression in (7) is just the kT/C noise of the sampled voltage.

$$\sigma_{sampling}^2 = \frac{1}{LSB^2} \cdot \frac{kT}{2^N C_u} \quad (7)$$

Substituting the sampling noise expression from (7) into the DAC switching energy expression from (6) yields (8) – which describes the DAC energy in terms of the sampling noise.

$$\Delta E_{DAC} \cong \frac{kT}{16} \left(\frac{2^N}{\sigma_{sampling}} \right)^2 (1+\alpha_P) \left[1 - \frac{1}{3(1+\alpha_T)(1+\alpha_P)} \right] \quad (8)$$

Equation (8) describes the average DAC switching energy across a full SAR conversion cycle for a uniformly distributed input. As shown in (8), the energy consumed by the DAC increases as the resolution, *N*, of the array increases. We can, however, express (8) in a more convenient form by expressing the energy in terms of the signal-to-noise ratio of the sampled DAC voltage. The definition of the signal-to-noise ratio is given by (9).

$$SNR = \frac{Signal\ Power}{Noise\ Power} \quad (9)$$

If we express the signal power and noise power from (9) in terms a full scale sine-wave input signal and the sampled kT/C noise, we arrive at (10) – where V_{FS} is the full-scale voltage range of the DAC.

$$SNR_{DAC} = \frac{\left(\frac{V_{FS}}{2\sqrt{2}}\right)^2}{\left(LSB \cdot \sigma_{sampling}\right)^2} \quad (10)$$

Since V_{FS} is equal to $2^N \cdot$LSB, we can further simplify this expression. The simplified expression is provided by (11).

$$SNR_{DAC} = \frac{1}{8} \left(\frac{2^N}{\sigma_{sampling}} \right)^2 \quad (11)$$

Equation (11) expresses the signal-to-noise ratio of a sampled voltage on the capacitor DAC in the presence of kT/C noise. If we substitute (11) into (8), we can express the energy of capacitor DAC as function of the sampled signal-to-noise ratio and the parasitic capacitances for the top plate, α_T, and the bottom plate, α_P.

$$\Delta E_{DAC} \cong \frac{kT}{2} \cdot SNR_{DAC} \cdot \left[(1+\alpha_P) - \frac{1}{3(1+\alpha_T)} \right] \quad (12)$$

As shown by equation (12), the DAC energy consumption increases linearly with both the available signal-to-noise ratio of the DAC and the bottom plate parasitic capacitance, α_P. Although the DAC energy increases as the top plate parasitic capacitance, α_T, increases as well, the increase in energy associated with α_T is a much weaker function than the signal-to-noise ratio or the bottom plate parasitic, α_P, and the increase in energy eventually approaches an asymptotic limit.

III. Comparator Energy Model

In this section, we derive an expression for the minimum energy consumption of a regenerative comparator. The goal of this derivation is to estimate the comparator energy consumption in a general manner such that the final expression does not depend on technology parameters such as threshold voltage, transition frequency, transconductance, etc. We estimate the lower bound of the

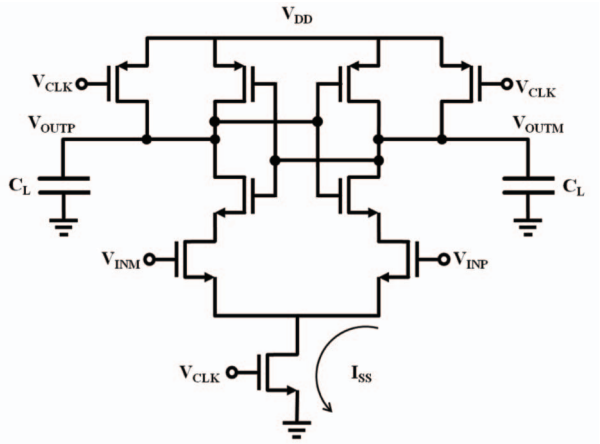

Figure 7: Simplified dynamic comparator from [14]. The key features of this comparator are a latched output and clocked reset.

comparator energy consumption in terms of the ADC bit resolution and the comparator input referred noise.

Fig. 7 shows a general comparator schematic that we use as a starting point for this analysis. Although the comparator is a simplified version of the dynamic comparator [14], the particular circuit topology is not important. For our purposes, the key features of this comparator are a capacitive load, a clocked reset, and a latching output. The comparator has two distinct phases of operation: a reset phase and an amplification stage. In the reset phase, the load capacitors are pre-charged to V_{DD}, and in the amplification phase, the input voltage difference is amplified by the positive feedback latching structure. During each of these operations, charge is transferred from the supply to the load capacitors. By estimating the energy consumption of these charge transfers, we estimate the overall energy consumption of the comparator.

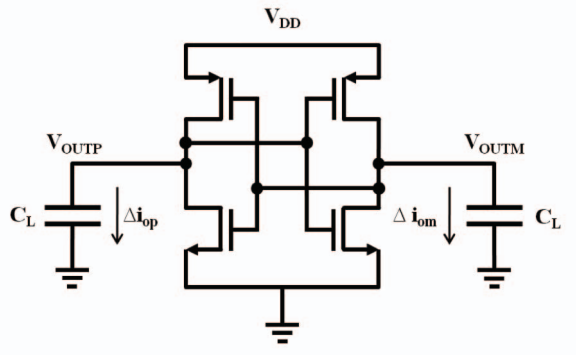

Figure 8: Simplified model of the comparator during the amplification phase. Assuming the latch outputs are initially balanced at $V_{DD}/2$, Δi_{OP} and Δi_{OM} describe the initial conditions generated from the input voltage.

We first calculate the energy associated with the reset phase. At the beginning of the reset phase, we assume that one of the output capacitors is fully charged to V_{DD} and other is completely discharged. Therefore, during reset, charge is only transferred to one capacitor. The energy consumed by the supply during this charging process is shown by (13).

$$\Delta E_{RESET} = C_L V_{DD}^{\ 2} \tag{13}$$

Next, we calculate the energy consumed during the amplification phase. Since the positive feedback latch structure at the output dominates the comparator behavior during amplification, we simplify the energy calculation by estimating only the energy consumption of a latch.

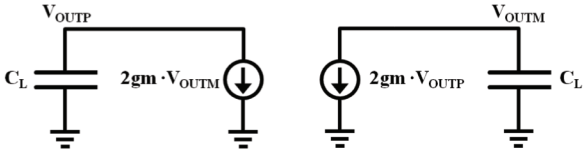

Figure 9: Small signal model of the latch. For simplicity output resistances are neglected and all transconductances are assumed equal.

The energy consumed by the latch is described by (14) – where $I_{DD,MAX}$ is the peak supply current and Δt is time interval of the latching operation.

$$\Delta E_{LATCH} \le I_{DD,MAX} V_{DD} \Delta t \tag{14}$$

When the latch outputs in are held at mid-rail, the overdrive voltages of the internal gates are largest and $I_{DD,MAX}$ is sourced from the supply. Summing the currents flowing through the top devices at this bias point, we approximate the peak supply as shown in (15) – where V_{GS} is approximated as $V_{DD}/2$ and we simply neglect the threshold voltage, V_{TH}.

$$I_{DD,MAX} \cong gm\left|V_{GS} - V_{TH}\right| < \tfrac{1}{2} gm V_{DD} \tag{15}$$

To estimate the time interval over which latching occurs, we derive a time domain expressions for the latch output and calculate the time until the outputs saturate. Applying KCL to the small signal model we derive the coupled system of differential equations shown in ((16).

$$\begin{aligned} \dot{V}_{OUTP} + \tfrac{2gm}{C_L} V_{OUTM} &= 0 \\ \dot{V}_{OUTM} + \tfrac{2gm}{C_L} V_{OUTP} &= 0 \end{aligned} \tag{16}$$

After some work, we obtain an expression for the differential output (17):

$$\Delta V_{OUT} = \tfrac{1}{2}\sinh\left[\frac{2gm}{C_L}t\right]\Delta V_{IN} \quad (17)$$

Since the latch saturates when the differential output voltage equals to $\pm V_{DD,}$ we set the output voltage in (17) to V_{DD} and solve for the latching time Δt as described in (18):

$$\Delta t = \frac{C_L}{2gm}\operatorname{arcsinh}\left[\frac{2V_{DD}}{\Delta V_{IN}}\right] \quad (18)$$

Finally, we obtain an estimate of the latch energy consumption by substituting both the latching time interval (18) and the $I_{DD,MAX}$ expression from (15) into the energy expression (14). Equation (19) describes the latch energy consumption as function of the comparator input voltage magnitude.

$$\Delta E_{LATCH}(\Delta V_{IN}) = \tfrac{1}{4}C_L V_{DD}{}^2 \operatorname{arcsinh}\left[\frac{2V_{DD}}{\Delta V_{IN}}\right] \quad (19)$$

Assuming the magnitude of input signal to the latch is uniformly distributed between 0 and $V_{DD}/2^m$ – where m defines some arbitrary binary weighted scaling factor, we calculate the average energy consumption as a function of m by averaging (19) across the input signal range as shown in (20). During a complete SAR conversion cycle, the magnitude of the comparator input range is halved after each comparison. Therefore, the input range is defined using 2^m in order to accommodate the binary scaling of the input signal magnitude during a conversion cycle.

$$\Delta E_{LATCH}(m) = \frac{2^m C_L V_{DD}}{4}\int_0^{2^{-m}V_{DD}} \operatorname{arcsinh}\left[\frac{2V_{DD}}{\Delta V_{IN}}\right] d\Delta V_{IN} \quad (20)$$

The integral in (20) is easier to compute numerically than to solve explicitly; therefore, we substitute the unitless parameter u for the argument of the *arcsinh* in the integrand. To calculate the average latch energy consumed after N comparisons, we sum the energy contributions across the binary scaling parameter m from 0 to N-1 as shown in (21).

$$\Delta E_{LATCH} = \frac{C_L V_{DD}{}^2}{4}\sum_{m=0}^{N-1} 2^m \int_0^{2^{-m}} \operatorname{arcsinh}\tfrac{2}{u}\,du \quad (21)$$

When deriving the latch energy expression in (21), we assumed that the latch was initially biased at mid-rail. During a comparison, however, the output voltages must discharge from the V_{DD} reset value to the latch common mode voltage before the positive feedback amplification can occur. As the current ramps up from zero to $I_{DD,MAX}$, this discharging process will consume energy.

If we consider the summation term in (21) as a measure of how efficiently the latch transfers charge to the load capacitance during transitions from the peak supply current down to zero current, we can approximate the energy efficiency of this initial discharging process during a transition from zero current to peak supply current as roughly equal to (21). Therefore the total energy consumed by the comparator after N comparisons is approximately the sum of N reset energy contributions (13) and twice the latch energy contribution form (21). Equation (22) describes the total energy consumption of the comparator.

$$\Delta E_{COMP} = \Gamma_N \cdot C_L V_{DD}{}^2$$
$$\Gamma_N = N + \tfrac{1}{2}\sum_{m=0}^{N-1} 2^m \int_0^{2^{-m}} \operatorname{arcsinh}\tfrac{2}{u}\,du \quad (22)$$

The Γ_N scaling parameter from (22) includes a complicated integral. Although an analytical solution exists for this integral, a simpler approximation is easier to manipulate and interpret. Equation (23) presents a quadratic approximation using the coefficients for a least-squares fit rounded to convenient fractions.

$$\Gamma_N \cong \tfrac{4}{23}\left[N^2 + 12N + 2\right] \quad (23)$$

Lastly, we remove the C_L dependency from (22) by relating C_L to input referred noise of the comparator. A comprehensive transient, noise analysis of the dynamic comparator can be found in [14], which describes the input referred comparator as scaled kT/C noise. Although less accurate than [14], we will approximate the input-referred noise as the simply the sum of the two kT/C noise powers contributed from each latch output. An estimate for the input referred comparator noise normalized to LSB^2 is shown in (24) – where σ_{COMP} is in bits, N is the resolution, and the differential input range, V_{FS}, is approximated as $2V_{DD}$.

$$\sigma_{COMP}{}^2 \le \frac{2kT}{C_L}\left[\frac{2^N}{2V_{DD}}\right]^2 \quad (24)$$

Substituting the input referred noise expression and the numeric approximation (23) into (22), the comparator energy is expressed as a function of the ADC resolution and the comparator input referred noise.

$$\Delta E_{COMP} \cong \frac{2kT}{23}\left[\frac{2^N}{\sigma_{COMP}}\right]^2\left[N^2 + 12N + 2\right] \quad (25)$$

Equation (25) describes the energy consumed by the comparator as a function of the ADC resolution and the input referred comparator noise. Similar to the derivation in the DAC energy section, we can relate 2^N and σ_{COMP} to the available signal-to-noise ratio from the comparator and express (25) in the more convenient form given by (26)

$$\Delta E_{COMP} \cong \frac{2kT}{3}\cdot SNR_{COMP} \cdot \left[N^2 + 12N + 2\right] \quad (26)$$

As shown in (26), the energy required to operate the comparator across all bit trials is linearly dependent on the

available signal-to-noise ratio of the comparator and is a quadratic function of the resolution, N, as expressed in bits. The linear dependence between the comparator energy and the available signal-to-noise ratio from the comparator derives, to the first order, from the load capacitance, C_L.

IV. Yield and Capacitor Matching

In practice, an ADC designer needs to target a particular ENOB specification, but when estimating the yield, only indirect metrics such as integral nonlinearity (INL) or differential nonlinearity (DNL) are available. Although ENOB, INL, and DNL are important indicators of ADC performance, ENOB is a better indicator of the *overall* system level performance, and with the yield expressions derived in this paper, ADC designers can easily target system level performance objectives.

In [11] we examine the effects of mismatch in a binary weighted, charge redistribution SAR ADC and then derive an exact algebraic formulation relating capacitor mismatch to the average noise power of the ADC output. From this algebraic formulation, we derive ENOB as a function of capacitor mismatch. Using this we explore the statistics of this ENOB expression and develop a statistical expression that predicts yield in terms of ENOB and mismatch. Finally, we generalize the results of this work by presenting a compact design equation, which accurately relates resolution, mismatch, and ENOB to yield for all binary weighted ratiometric converters. The design equation offered is accurate to within ±0.17 bits for yield values between 0.5% and 99.5% and is consistent with standard test methodology.

A complete formulation of our simplified yield approximation is given in (27) – where $ENOB_{MIN}$ is the minimum desired ENOB, N is the resolution in bits, σ_c/C_{nom} is the standard deviation of the fractional mismatch, $F_Z(z)$ is the CDF of Z (both the expressions for $F_Z(z)$ and its inverse are standard functions in most commercial math programs), Γ is the Gamma function, and both k and b are empirical fitting parameters.

$$
\begin{aligned}
&\mathrm{P}(ENOB > ENOB_{MIN}) = \mathrm{P}(X < 4^{N-ENOB_{MIN}} - 1) \\
&Z = X \cdot 2^{-N} \left[\frac{C_{nom}}{\sigma_c}\right]^2 \\
&\mathrm{F}_Z(z) = \frac{1}{\Gamma(k)} \int_0^{b\sqrt{z}} t^{k-1} e^{-t} dt \\
&k = 7.944 \quad b = 13.146
\end{aligned}
\tag{27}
$$

```
% Parameter Values
N = 9;  SIGMA = 0.1;  ENOB_MIN = 7.7;
YIELD = 0.95;  k = 7.944;  b = 13.146;

% Yield Calculation
X=4^(N-ENOB_MIN)-1;
Z=X/2^N/SIGMA^2;
YIELD=gammainc(b*sqrt(Z),k)

% Sigma Calculation
X=4^(N-ENOB_MIN)-1;
Z=(gammaincinv(YIELD,k)/b)^2;
SIMGA=sqrt(X/Z/2^N)
```

Figure 9: Example MATLAB® code for implementing the yield equation provided in (27). This code calculates the yield as function of resolution and mismatch and calculates mismatch as a function of yield and resolution.

Equation (27) relates yield, mismatch, ENOB, and resolution in a single closed form expression.

For simplicity, we offer MATLAB® code in Fig. 9. This code calculates the yield as function of resolution and mismatch and calculates mismatch as a function of yield and resolution as an example of how to interpret (27) – where we have implemented $F_Z(z)$ using the standard function provided by the software. When this code is executed, the yield calculation will return 95% for YIELD and the sigma calculation will return 0.1 for SIGMA. We omit the resolution calculation, but this calculation is easily derived from the sigma calculation by rearranging the terms.

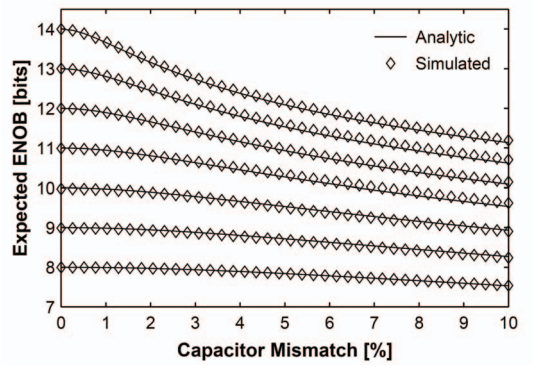

Figure 10: Comparison between simulated and calculated expected values for ENOB across various resolutions. The numerical simulation results are obtained using a 1024 point FFT of 300,000 randomly mismatched ADCs at each resolution and each standard deviation of capacitor mismatch.

V. Conclusions

The last two decades have seen dramatic improvements in the speed and the energy efficiency of ADCs. SAR ADCs are particularly well suited to take advantage of process scaling. The SAR assisted pipeline architecture makes the SAR structure useful for higher resolution conversion. The combination of ring amplifiers with the SAR assisted pipeline architecture is especially attractive for advanced processes. Noise shaping promises to further extend the performance space of SAR ADCs. This paper gives a detailed analysis of the energy consumption of the SAR capacitor DAC and comparator in terms of the resolution and bandwidth constraints. It also examines the effects of capacitor mismatch on ADC resolution and yield.

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