A 192MHz Differential XO Based Frequency Quadrupler with Sub-Picosecond Jitter in 28nm CMOS

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***Abstract*—A low jitter 192MHz crystal reference quadrupler leverages a new active inductor based 48MHz differential XO, two skewed inverters, a new duty cycle correction circuit, and a frequency doubler. The 192MHz quadrupler can serve as a fast, low jitter reference for a low phase noise PLL and requires far less power and area than reference multiplying PLL or MDLL circuits. The measured RMS jitter is 168fs for the XO, and 184fs for 96MHz output (192MHz divide by 2). The entire circuit, including the XO, draws 5.5mA from a 1V supply and occupies 0.045mm^2. To our best knowledge, this is the first reference frequency quadrupler with sub-picosecond jitter.**

***Index Terms*—Oscillators, phase noise, jitter.**

I. Introduction

High performance frequency synthesizers often use a multiple of the Crystal Oscillator (XO) frequency as a reference input to meet stringent phase noise requirements [1-3]. A high reference frequency reduces the fractional-*N* modulator quantization noise. Because high frequency crystal oscillators are expensive, it is preferable to more than double the XO frequency. However, the use of multiple frequency doublers in series is best avoided due to high jitter. For example, when two frequency doublers are used in series, both the rising and falling edges are corrupted by long delays and therefore have high jitter.

In LO frequency synthesizers with GHz range outputs, an injection locked integer-*N* PLL or MDLL reference multiplier is cascaded with an LC fractional-*N* PLL to achieve low phase noise [3]. Nevertheless, the power consumption and area of these reference multipliers is high because of the complexity needed for PVT insensitive reference injection, to achieve low jitter and spurs [3], [4]. Although the injection locked fractional-*N* MDLL in [5] has a 1.5GHz output, the use of a ring VCO means that the far offset phase noise is much worse than when a reference multiplier is cascaded with an LC PLL.

We introduce a new low power, compact differential XO that achieves a measured RMS jitter of 168fs. We also propose a new method to multiply the XO frequency by four with less than half the power consumption and less than a quarter of the area of conventional methods. This 192MHz quadrupler circuit achieves low edge jitter making it an ideal fast reference for low noise synthesizers.

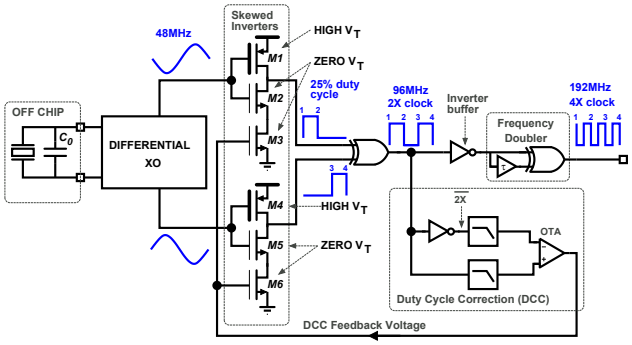

Fig. 1. New differential XO based frequency quadrupler (F4Xer)

II. Frequency Quadrupler Operation

Fig. 1 shows the new differential XO based Frequency Quadrupler (F4Xer). A new active inductor based XO generates a 48MHz differential sinusoid. This work uses the differential XO outputs in a unique way to double the frequency. The differential XO outputs are fed to two skewed inverters, with thresholds adjusted by Duty Cycle Correction (DCC) feedback, to produce two 25% duty cycle 48MHz square waves (i.e., at the XO frequency). The two 25% duty cycle clocks are XORed to form a 50% duty cycle, 96MHz, 2X clock (i.e., double the XO frequency). Both the rising and falling edges of the 2X clock have low jitter since they are directly generated from the XO outputs. It is important to note that this is unlike a standard frequency doubler where one edge per cycle is corrupted by a long delay. After an inverter buffer, a conventional XOR-plus-delay based frequency doubler generates a 192MHz, 4X clock. As seen in Fig. 1, the 4X clock has one low jitter edge per cycle (directly from XO). Therefore, the 192MHz, 4X clock can serve as a clean reference in any edge-triggered system such as a PFD or PD based PLL or DLL.

III. Differential Crystal Oscillator

Fig. 2 shows the new differential XO circuit. Compared to single-ended XOs, differential XOs have several advantages such as reduced spurs and better PSR [6]. A differential cross-coupled oscillator circuit cannot be used because when a crystal replaces the LC tank, the circuit latches up due to the lack of a low impedance DC path.

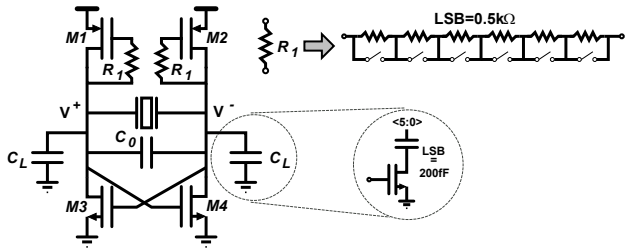

Fig. 2. New active inductor based differential XO schematic

The differential XO in [6] solves this latch-up problem by AC coupling the cross-coupled transistors. However, this method is susceptible to noise injection since a separate DC voltage biases the cross coupled pair in the XO core. Furthermore, it requires a large die area to reduce the noise of this on-chip DC bias voltage.

Instead, we introduce a low power, compact active inductor to provide a low impedance DC path and prevent latch up. Two single ended active inductors are formed by placing a resistor, R_1, between the gate and drain of diode-connected transistors, M1 and M2. Cross-coupled transistors, M3 and M4, provide negative resistance to sustain XO oscillation. C_L, a programmable 6-bit binary capacitor bank with an LSB of 200fF, is placed on both sides of the XO for fine tuning. C_0 is a 10pF off chip capacitor for XO coarse tuning. Resistor R_1, used in the active inductor, is a programmable 6 bit binary weighted resistor with an LSB of 0.5kΩ.

IV. Duty Cycle Correction Operation

Two offset 25% duty cycle clocks at the XO frequency are XORed to form the 50% duty cycle 2X clock. The duty cycle of this 96MHz, 2X clock must be 50% as both its rising and falling edges are used to generate the clean edges of the 192MHz, 4X clock (Fig. 1). The new DCC circuit ensures the generation of the 25% duty cycle 1X clocks so that when these are combined, the duty cycle of the 96MHz, 2X clock is 50%. The DCC feedback loop forces the average (i.e., DC component) of the 96MHz, 2X clock and its inverse, $\overline{2X}$ (formed by an extra inverter) to be the same to achieve a 50% duty cycle. Two *RC* LP filters extract the DC of 2X and $\overline{2X}$ clocks. The DCC uses a folded cascode OTA as an error amplifier to generate a feedback voltage based on DC values of 2X and $\overline{2X}$. This feedback voltage sets the switching thresholds of the skewed inverters so that the duty cycle of both 1X clocks is 25%. The switching threshold is set by applying the DCC feedback voltage to the gates of zero V_T NMOS transistors, M3 and M6, at the bottom of the skewed inverters. The *RC* LP filters set the dominant pole of the DCC loop in the kHz range for easy stability.

This differential method of duty cycle correction, based on comparing DC values, does not require a precise bias voltage and is insensitive to PVT. The switching threshold of each skewed inverter is set below $V_{DD}/2$ by using high V_T PMOS transistors, M1 and M4, and zero V_T NMOS transistors, M2 and M5 (Fig. 1). The skewed inverters are sized large to reduce noise. The large size, in addition to a symmetric layout, yields good matching. The input stage of OTA is sized large to reduce the DC offset which manifests itself as a static duty cycle error. The DCC operation is unaffected by the extra inverter delay in the $\overline{2X}$ path since the DC value of $\overline{2X}$ remains unchanged.

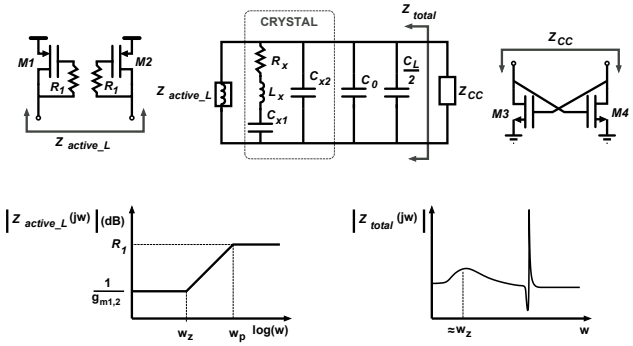

Fig. 3. Differential XO small signal model, magnitude of active inductor impedance (Z_{active_L}), and combined impedance (Z_{total})

V. XO Design Considerations

Fig. 3 shows a small signal model of the differential XO. The crystal is modelled as a series *RLC* network with motion inductance L_x, motion capacitance C_{x1}, and equivalent series resistance R_x, in shunt with parasitic capacitance C_{x2}. $C_L/2$ is the equivalent series combination of on-chip fine tune capacitors. The impedance of the cross coupled pair, Z_{CC}, is $-2/g_{m3,4}$ at low frequency. The active inductor small signal impedance, Z_{active_L}, has a zero at $\omega_z=1/R_1C_{gs1,2}$ and a pole at $\omega_p=g_{m1,2}/C_{gs1,2}$. Z_{total} is the combined impedance of crystal and active inductor.

As shown in the magnitude plot of Z_{active_L} vs frequency in Fig. 3, the low frequency impedance of the active inductor is $1/g_{m1,2}$ and the high frequency impedance is R_1. M1 and M2 are sized large to achieve low impedance at DC to avoid latch up (i.e., DC loop gain less than 1). The active inductor impedance increases with frequency, and this affects the total impedance as shown in the plot of Z_{total} in Fig. 3. The R_1 value of the active inductor is judiciously chosen to 1) avoid crystal loading at oscillation frequency and 2) set ω_z to prevent oscillation at any frequency other than crystal's high Q, parallel resonance frequency (i.e., avoids large loop gain at any frequency other than crystal's oscillation frequency).

VI. Measurement Results

Fig. 4 shows the measured phase noise of the 48MHz differential XO signal using an Agilent 5052B signal

TABLE I
DIFFERENTIAL XO SUMMARY AND COMPARISON

Parameter	**This Work**	JSSC'12 [6]	RFIC'10 [8]
Differential?	**Yes**	Yes	No
CMOS tech.	**28nm**	65nm	65nm
Power (mW)	**1.5**	2.16	7
Supply voltage (V)	**1**	1.8	1.4
Active area (mm^2)	**0.0133**	0.15†	0.09
Crystal freq. (MHz)	**48**	26	38.4
Phase noise* (dBc/Hz) 10kHz offset	**-147.7**	-146.4	-144
Phase noise* (dBc/Hz) 100kHz offset	**-155.8**	-150.7	-
Phase noise* (dBc/Hz) 1MHz offset	**-158.5**	-151.3	-
RMS jitter (fs) 10kHz-10MHz BW	**168**	420‡	-
Tuning range (ppm)	**±35**	±45	280
Avg. tuning step (ppm)	**1**	0.005	0.002

*All referred to 48MHz for fair comparison
†Includes coarse tuning capacitors
‡10kHz to 5MHz integration bandwidth

analyzer. The RMS jitter, measured over an integration bandwidth from 10kHz to 10MHz, is only 168.1fs. The measured phase noise is -147.7dBc/Hz, -155.8dBc/Hz, and -158.5dBc/Hz at 10kHz, 100kHz, and 1MHz offsets, respectively. Fig. 5 shows the measured phase noise of 96MHz clock (the input to final doubler). The measured RMS jitter is 183.6fs. The phase noise of the 192MHz, 4X clock cannot be directly measured using a signal source analyser because one edge per cycle is noisy due to the delay in final doubler [3] (most clock inputs are edge-triggered and require one low jitter edge). The last stage XOR-plus-delay based frequency doubler adds little phase noise [7] since the low jitter edges of the 192MHz, 4X clock are merely buffered versions of the rail-to-rail 96MHz, 2X clock edges which have low measured phase noise. Fig. 6 shows a scope capture of the differential waveforms at the XO I/O pins, measured with an active probe. Fig. 7 shows a scope capture of the 96MHz, 2X clock with a measured duty cycle of 50% with DCC enabled. Fig. 8 captures the 192MHz, 4X clock that is generated from the 96MHz, 50% duty cycle 2X clock. The rising and falling edges of 2X clock are used to generate a 192MHz, 4X clock with clean falling edges. Fig. 9 compares the F4Xer FoM vs area. Fig. 10 shows the die photo. The entire circuit, including the XO, occupies an active area of 0.045mm^2. Table I summarizes the performance of differential XO and compares with recent work. Table II outlines the F4Xer measured results.

VII. CONCLUSION

We present a new low power, low jitter, compact 192MHz reference frequency quadrupler that leverages a new low phase noise, active inductor based 48MHz differential XO. This 192MHz clock is ideal as a clean reference for a low phase noise PLL. It needs significantly less power and area compared to conventional methods.

TABLE II
FREQUENCY QUADRUPLER RESULTS SUMMARY

Technology	28nm CMOS	
Total power (mW)	5.5	
Supply voltage (V)	1	
Current (mA)	Total XO F4Xer	5.5 1.5 4
Active area (mm^2)	Total XO F4Xer	0.045 0.013 0.032
Phase noise (dBc/Hz)†	10kHz 100kHz 1MHz	-139.8 -148.3 -151.9
RMS jitter†(fs)	183.6	
96MHz 2X clock duty cycle(%)	50	

†Measured @ 96MHz (quadrupler divide by 2)

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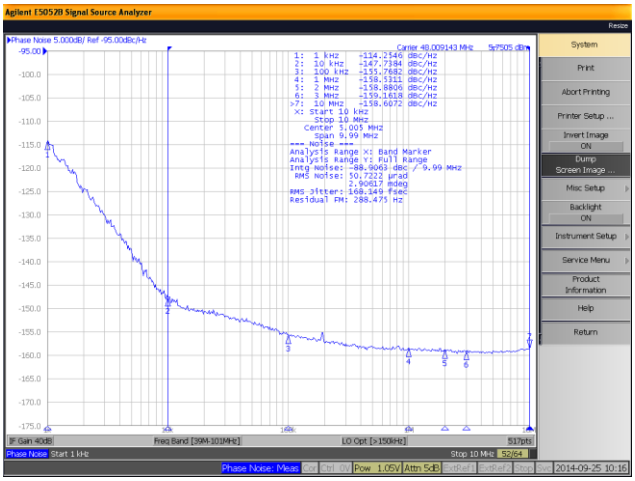

Fig. 4. Measured phase noise of the new active inductor based 48MHz differential XO using 5052B signal source analyzer

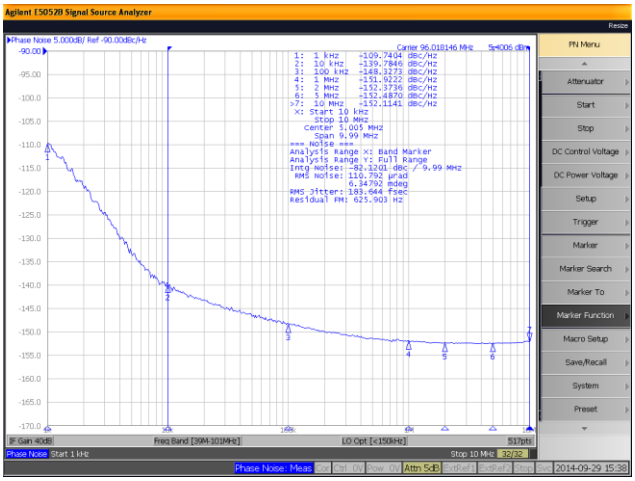

Fig. 5. Measured phase noise of 96MHz clock (double of XO and input to final doubler) using 5052B signal source analyzer

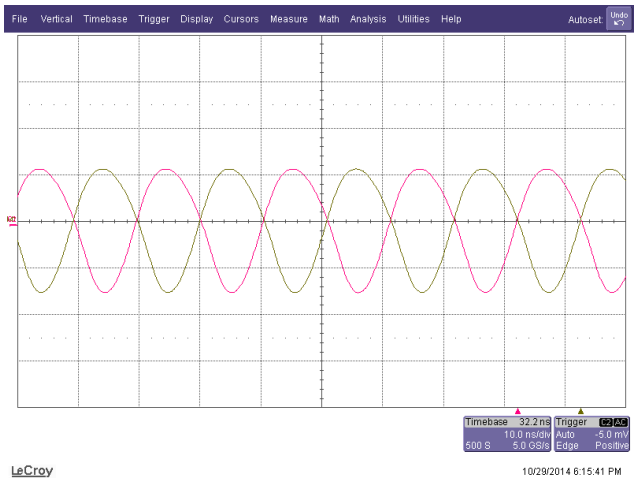

Fig. 6. Measured 48MHz differential XO waveform probed at XO I/O pins

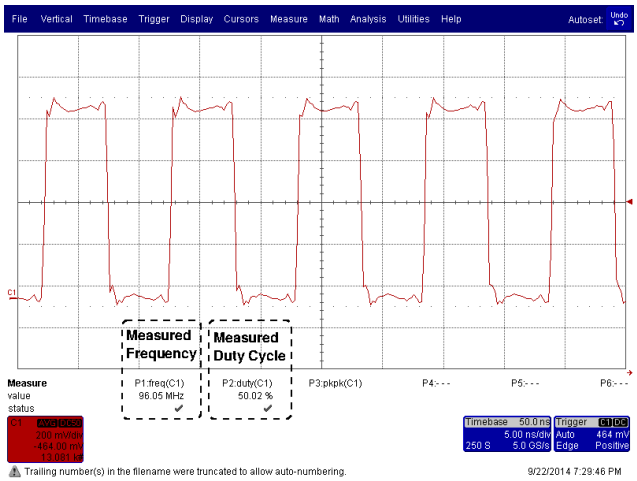

Fig. 7. Measured 96MHz, 50% duty cycle 2X clock with DCC enabled

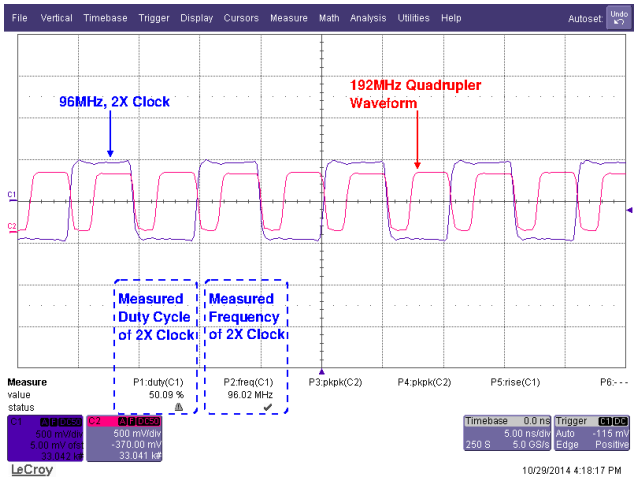

Fig. 8. Measured 192MHz quadrupler waveform (red) generated from the 50% duty cycle 96MHz, 2X clock (blue)

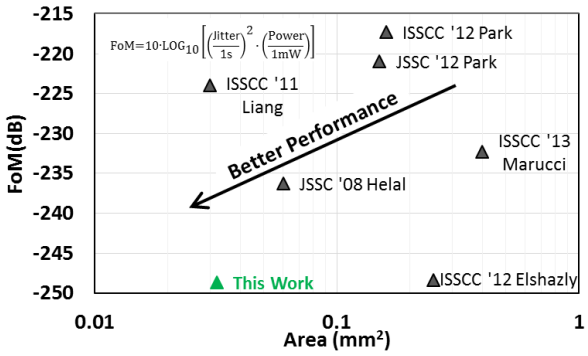

Fig. 9. Frequency quadrupler FoM vs active area comparison

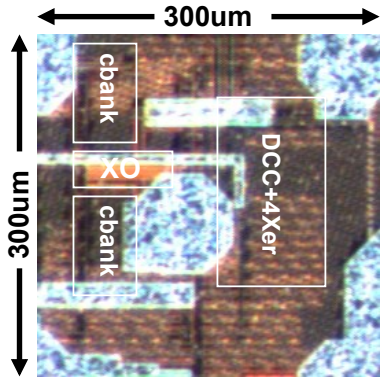

Fig. 10. Die photo including 50Ω o/p buffers, ESD, and bypass caps. The XO and F4Xer total active area is 0.045mm^2

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