26.1 A 1mW 71.5dB SNDR 50MS/s 13b Fully Differential Ring-Amplifier-Based SAR-Assisted Pipeline ADC

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The SAR-assisted pipeline ADC is an energy-efficient architecture for high resolution [1]. Consisting of two low-resolution charge-redistribution SAR ADCs coupled by a residue amplifier, a SAR-assisted pipeline ADC relaxes the noise requirements of the second stage and enhances the overall ADC speed while maintaining excellent power efficiency [1-4]. However, designs reported in [1,2] rely on power-hungry telescopic amplifiers that also limit the available inter-stage residue gain due to low output swing. A lower-power alternative is a dynamic amplifier, which operates as an open-loop time-domain integrator [3,4]. Although time-domain integration provides the benefit of noise filtering, the calibration required to achieve an accurate residue gain increases design complexity and test cost, and limits robustness. We introduce an uncalibrated fully differential ring-amplifier-based 13b 50MS/s rail-to-rail input swing SAR-assisted pipeline ADC with Walden and Schreier (SNDR) FoMs of 6.9fJ/conversion-step and 174.9dB, respectively. We also present an improved DAC switching technique that further reduces the first DAC energy consumption and also reduces the DAC errors.

The ADC (Fig. 26.1.1) comprises a 6b 1st-stage SAR ADC, a 32× residue gain stage, and an 8b 2nd-stage SAR ADC. With 1b of stage redundancy, the ADC resolves 13b after digital correction. The 1st-stage DAC is divided into two separate arrays to reduce both the DAC switching energy (a similar technique was independently developed in [5]) and the INL/DNL due to the first DAC mismatch. Although the input sampling requires 13b kT/C noise, the 1st-stage SAR DAC only requires 6b kT/C noise, therefore, we reduce the DAC switching energy by using only a quarter of the total 2pF DAC capacitance. This smaller 1st-stage DAC (*small* DAC) is configured as a 6b SAR ADC using merged capacitor switching (MCS) [6] with bottom plate sampling. The remaining three-quarters of the DAC (*big* DAC) samples the same input, but generates a residue based on the small DAC SAR result with an energy-efficient technique, derived from [7]. After the 1st-stage conversion, the residues of the big and small DACs are merged to meet the 13b kT/C noise requirement and amplified using an auto-zeroed ring amplifier based SC amplifier. The 1b redundancy corrects mismatch between the overall DAC and the small DAC SAR ADC.

We fully utilize the output swing of the ring amplifier and facilitate digital correction by auto-zeroing. C_{AZ} (Fig. 26.1.1) samples the offset of the ring amplifier during the 1st-stage sampling. A relatively big C_{AZ} value (4pF) reduces noise folding of the auto-zero. However, the use of a big C_{AZ} capacitance does not increase power consumption because the sampled voltage on C_{AZ} stays constant. The ring amplifier is turned off during the 1st-stage SAR decision to further reduce the power consumption. The amplified residue is quantized by an 8b 2nd-stage SAR ADC that also uses MCS and bottom plate sampling. The second DAC is reset after the 8b decision so that residue amplification always starts from the common mode (V_{CM}), thereby halving the maximum slew rate required of the ring amplifier. The clocks for the both SAR ADCs are generated asynchronously. The ADC requires one reference voltage V_{CM} since it uses a full residue gain (32×), and both of the SAR ADCs support a rail-to-rail input.

We introduce a fully differential ring amplifier (Fig. 26.1.2) to solve the problems of even-order distortion as well as limited common-mode and supply rejection in existing ring amplifiers. A ring amplifier [8,9] is an energy-efficient and wide-swing alternative to an OTA for SC circuits. The ring amplifier is essentially a 3-inverter amplifier that is stabilized in feedback by operating the last stage in the sub-threshold region as the output nears the desired settling point, thereby forming a dominant pole thanks to the high output resistance in sub-threshold operation. Our fully differential ring amplifier replaces the 1st-stage of the self-biased ring amplifier [9] with a differential pair. To reduce noise, it uses both PMOS and NMOS input devices to maximize g_m for a given bias current. A PMOS triode CMFB sets the common mode of the 1st-stage. A separate SC CMFB sets the output common mode to V_{CM} during the residue amplification. The resistors R_B in the 2nd-stage dynamically bias the 3rd-stage in sub-threshold. The 2nd-stage uses high V_{TH} devices to increase gain by extending the saturated operating region of its output swing. The simulated small-signal ring amplifier gain is >80dB over an output swing from 0.1 to 1.1V. The wide output swing enables the full residue gain (32×), unlike the case with [1-4].

A floated detect-and-skip technique (FDAS) improves the first DAC energy efficiency. The switching energy of the big DAC can be greatly reduced with the detect-and-skip (DAS) algorithm [7], which only switches the big DAC capacitors in one direction (or skips switching), based on the small DAC SAR decision. However in [7], aligned switching (AS), which sets the big DAC switches after the small DAC SAR is completely finished, requires additional settling time. Instead of using DAS and AS together, we introduce FDAS (Fig. 26.1.3), which sets the big DAC switches immediately after each small DAC SAR bit decision while undecided capacitors are floated to save switching energy. The MSB of the small DAC first decides the switching direction to V_{DD} or ground (GND). Then we successively connect the switches to the decided direction or V_{CM} depending on the SAR bit decision. The decision results are one bit shifted to left and applied directly (when MSB=1b), or inverted and applied (when MSB=0b) to the big DAC switches. The two LSBs and the dummy capacitors are switched together after the small DAC LSB decision. Although FDAS consumes slightly more switching energy (2.7%) than DAS with AS [7] (Fig. 26.1.4(a)), FDAS has the advantage of not requiring additional settling time for the big DAC; this allows us to reduce the size of the big DAC switches, which reduces the power consumption of the FDAS encoder. The first DAC switching energy is 55.2% lower than that of the MCS with the same DAC capacitor size.

The FDAS also reduces INL/DNL due to capacitance mismatch. The worst-case INL for MCS occurs when the MSB capacitor switches between V_{DD} and GND. However, for FDAS (also DAS, though not mentioned in [7]), the worst-case INL occurs when the MSB capacitor switches between GND and V_{CM}, or V_{DD} and V_{CM}. Since the voltage change is halved in FDAS, the residue voltage error is also halved. The simulation result (Fig. 26.1.4(b)) shows that the maximum RMS INL from the first DAC is reduced by 37.9%, compared with the MCS.

The ADC is implemented in 1P9M 65nm 1.2V CMOS and occupies 0.054mm^2 (Fig. 26.1.7). The SAR DACs are implemented with custom designed encapsulated MOM capacitors, laid out in common centroid. Without calibration, the measured SNDR, SNR and SFDR are 70.9dB (11.5b), 71.3dB and 84.6dB, respectively for a Nyquist input sampled at 50MS/s (Fig. 26.1.5). The measured power consumption is 1.0mW for a Nyquist input sampled at 50MS/s; this includes the clock buffer, digital correction, and the reference power. The measured DNL and INL are 0.58/-0.50 LSB and 0.96/-0.83 LSB, respectively. The ADC is robust to temperature and supply variation. Over a 100°C temperature range from -20 to 80°C, the worst-case measured SNDR is 69.7dB. SNDR varies by 0.45dB over a ring amplifier supply range from 1.15 to 1.25V. Figure 26.1.6 summarizes the performance of the ADC and compares with conventional SAR-assisted pipeline ADCs. The Walden FoM and SNDR based Schreier FoM with a Nyquist frequency input are 6.9fJ/conversion-step and 174.9dB respectively, which improves upon the numbers reported for state-of-the-art ADCs with sampling speed faster than 5MS/s [10].

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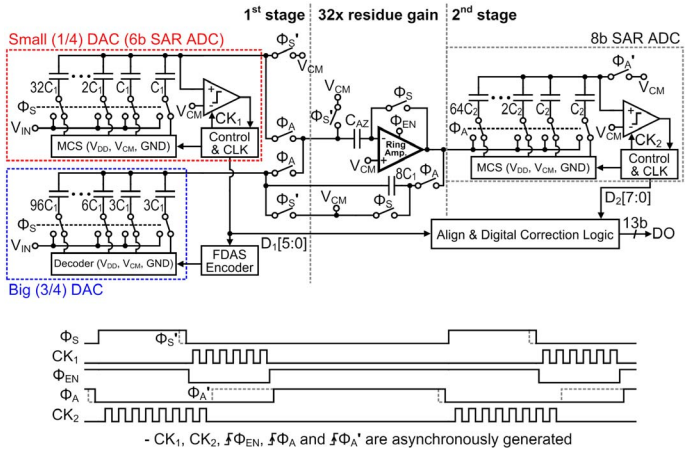

Figure 26.1.1: Block diagram and timing of the ADC (Actual implementation is fully differential).

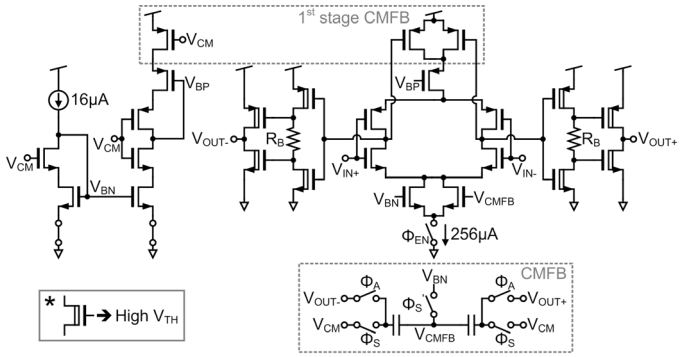

Figure 26.1.2: Fully differential ring amplifier and bias circuit.

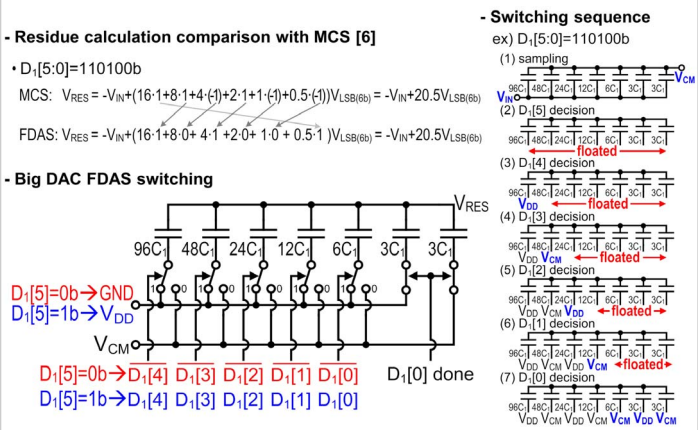

Figure 26.1.3: Floated detect-and-skip (FDAS) big (3/4) first DAC switching.

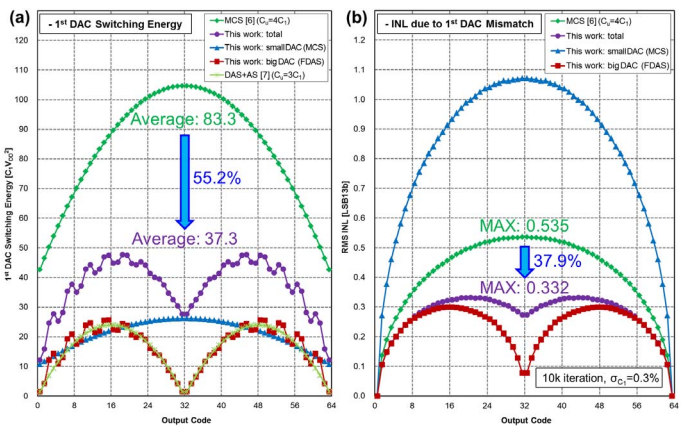

Figure 26.1.4: (a) calculated first DAC switching energy, (b) simulated INL due to first DAC mismatch.

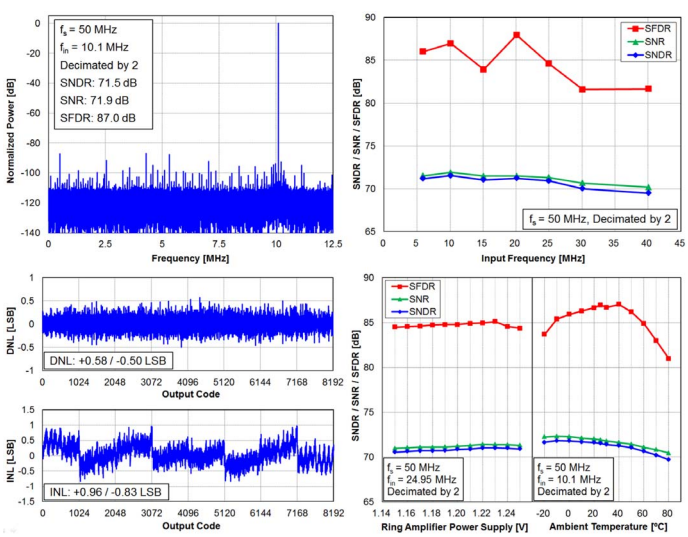

Figure 26.1.5: Measurement results.

		This Work	VLSI2010 [1]	ISSCC2012 [2]	ISSCC2014 [3]	VLSI2014 [4]
Resolution		13 bits	12 bits	14 bits	14 bits	14 bits
Analog Supply		1.2 V	1.3 V	1.2 V	1.0 V	0.9 V
Residue Amp. Structure		Fully differential ring amplifier	Double-cascoded Telescopic amplifier	Double-cascoded Telescopic amplifier	Dynamic amplifier	Dynamic amplifier
Calibration		No	No	No	Yes (gain, offset, DAC)	Yes (gain, offset, DAC)
Sampling Rate		50 MSPS	50 MSPS	30 MSPS	80 MSPS (2x interleaved)	200 MSPS (2x interleaved)
Technology		65nm CMOS	65nm CMOS	130nm CMOS	28nm CMOS	28nm CMOS
Active Area		0.054 mm²	0.16 mm²	0.24 mm²	0.137 mm²	0.35 mm²
Input Range		2.4 $V_{pk\text{-}pk}$ diff.	2 $V_{pk\text{-}pk}$ diff.	2 $V_{pk\text{-}pk}$ diff.	1.4 $V_{pk\text{-}pk}$ diff.	-
The best result	SNDR	71.5 dB	66.0 dB	70.8 dB	68.0 dB	70.0 dB
	SFDR	87.0 dB	78.0 dB	87.8 dB	80.7 dB	-
	ENOB	11.6 bits	10.7 bits	11.5 bits	11.0 bits	11.3 bits
With Nyquist freq. input	SNDR	70.9 dB	64.4 dB	70.4 dB	66.0 dB	65.0 dB
	SFDR	84.6 dB	75.0 dB	79.6 dB	74.0 dB	-
	ENOB	11.5 bits	10.4 bits	11.4 bits	10.7 bits	10.5 bits
Total Power		1.0 mW	3.5 mW	2.54 mW	1.5 mW	2.3 mW
FOMw (with the best result)		6.5 fJ/conv-step	42.9 fJ/conv-step	29.8 fJ/conv-step	9.1 fJ/conv-step	4.4 fJ/conv-step
FOMw (with Nyquist freq. input)		6.9 fJ/conv-step	51.8 fJ/conv-step	31.3 fJ/conv-step	11.5 fJ/conv-step	7.9 fJ/conv-step
FOMs (with the best result)		175.5 dB	164.5 dB	168.5 dB	172.3 dB	176.4 dB
FOMs (with Nyquist freq. input)		174.9 dB	162.9 dB	168.1 dB	170.3 dB	171.4 dB

Figure 26.1.6: Performance comparison with conventional SAR-assisted pipeline ADCs.

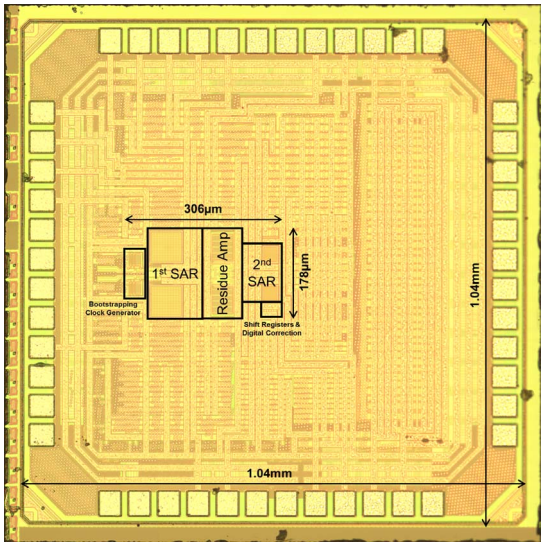

Figure 26.1.7: Die micrograph.

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