# A Low Voltage Sub 300μW 2.5GHz Current Reuse VCO

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***Abstract*-The two-transistor CMOS current reuse VCO is modified with the addition of an ac-coupling capacitor to reduce the supply voltage and achieve good phase noise with very low power consumption. A 2.17-2.9GHz prototype VCO operates with a supply voltage as low as 0.6V. At 2.53GHz, with a 0.7V supply and a 185μW power consumption, the measured phase noise at 3MHz offset is -122.6dBc/Hz and varies by only 2.2dB over a temperature range from -30 to 120°C. For a 0.85V supply, phase noise is improved to -126.1dBc/Hz with a 280μW power consumption which corresponds to a Figure of Merit (FoM) of 190.2dB. This is the lowest reported power consumption and supply voltage for any current reuse VCO. Fabricated in 65nm CMOS, the prototype occupies 0.13mm$^2$.**

## I. Introduction

Low supply voltages due to process scaling are an impediment to reducing the VCO power consumption, because they limit the choice of VCO topologies to those that do not have a high DC to RF conversion efficiency. VCO topologies such as CMOS current reuse and cross coupled CMOS have excellent DC to RF efficiencies, often a factor of two better than NMOS or PMOS only VCOs [7]. However, the standard implementation of such VCOs, where a PMOS transistor is stacked on top of an NMOS transistor, requires a supply voltage larger than the sum of the threshold voltages of the two transistors, $Vth_n+Vth_p$. In order to have reliable operation over PVT, the minimum supply voltage is more than this sum and can be as high as 1.1V in a 65nm digital CMOS process. In addition, VCOs are highly sensitive to supply noise, pushing, and pulling, and therefore a regulated voltage is always required. This further lowers the available internal voltage supply for VCOs and makes the use of CMOS VCOs operating from a low supply even more difficult.

In recent years, researchers have reported a number of VCOs using ac-coupling capacitors to achieve better phase noise and higher FoM by operating the transistors in class C regime. However, low start up gain restricts the VCO topology to NMOS or PMOS only for low voltage operation [4], or else the penalty of a high supply voltage if the more efficient CMOS topology is used [3].

This paper offers a simple technique to enable CMOS current reuse VCOs to operate at very low supply voltages by adding an ac-coupling capacitor to achieve good phase noise at low power consumption. Introduced in [6], a 1.25V two-transistor current reuse VCO uses a PMOS and an NMOS transistor to provide negative resistance to sustain oscillation in an *LC* tank. Fig. 1 shows the proposed current reuse VCO which operates with a supply voltage as low as 0.6V, which is much lower than the sum of NMOS and PMOS threshold voltages. In steady state, the operation of the VCO can be divided into two parts during each cycle: in the first half cycle, both *MN* and *MP* are on, injecting energy into the *LC* tank; and in the second half cycle, both transistors are off, and energy is dissipated through the loss of the tank.

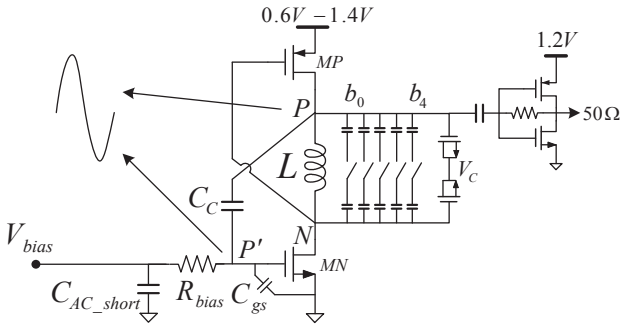



Fig. 1. The proposed ac-coupled current reuse VCO.

In the modified current reuse VCO, the voltage at node *P* is ac-coupled to gate of *MN* (node *P*′) through capacitor $C_C$. A separate DC bias is applied to the gate of *MN* through resistor $R_{bias}$ to independently set its $g_m$ to ensure start up at lower supply voltages. This enables both *MN* and *MP* to operate in saturation even at supply voltages as low as 0.6V and still provide the needed start-up gain. This in turn reduces the power consumption while enabling low phase noise operation.

Sec. II details the design methodology and Sec. III comments on practical design considerations. Implementation details and measurement results are provided in Sec. IV followed by conclusion in Sec. V.

## II. Design Methodology

The focus of this design is to minimize power consumption while meeting the phase noise requirement for a desired application at a very low voltage supply. A large inductance is desired to achieve a very low power VCO. However, the inductance cannot be arbitrarily increased as VCO phase noise is limited by *kT/C* and *Q*, where *C* is the total tank capacitance, and *Q* the quality factor of the VCO tank. For a fixed oscillation frequency and constant *Q*, as inductance is increased, total tank capacitance *C* is reduced, therefore increasing *kT/C* and degrading the phase noise. The tank quality factor of the VCO shown in Fig. 1 is given by $Q_{tank} = R_P\sqrt{C/L}$, where it is dominated by the inductance *L* and its equivalent parallel resistance $R_p$. The power consumption of

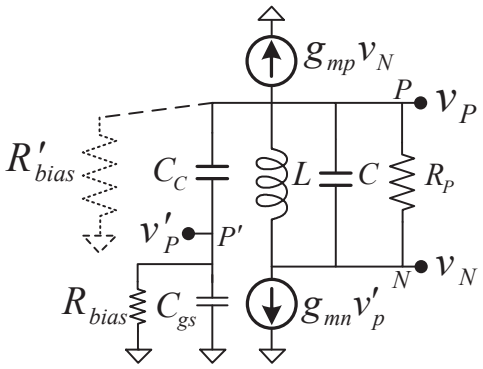



Fig. 2. Small signal model of the proposed ac-coupled VCO.

an *LC* VCO is directly proportional to $R_p$.

In a conventional current reuse VCO [6], meeting the startup condition over PVT for a supply voltage lower than 1V is very difficult. An ac-coupling capacitor, $C_C$, enables the VCO to work at much lower supply voltages because $g_{mn}$ can be independently adjusted to meet the startup condition in (1) by increasing the bias voltage $V_{bias}$. In order to operate the VCO at the lowest voltage supply, the start up gain needs to be maximized by choosing large values for $C_C$ and $R_{bias}$. This is explained by looking at the impedance $Z_p$ at node $P$ at resonance using the small signal model in Fig. 2. Impedance $Z_P$ should be negative to ensure start up so that:

$$Z_P = \left(\frac{1}{R'_{bias}} + |\alpha|g_{mn} + g_{mp} - |\alpha|g_{mn}g_{mp}R_P\right)^{-1} < 0, \quad (1)$$

where $g_{mn}$ and $g_{mp}$ are the transconductances of *MN* and *MP*, $R'_{bias}$ the equivalent resistance seen at node $P$ due to $R_{bias}$, and $\alpha = v'_p/v_P$ is the voltage divider ratio between nodes $P$ and $P'$. It is important to choose the optimum values for $C_C$ and $R_{bias}$ to have sufficient start up gain. In an ideal case $v'_p/v_P$ must be close to one. As suggested by Fig. 2, $C_C$ should be bigger than $C_{gs}$ (capacitance at node $P'$) by a large factor so to maximize the transfer function

$$\frac{v'_P}{v_P} = \alpha = \left(1 + \beta + \frac{1}{sR_{bias}C_C}\right)^{-1}, \quad (2)$$

where $\beta = C_{gs}/C_C$. Using (2), a lower bound for bias resistance $R_{bias}$ is derived as

$$R_{bias} \geq \frac{1}{C_C\omega}\left(\frac{|\alpha|}{\sqrt{1-|\alpha|^2(1+\beta)^2}}\right). \quad (3)$$

In addition, $R_{bias}$ should be large to avoid degrading the tank quality factor by reducing the impedance at node $P$. Using Fig. 2, $R'_{bias}$ at resonance is given by

$$R'_{bias} = \left(\frac{1+Q^2}{Q^2}\beta^2 + 2\beta + 1\right)R_{bias}, \quad (4)$$

where $Q = R_{bias}C_{gs}\omega$ is the quality factor of parallel combination of $C_{gs}$ and $R_{bias}$. For $\beta \ll 1$ ($C_{gs} \ll C_C$), we can assume that $R'_{bias} \approx R_{bias}$. To avoid degrading the tank $Q$ by more than 10%, $R'_{bias}$ should be approximately 10 times larger than $R_P$. This is a conservative approximation because it only considers the inductor parallel resistance $R_p$ and not the loading effect of *MN*, *MP*, and the capacitor bank. Therefore, $R_{bias} \approx 10 \cdot Rp$ is more than enough to avoid significant $Q$ degradation.

## III. Practical Design Considerations

The prototype VCO, implemented in 65nm CMOS, uses a compact 5-turn 8nH inductor with a quality factor of 11. This results in an equivalent parallel tank resistance $R_P \cong 1.4k\Omega$. Considerably higher $Q$ values can be obtained at the cost of larger inductor area, which will further improve the phase noise and lower the power consumption.

Transistors *MN* (4.8µm/80nm) and *MP* (18µm/80nm) are sized so to meet the startup condition in (1) for a voltage supply as low as 0.6V. Flicker noise upconversion is reduced by avoiding the use of minimum length transistors. Using longer transistors also improves the VCO loaded $Q$ and reduces the noise contribution of *MN* and *MP* by reducing their effective $g_{ds}$ [7]. An ac-coupling capacitor $C_C$=250fF ($\beta \approx 0.02$) is used, which is large enough to result in a voltage divide ratio $|\alpha| \approx 0.96$ from (2). From (3), a resistor bias value $R_{bias} \geq 1.4k\Omega$ is sufficient for start up; and according to (4), $R_{bias} \approx 10 \cdot R_P = 14k\Omega$ for minimum $Q$ degradation of the tank. The analysis to optimize the start up gain and minimize the tank $Q$ degradation, leads to $R_{bias}$ values ranging from 1.4kΩ to 14kΩ. However, the thermal noise of $R_{bias}$ is also important. Considering sufficient start up gain, minimal $Q$ degradation, and the thermal noise contribution of $R_{bias}$, an optimum value of 5kΩ is chosen.

## III. Implementation and Measurement

The prototype VCO (Fig. 3) is implemented in a 1P9M 65nm digital CMOS process and occupies a core area of 0.13mm$^2$. The inductor is formed with thick metal 9 and tuning is achieved with a 5-bit bank of MIM capacitors. The varactor is formed with an N-type MOS capacitor biased at 0.55V for all measurements. The simulated VCO gain is approximately 45MHz/V. The device is packaged in a 40-pin 6×6 QFN package. Phase noise is measured using an Agilent E5052B source analyzer, and current is sensed with a Keithley 2400 source meter.

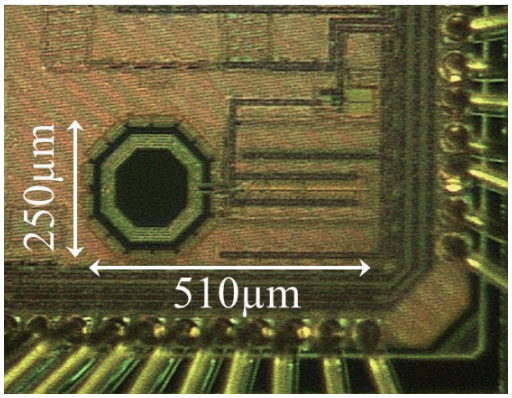
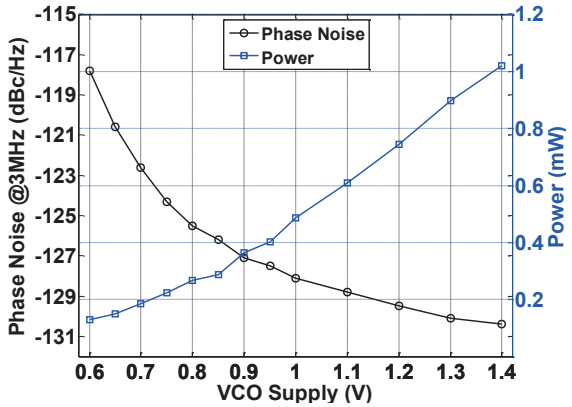
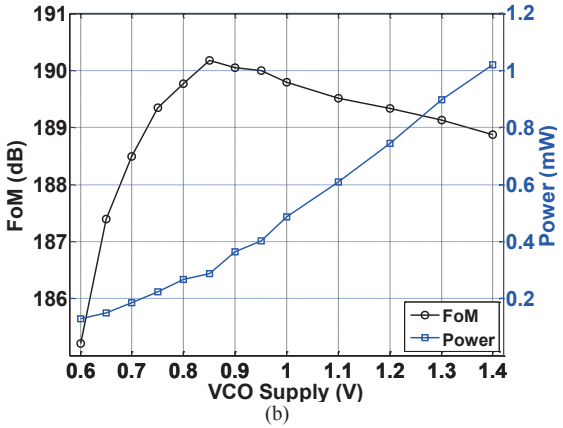



Fig. 3. Chip photo. Active area is 0.13mm$^2$.




(a)




(b)

Fig. 4. Measured VCO phase noise (a) and FoM (b) at 2.53GHz with power consumption for different supply voltages.

The measured tuning range is 2.17-2.9GHz and the VCO operates with supply voltage as low as 0.6V. Fig. 4(a) shows the measured phase noise and power consumption at 2.53GHz for different supply voltages. With a 0.7V supply, the measured VCO phase noise at a 3MHz offset is -122.6dBc/Hz with a power consumption of 185µW. For a 0.85V supply, phase noise is improved to -126.1dBc/Hz with a 288µW power consumption. For applications requiring better performance, a phase noise of -130.1dBc/Hz is achieved by increasing the supply to 1.3V with a 0.9mW power consumption.

The oscillator Figure of Merit (FoM) defined as

$$FoM = 10\log\left(\left(\frac{f_0}{\Delta f}\right)^2 \frac{1}{P}\right) - \mathcal{L}\{\Delta f\} \qquad (5)$$

is used to characterize the VCO at a frequency $f_0$, where $\mathcal{L}\{\Delta f\}$ is the phase noise at $\Delta f$ offset, and $P$, the power consumption in mW. Fig. 4(b) shows the FoM associated with phase noise measurements in Fig. 4(a). The VCO FoM is 188.5dB for supply voltage of 0.7V. At 0.85V, FoM is 190.2dB with phase noise of -126.1dBc/Hz at 3MHz consuming 280µW. This is the highest FoM reported for a current reuse VCO with power consumption below 300µW. An instrument screen shot of phase noise measurement for the peak FoM is shown in Fig. 5.

Fig. 6 shows the measured phase noise at 2.53GHz with a 0.7V supply at -30, 25 and 120°C. At 3MHz offset, worst phase noise is -120dBc/Hz at 120°C with FoM of 185dB. Phase noise variation across temperature is 2.2dB.

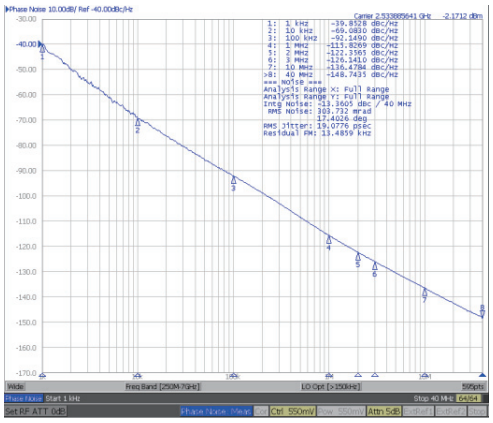


Fig. 5. Instrument screen shot of phase noise measurement with a 0.85V supply.

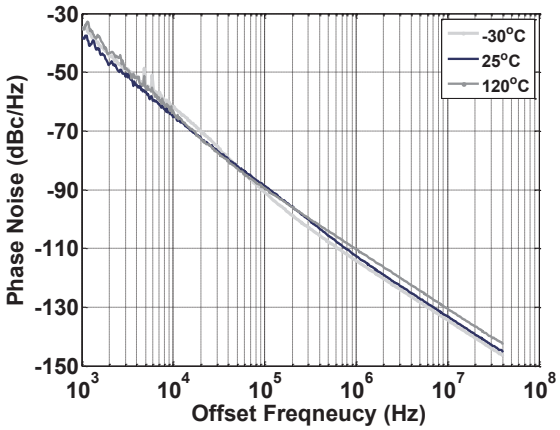



Fig. 6. Measured phase noise at 2.53GHz over temperature.

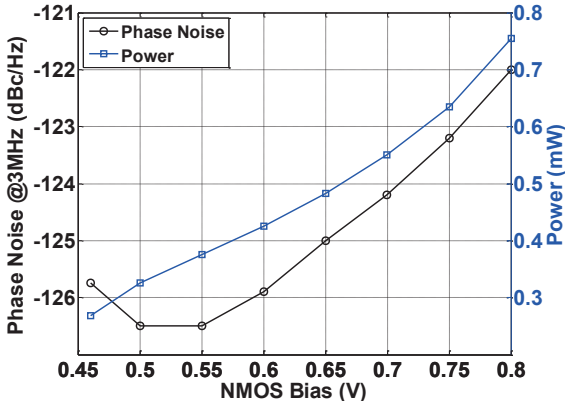



Fig. 7. Measured phase noise at 2.53GHz versus NMOS gate bias voltage with a 0.85V supply.

TABLE I
PERFORMANCE COMPARISON

| | **This Work** | [1] CICC 11 | [2] CICC 11 | [3] ISSCC 12 | [4] LMWC 11 | [5] LMWC 09 | [6] ISSCC 05 |
|---|---|---|---|---|---|---|---|
| Frequency (GHz) | **2.53** | 1.6 | 5.6 | 3.92 (7.84÷2) | 3.1 | 3[b] | 1.97 |
| Tuning Range (GHz) $F_T$ | **2.17-2.9 (29%)** | 1.35-1.75 (26%) | 5.4-5.62 (4%) | 3.25-4.5 (33%) | 2.6-3.2 (20%) | 2.93-3.62 (21%) | - |
| Phase Noise @3MHz (dBc/Hz) | **-126.1** | -130[a] | -132.3 | -132.5[a] | -121[b] | -131[a] | -125[a] |
| Supply Voltage (V) | **0.85** | 1 | 0.6 | 1.5 | 1 | 1.5 | 1.25 |
| Power (mW) | **0.28** | 2.6 | 4.2 | 6 | 0.56 | 1.7 | 1 |
| FoM (dB) | **190.2** | 180.4 | 191.5 | 185.6 | 183.8 | 188.7 | 181.3 |
| FoMT (dB) | **199.4** | 188.7 | 183.5 | 195.9 | 189.8 | 195.2 | - |
| Area ($mm^2$) | **0.13** | - | 0.48 | 0.49 | 0.77 (w/ pads) | 0.3 (w/ pads) | - |
| Technology | **65nm** | 65nm | 0.13µm | 55nm | 0.18µm | 0.18µm | 0.18µm |
| Description | **CMOS ac-coupled current reuse** | NMOS QVCO and divide by 2 | NMOS QVCO w/ capacitive coupling | NMOS/PMOS combined for constant FoM | PMOS Class C w/ start up circuit | CMOS current reuse | CMOS current reuse |

[a]Estimated form PN plot
[b]Back calculated from FoM @1MHz
$FoMT = FoM + 20\log\left(\frac{F_T}{10}\right)$

Fig. 7 shows the variation in phase noise for different $V_{bias}$ values (*MN* gate bias) along with the corresponding power consumption. The best phase noise-power tradeoff is obtained with $V_{bias}$ set to 0.5V. Increasing $V_{bias}$ beyond a certain point degrades the phase noise while increasing the power consumption as *MN* enters the triode region.

Table I summarizes the performance of the prototype VCO with comparison to some recent low power counterparts. At 0.85V, the proposed ac-coupled current reuse VCO achieves a phase noise of -126.1dBc/Hz at 3MHz offset for an oscillation frequency 2.53GHz and consumes 280µW. This corresponds to a FoM of 190.2dB which is comparable to the state of the art. Considering the 2.17-2.9GHz (29%) tuning range, the Figure of Merit with Tuning (FoMT) is 199.4dB, which is the highest, reported for any current reuse VCO.

## V. CONCLUSION

A versatile, compact, low voltage, low power 2.5GHz VCO with low phase noise is presented. A conventional CMOS current-reuse VCO is modified with the introduction of an ac-coupling capacitor to reduce the supply voltage and achieve comparable phase noise at a much lower power consumption. The 2.17-2.9GHz VCO is capable of operating with a supply voltage as low as 0.6V. With a 0.7V supply and a 185µW power consumption, the phase noise at a 3MHz offset is -122.6dBc/Hz, which is suitable for applications such as ZigBee. Increasing the supply voltage to 1.3V results in a phase noise of -130.1dBc/Hz with a 0.9mW power consumption. This phase noise meets the requirements for applications such as Bluetooth, GPS, and even some lower data rate Wi-Fi applications. At 0.85V, the VCO phase noise is -126.1dBc/Hz with a 190.2dB FoM, the highest reported for power levels as low as 280µW. This is the lowest reported power consumption and supply voltage for any current reuse VCO. Implemented in 65nm CMOS, the VCO occupies a core area of $0.13mm^2$.

## ACKNOWLEDGMENTS

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