A 9b 1GS/s 27mW Two-Stage Pipeline ADC in 45nm SOI-CMOS

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***Abstract*-A novel, 9b 1GS/s 2-stage pipeline ADC architecture enables high performance with a low-gain op-amp and poor accuracy in the sub-ADC comparators. A reduced MDAC gain of two relaxes the op-amp gain and bandwidth requirements by a factor of 5.7. Deliberate and random comparator mismatch set the trip-points in the 2nd stage flash sub-converter and decouples performance from matching requirements. Digital trimming of a delay chain eliminates mismatch in the sampling paths to provide a simple, low power alternative to a dedicated front-end SAH. The ADC achieves an ENOB of 7.4b at Nyquist, consumes 27mW from a 1.0V supply, yielding an FOM of 160fJ/conversion-step.**

I. Introduction

Future high-speed communications systems and emerging communication standards require analog to digital converters (ADCs) in nanometer CMOS processes with both high bandwidth and dynamic range. For mobile applications and for applications where several ADCs must be integrated on a single chip, the power efficiency of these ADCs becomes critical. The time-interleaved pipeline and SAR architectures, are extensively employed for moderate resolution Giga-Sample per second conversion. However, interleaving of sampling is challenging, and complex calibration algorithms are required to correct for gain, offset and timing mismatch between channels. Furthermore, the high op-amp gain required even in conventional moderate-resolution pipeline ADCs is challenging in 45nm CMOS and below where the transistor self-gain is ~10. On the other hand, interleaved SAR ADCs consume considerable die area. Comparator redundancy makes the flash ADC architecture ideal for advanced processes because it decouples accuracy and performance [1] however thermal noise limits efficient operation to 6 bits or less.

We introduce a new combination of redundancy and pipelining that relaxes the op-amp gain and bandwidth requirements and at the same time facilitates the use of an efficient low-resolution redundancy based flash sub-ADC. This pipelined architecture exploits redundancy to take advantage of compact energy-efficient, digital-like dynamic comparators. The two-stage pipeline reduces the required resolution of the 2nd stage flash sub-ADC to 6 bits so that it can benefit from a redundant comparator design. Pipelining in 45nm CMOS is enabled by a high feedback factor approach, which allows the use of a simple, low-gain op-amp. The front-end sample and hold (SAH) is eliminated to further improve energy efficiency. The 9bit, 1GS/s 45nm SOI-CMOS prototype achieves a peak ENOB of 7.8b, no missing codes at 9b resolution and consumes only 27mW at 1GS/s from a 1V supply. This non-interleaved 9bit ADC occupies only 0.125mm^2 and achieves a figure of merit (FOM) of 160fJ/conversion-step at Nyquist.

II. Architecture and Circuit Implementation

A. Overview

As shown in Fig. 1, the proposed ADC architecture pipelines a 4b flash-based MDAC with a 6b flash ADC sub-converter. A high-feedback-factor two-stage pipeline architecture is key to exploiting the performance of the 45nm SOI process. In particular, two-stage pipelining allows efficient redundancy-based flash sub-ADCs to be used in the first and second stages. The second stage 6bit sub-ADC employs redundancy and re-assignment to achieve a low second-stage FOM of only 170fJ/conversion-step. Comparator redundancy and reassignment [1] decouple performance from transistor matching. This enables the use of low-precision, dynamic comparators that are optimized for speed and efficiency

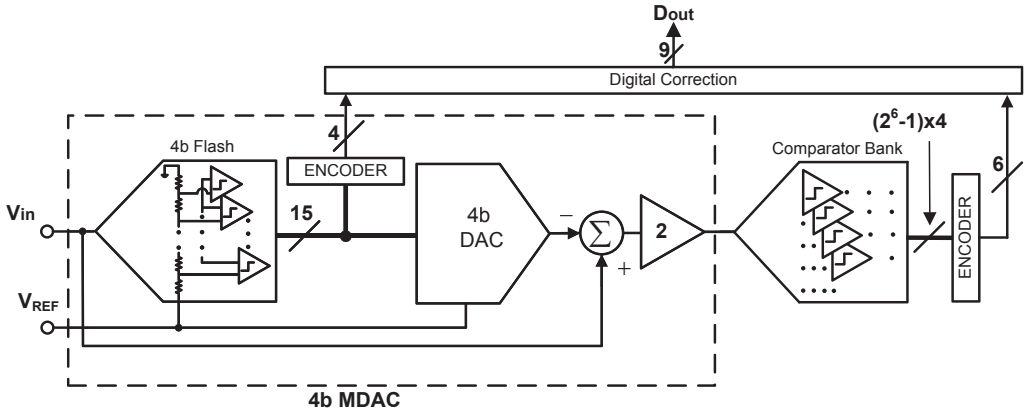

Fig. 1 Simplified single-ended representation of ADC architecture.

instead of accuracy. Furthermore, deliberate and random mismatch set the desired trip-points in the 6 bit sub-ADC, eliminating the need for a power-hungry low-impedance high-precision resistor reference ladder [2]. Similarly, comparator redundancy improves the energy efficiency and reduces the input capacitance of the 1st stage sub-ADC. A 1bit over-range in the 2nd stage sub-ADC compensates for 1st stage comparator offsets.

Reducing the MDAC gain from 16 to 2 increases the MDAC feedback factor (β) from 1/17 to 1/3, yet still sufficiently relaxes the noise requirement of the 2nd stage sub-ADC. A relatively high feedback factor of 1/3 allows a simple low-gain telescopic amplifier to be used. Critically, this increased β enables a 5.7X reduction of both the required op-amp open-loop gain and the required op-amp bandwidth. The lower MDAC gain also has the important benefit of reducing the output voltage swing by a factor of four, providing more headroom for simple cascoding to achieve gain [3].

A simple clock skew calibration block corrects timing mismatch between the MDAC and its sub-ADC, allowing the elimination of the power-hungry conventional front-end sample and hold.

B. 1st stage sub-ADC

Fig. 2 shows the MDAC and first-stage 4b sub-ADC. The 1st stage comparators, which achieve a 75ps decision time, are based on [4] but adapted to use floating-body FETs which have a speed, power and area advantage over body-contacted devices. SOI memory effects are eliminated by resetting the comparator inputs to a common mode voltage and resetting all internal nodes to either the supply or ground prior to the comparison phase. Furthermore, a redundancy of two comparators per level reduces the total capacitance and area of the input pair by 33% for the same yield. This enables the use of smaller sampling capacitors in the first stage sub-ADC. Comparators with the lowest offset are chosen at startup.

C. Op-amp

The op-amp (Fig. 3(a)) is a telescopic, NMOS-input, triple-cascode amplifier with a minimum gain of 42dB. A tunable negative resistance increases the overall output resistance enabling a maximum gain of 63dB. All devices are body-contacted, 56nm channel length FETs to avoid memory effects associated with floating-body transistors. The tail transistor is biased in triode with a 40mV V_{DS} while all other FETS are biased in saturation with a 160mV V_{DS}. An 85mV V_{DSAT} ensures sufficient headroom to support a maximum pk-pk output swing of 150mV with a 1V supply. The reduced MDAC gain in this ADC and corresponding increase in feedback factor to 1/3 means that an open-loop unity gain frequency of 7.5GHz is sufficient for 1GS/s operation.

D. Elimination of SAH

The speed of the 45nm process is leveraged to implement a simple clock-skew calibration of a delay chain in the sampling paths which allows the elimination of a dedicated front-end sample and hold circuit. The delay consists of programmable inverter delay chains in the clock paths of the MDAC and its sub-ADC (Fig. 2). Delay increments of 7ps provide sufficient granularity within a 48ps window to correct for sampling skew and prevent ADC performance degradation at high input frequencies.

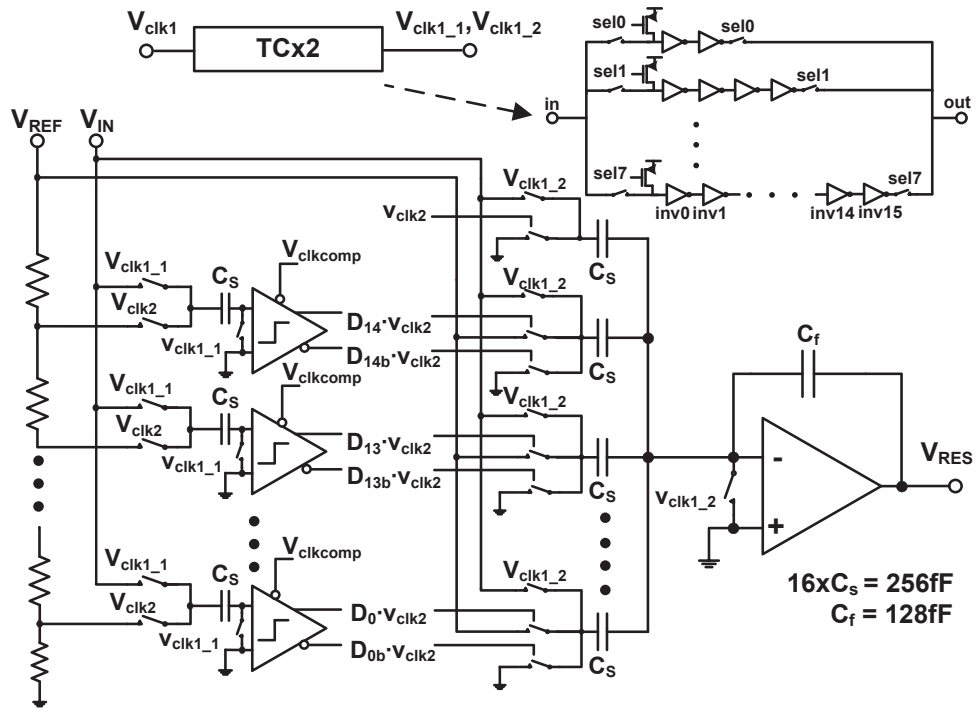

Fig. 2 Single-ended representation of differential 4-bit MDAC.

E. 2nd stage sub-ADC

The 6b 2nd stage sub-ADC is implemented as a comparator bank that incorporates redundancy and re-assignment to correct DNL errors [1]. A combination of deliberate and random offsets determines the comparator thresholds [2] and eliminates the need for a low impedance, high precision resistor reference ladder. Unlike conventional approaches, these techniques decouple comparator performance from matching requirements so that small and fast comparators can be employed.

The 2nd stage sub-ADC comparators, also based on [4], consist of floating-body FETs that leverage sub-micron device widths for power and speed and exhibits large offset suited for redundancy and reassignment. Deliberate offsets are introduced by asymmetric loading of the drain nodes of the differential pair as shown in Fig. 3 (b). Twelve variants of a floating-body MOS capacitor enable a 2nd stage sub-ADC input range from -50mV to 150mV in 12.5mV increments. This method, unlike asymmetric sizing of the input pair [2], does not tradeoff comparator input capacitance for deliberate offset and results in a comparator input capacitance less than 1fF.

A 1 σ comparator random offset of 17 ADC-LSBs and a comparator redundancy of four-per-code provide sufficient granularity in between deliberate offsets to ensure an overall ADC ENOB greater than 8.5bits with 90% yield. Furthermore, SOI memory effects are eliminated by resetting the comparator inputs to a common mode voltage and resetting all internal nodes to either the supply or ground prior to the comparison phase.

F. Calibration

At power-on, an off-chip calibration engine initiates a search algorithm to select comparators closest to the desired trip points for both 1st and 2nd stage sub-ADCs [2]. Furthermore, calibrating the 2nd stage sub-ADC through the ADC input corrects errors due to finite op-amp gain and offset. The simplicity of this calibration approach not only corrects DNL errors, but also eliminates the need for digital correction beyond 1st stage comparator offset compensation.

For each sub-ADC code, the algorithm sequentially enables trial comparators and instructs an off-chip digital-to-analog converter (DAC) to apply input voltages about a desired sub-ADC trip voltage. When a comparator with an actual trip-point near the ideal trip-point is located, the algorithm assigns the comparator to the sub-ADC code and proceeds to the next code. The process continues until a comparator for each sub-ADC code is found.

G. Encoder

The outputs of the 1st and 2nd stage sub-ADCs are routed to dedicated encoding blocks [2] and summed to form a 4-bit and 6-bit word respectively. Summation of logic ones at the encoder inputs guarantees monotonicity and permits comparators to seamlessly be re-assigned to any code. Digital correction is off-chip.

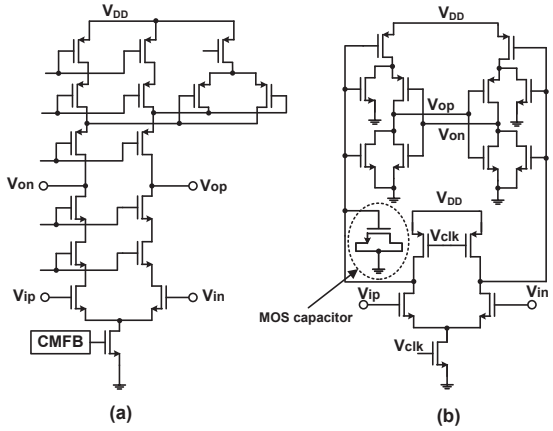

Fig. 3 (a) MDAC op-amp with gain enhancement and (b) 2nd stage sub-ADC comparator with MOS capacitor for deliberate offset.

III. Measurement Results

The prototype, fabricated in a 45nm SOI-CMOS process, occupies a core area of 0.125mm^2. A die micrograph is shown in Fig. 4. The prototype ADC has a differential input signal range of 800mV$_{pp}$ and input capacitance of 500fF. The maximum measured DNL/INL values are 0.75/1.17LSB (Fig. 5). Fig. 6 shows the output spectrum for a 500.5MHz input signal sampled at 1GS/s, with and without clock skew calibration. The output data is decimated by 16X for reliable transmission off-chip. Fig. 7 shows the measured SNDR and SFDR versus input frequency at 1GS/s with and without clock skew calibration. A 3.5dB improvement in SNDR is observed for Nyquist-rate and 750MHz input signals. The ADC achieves an ENOB and SFDR of 7.8bits and 61.6dB, respectively, at low frequency and 7.4 bits and 52.7 dB at Nyquist. The ADC consumes a total of 27mW from a 1V/1V analog/digital supply and achieves an FOM of 160fJ/conversion-step. Table I shows the performance summary of the prototype ADC.

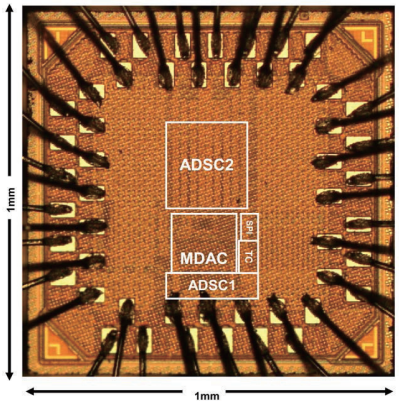

Fig. 4 Die micrograph of 45nm SOI-CMOS ADC.

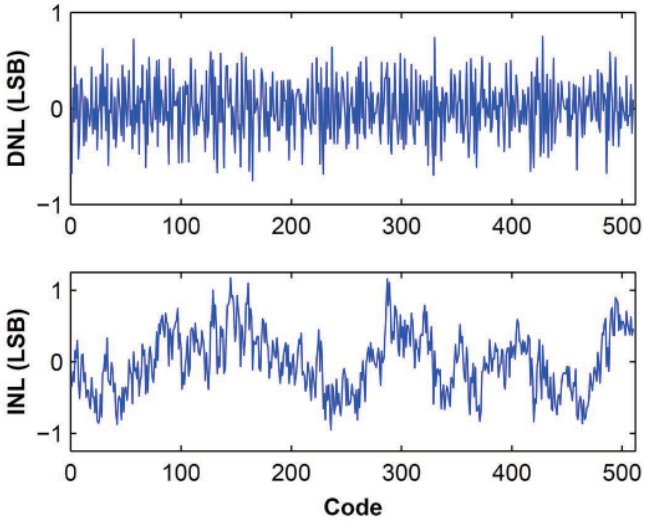

Fig. 5 Measured DNL and INL.

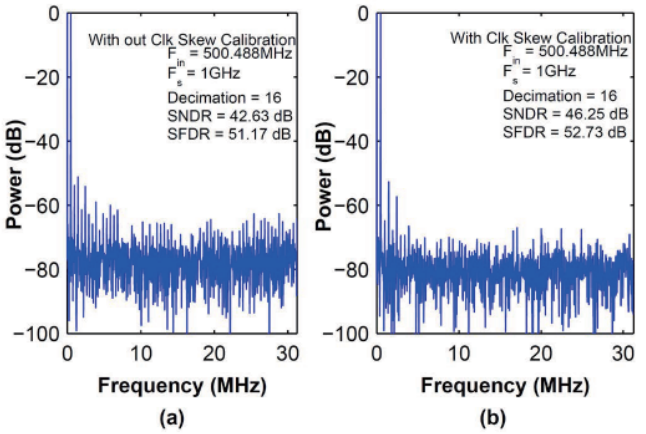

Fig.6 Output spectrums for 500.49MHz input and 16X decimation without (a) and with (b) clock skew calibration.

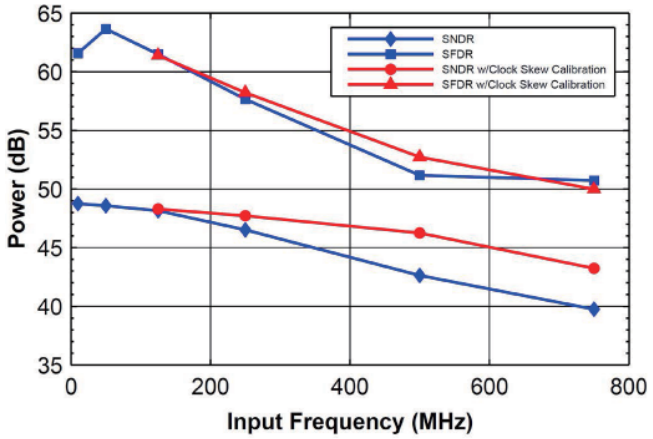

Fig. 7 Measured SNDR & SFDR vs. F_{in} (F_s=1.0GS/s) with and without clock skew calibration.

TABLE I
ADC PERFORMANCE SUMMARY

Technology	45nm SOI-CMOS
Supply	1.0V
Resolution	9bit
Input Range (Differential)	800mV$_{PP}$
Sampling Rate	1GS/s
Power Consumption	27mW
DNL/INL	0.75/1.17LSB
SFDR @ Nyquist	52.7dB
SNDR @ Nyquist	46.3dB
ENOB @ Nyquist	7.4
FOM	160fJ/Conv-step

IV. CONCLUSION

This paper introduces a SAH-less 9b 1GS/s two-stage pipeline ADC that incorporates a new combination of redundancy and pipelining. The trip-points of the 2nd stage comparators are set purely by random and deliberate offsets to decouple ADC performance from matching requirements. Only twelve deliberate offsets and a 1σ comparator random offset of 17 ADC-LSBs with a redundancy of only four gives sufficient granularity to limit SNR degradation to less than 3dB with 90% yield. Reducing the gain from 16 to 2 in the 4b MDAC increases the feedback factor (β) from 1/17 to 1/3 which substantially relaxes the op-amp gain and bandwidth requirements by a factor of 5.7. Furthermore, the reduced op-amp output swing enables extensive cascoding with only a 1V power supply. Finally, the front-end sample and hold is substituted with digital trimming of a delay chain that matches the sampling paths of the 1st stage sub-ADC and MDAC.

The architecture scales with CMOS technology and benefits from the power and speed advantages associated with each new process node. The prototype ADC achieves a Nyquist FOM of 160fJ/conversion-step and has one of the best energy efficiencies among reported 1GS/s+ ADCs with ENOB > 7b.

ACKNOWLEDGMENT

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