

# A Wirelessly Powered Log-based Closed-loop Deep Brain Stimulation SoC with Two-way Wireless Telemetry for Treatment of Neurological Disorders

Hyo-Gyuem Rhew<sup>1</sup>, Jaehun Jeong<sup>1</sup>, Jeffrey A. Fredenburg<sup>1</sup>, Sunjay Dodani<sup>2</sup>, Parag Patil<sup>3</sup>, Michael P. Flynn<sup>1</sup>

<sup>1</sup>Electrical Engineering and Computer Science, University of Michigan, Ann Arbor, MI

<sup>2</sup>Biomedical Engineering, University of Michigan, Ann Arbor, MI

<sup>3</sup>Department of Neurosurgery, University of Michigan, Ann Arbor, MI

## Abstract

A log-based closed-loop Deep Brain Stimulation system detects and processes low-frequency brain field signals to optimize stimulation parameters. The fully self-contained single-chip system incorporates LNAs, a log-ADC, digital log-filters, a log-DSP with a PI-controller, current stimulators, a two-way wireless transceiver, a clock generator, and an RF energy harvester. The 2x2mm<sup>2</sup> 180nm CMOS prototype consumes 468μW for recording and processing neural signals, stimulation, and for two-way wireless communication.

## Introduction

Deep brain stimulation (DBS) of the subthalamic nucleus is an effective therapy for numerous neurological disorders, including Parkinson's disease, which affects more than 1.5m people in the US [1]. However current treatment systems require monthly or weekly adjustment by trained clinicians. Despite more than a decade of research, effective closed-loop optimization of stimulation parameters, which would greatly improve quality of life, remains elusive. Recently, several SoCs incorporating both neural recording and stimulation have been described [2], but these lack true closed-loop capability. Spike sorting and principal component analysis (PCA) disentangle neural spikes [3,4], but this approach is not effective for closed-loop DBS. Moreover, spike sorting with PCA requires significant computation, making RF-powered or even long-term battery-powered operation difficult.

We present the first wirelessly-powered closed-loop DBS SoC with RF telemetry. Our device implements stimulation control based on analysis of Local Field Potential (LFP) energy, as proposed in recent brain research [5]. Energy efficiency is improved with a novel, highly efficient log-domain signal processing chain that incorporates a log-ADC, digital log-filters, and a log-DSP. The reduced power consumption makes operation with RF energy harvesting feasible. In addition to recording and stimulation capabilities, the single chip device incorporates RF energy harvesting, voltage regulation, clock generation, and a two-way wireless transceiver, to achieve a true self-contained

solution. The SoC also incorporates support for optical stimulation.

## System Architecture

Fig. 1 shows the overall system. As neural signals are elegantly expressed in logarithmic scale, we improve energy efficiency by introducing a complete log-domain neural recording and processing chain. Four band-pass LNAs amplify neural signals and these signals are multiplexed to a 100kSample/s 8b pipeline log-ADC. A new log-ADC scheme eliminates the dead zone in earlier log-ADCs [6]. Furthermore, log-domain digital filtering is introduced to efficiently process the log-scale digital output from the ADC, saving power consumption by avoiding multiplication. Similarly, the log-DSP calculates LFP energy by simple bit-shifting instead of squaring.

Uniquely, the DSP includes a programmable PI-controller that evaluates the LFP energy to set the optimal stimulation amplitude. An advantage is that the closed-loop feedback is based on low-pass-filtered LFP signals, making it robust to high-frequency stimulation artifacts. There are six 6b general-purpose (116μA) stimulation channels and two 6b high-current (4.2mA) channels. The high-current channels can also drive LEDs for optogenetic applications.

For battery-less operation, an on-chip energy harvester, comprised of a rectifier and two on-chip LDOs, recovers energy to power the entire system from a 915MHz RF carrier. The single-chip system also incorporates a bandgap reference, bias circuitry and a clock generator. The stimulation parameters can also be set manually via a 2.4GHz wireless downlink. The device also includes an 800kbps power-efficient backscatter RF transmitter that can communicate recorded LFP, spike or raw data wirelessly to an external base station. Compared to [2], the prototype has fully complete DSP, a more efficient recording chain, and also incorporates two-way wireless interface, RF energy harvesting, power management and clock generation.

## Circuit Implementation

The log-ADC improves on that in [6] to achieve a dynamic range of 59dB by removing the dead zone (Fig. 2), where otherwise small signals are compressed below the quantization

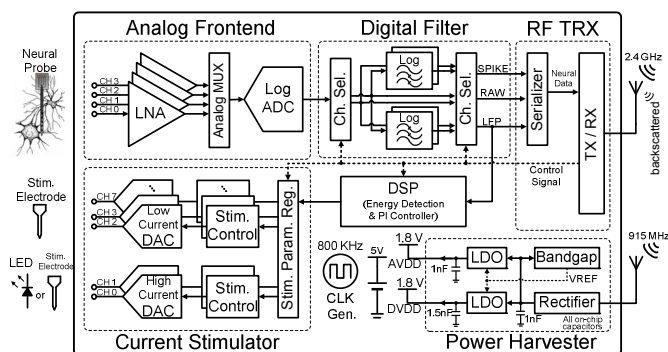


Fig. 1. Overall system block diagram of the proposed log-based closed-loop DBS system.

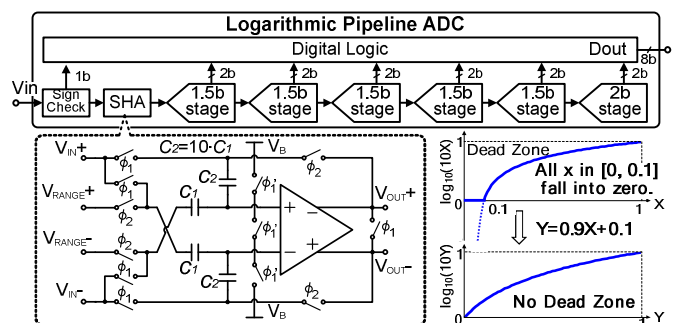


Fig. 2. Simplified schematic and operation of log-ADC.

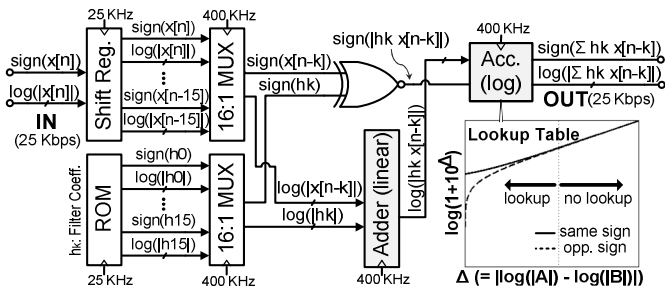


Fig. 3. Block diagram of logarithmic digital filters.

range. The dead-zone elimination scheme is embedded in SHA of the log-ADC.

We improve energy efficiency by taking advantage of the logarithmic output of the ADC to introduce log-domain digital signal processing. The log-filters (Fig. 3) consume 48% less power than equivalent linear-filters. Low-pass and high-pass 15<sup>th</sup> order FIR filters simultaneously separate low-frequency LFPs and high-frequency spikes. These log-filters replace power-hungry multipliers with adders. A look-up table method is used for logarithmic accumulation. Further power reduction is achieved by avoiding accumulation when the difference of the two inputs is larger than a threshold where the output is simply and accurately approximated as the larger input. The log approach also simplifies the PI-controller, which optimizes stimulation amplitude based on LFP energy. Moreover, instead of squaring, simple 1b left-shifting determines the energy of the log-domain LFP signals in the log-DSP.

The LNAs consist of a cascade of two band-pass filters. The current stimulators include parameter registers, biphasic stimulation controllers, and 6b current DACs. Backscatter modulation is exploited in the transmitter to minimize power consumption, achieving an energy consumption of 6.25pJ/b. The receiver demodulates a PWM input to set the parameters of the PI-controller and the stimulators.

The system is entirely powered by the RF energy harvester except for the high-current DACs, which require a 5V battery. A full-wave self-threshold-compensated rectifier based on [7] has the body of each FET tied to the drain for lower on-resistance and less reverse-bias leakage. A source-coupled relaxation oscillator generates the 800kHz system clock.

### Measurement Results

The prototype is fabricated in 180nm CMOS and occupies 2x2 mm<sup>2</sup> (Fig. 7). The measured total power consumption of the system is 468μW. The measured performances of the

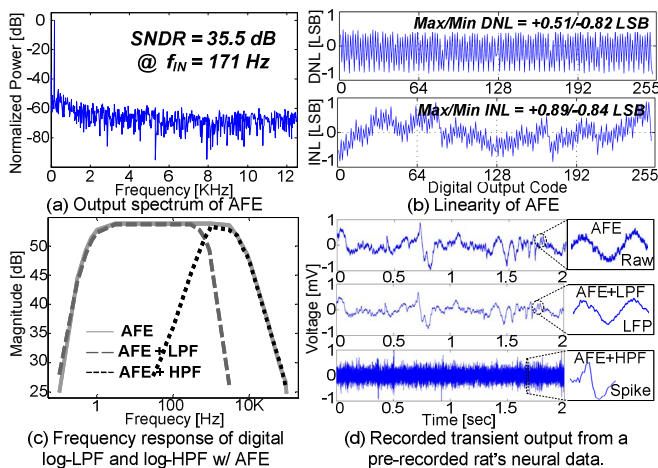
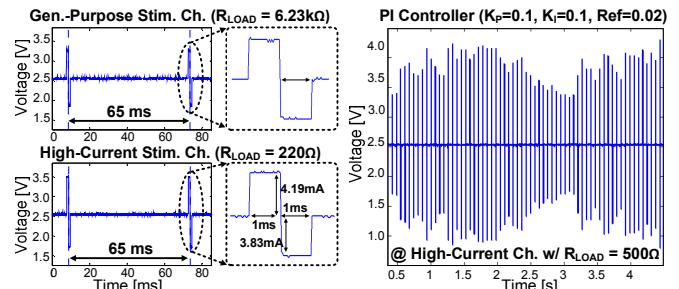


Fig. 4. Measured performance of AFE (LNAs+log-ADC) and logarithmic digital low-pass and high-pass filters at 27°C.



(a) Gen.-purpose and high-current stim. (b) A high-current stim. ch. in closed-loop mode using LFP energy detection.

Fig. 5. Measured stimulation current waveforms at 27°C.

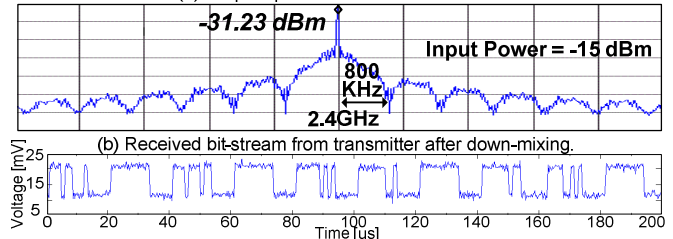
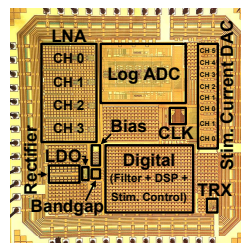


Fig. 6. Measured performance of RF transmitter at 27°C.

analog frontend (AFE: log-ADC + LNAs) and digital log-filters are shown in Fig. 4. The SNDR and maximum DNL/INL of the AFE are 35.5dB and 0.82 LSB/0.89 LSB, respectively. The LNAs achieve a measured gain of 54dB over a passband from 0.64Hz to 6kHz. Both the low-pass and high-pass digital filters have a 3dB cutoff frequency of 700Hz. Measured raw, LFP and spike recordings of a pre-recorded rat-brain neural signal recorded by the prototype are also shown in Fig. 4. Fig. 5 shows measurements of stimulation current pulse trains. As demonstrated in Fig 5 (b), the closed loop system adapts the stimulation current in real-time responding to the energy of input LFP signals. Fig. 6 shows the measured output spectrum and transmitted bit stream of the backscatter transmitter.



AFE Power	245 μW
Digital (Filter + DSP + Stim. Controller) Power	138 μW
TX/RX Power	5/4.6 μW
Total Power	468 μW
Estimated Rectifier Power	52% @ I_LOAD =
Conversion Efficiency	350 μA

Fig. 7. Die photo and power breakdown for the prototype system.

### Conclusions

We present the first fully self-contained wirelessly-powered closed-loop DBS SoC based on the analysis of LFP energy. Log-domain signal processing improves energy efficiency allowing wirelessly powered operation and a two-way wireless interface adds to the flexibility of the device. This work was funded in part by the Catalyst Foundation.

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